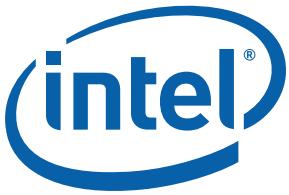

Enabling TMII Hardware on Intel® IXP435 Network Processors

Application Note

December 2008

Order Number: 319092-001US

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Revision History

Date	Revision	Description
December 2008	001	Initial release of document

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1.0 Introduction

The TMII (Turbo Media Independent Interface) also named as Turbo MII is used to increase the MII clock from 25 MHz to 50 MHz. The purpose of the Turbo MII is to enhance LAN throughput performance by doubling the MII clock rate.

The complete solution has been validated on the hardware platform of Flexcomm* called as CRONUS1000 using the Intel® IXP435 Network Processor.

1.1 Purpose

The objective of this application note is to illustrate the hardware block diagram that has been validated while working on the Flexcomm CRONUS1000 using the Intel® IXP435 Network Processor.

The following sections explain the block diagram of the TMII construction.

Note: The Flexcomm CRONUS1000 has been validated using the Intel® IXP400 Software v3.0.1 only. The hardware guide below is based on the TANTOS-3G* Switch (PSB6973) from Infineon*.

1.2 Intended Audience

This application note is targeted for those who intend to enhance the throughput performance of their system using the TANTOS-3G switch (PSB6973).

1.3 Acronyms

Acronym	Description
MII	Media Independent Interface
TMII	Turbo MII or Turbo Media Independent Interface

1.4 Related Documents

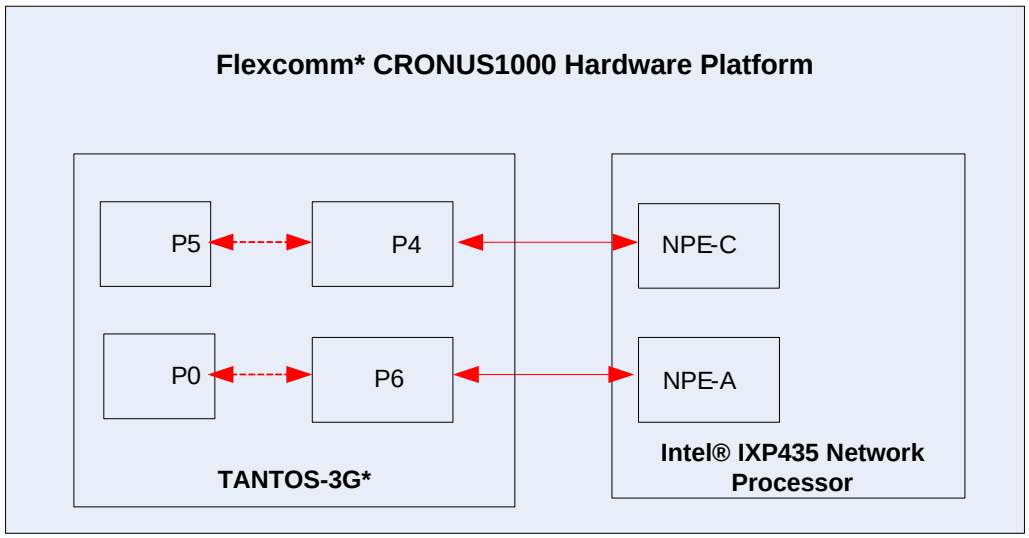
Document Title	Document Number
Intel® IXP43X Product Line of Network Processors Developer's Manual	316843
Intel® IXP400 Software Programmer's Guide v3.0	252539
Intel® IXP400 Software Release 3.0 Software Release Notes	-
Intel® IXP400 Software Release 3.0.1 Readme	-

2.0 Flexcomm* CRONUS1000 Block Diagram

Figure 1 shows the block diagram of the Flexcomm CRONUS1000.

The solid lines show the connection between the IXP435 network processor and TANTOS-3G switch. The dotted lines show the internal VLAN connection of individual ports in the TANTOS-3G switch. The VLAN connections can be configured by the software.

Figure 1. Block Diagram of Flexcomm* CRONUS1000 Hardware Platform



3.0 Hardware Reference Block Diagram

Figure 2 shows the connection between the IXP435 network processor and TANTOS-3G switch.

The data, clock, and control signals should be terminated with a 33 ohm series resistor for drive strength adjustment and must be placed very close to the driver. The Collision signal and RX_Error signal are not used in the implementation, and therefore should be tied to the ground.

A 50 MHz oscillator with 50 ppm is recommended. It must be placed at the center of the RXCLK / TXCLK trace (in between the IXP435 network processor and TANTOS-3G) to ensure same clock propagation to each device. Place a 33 ohm series resistor close to the oscillator output pin. This value should be adjusted to optimize signal integrity depending on the oscillator drive strength.

It is recommended to length match (ball to ball) the DATA, and TXCLK/RXCLK traces within 400 mils.

If you use a 5 mil trace width, ensure that the trace separation of TX data, RX data, TXCLK, and RXCLK is at least 10 mil. Avoid parallelism on these signal traces. Trace impedance of 50-60 ohm should be used.

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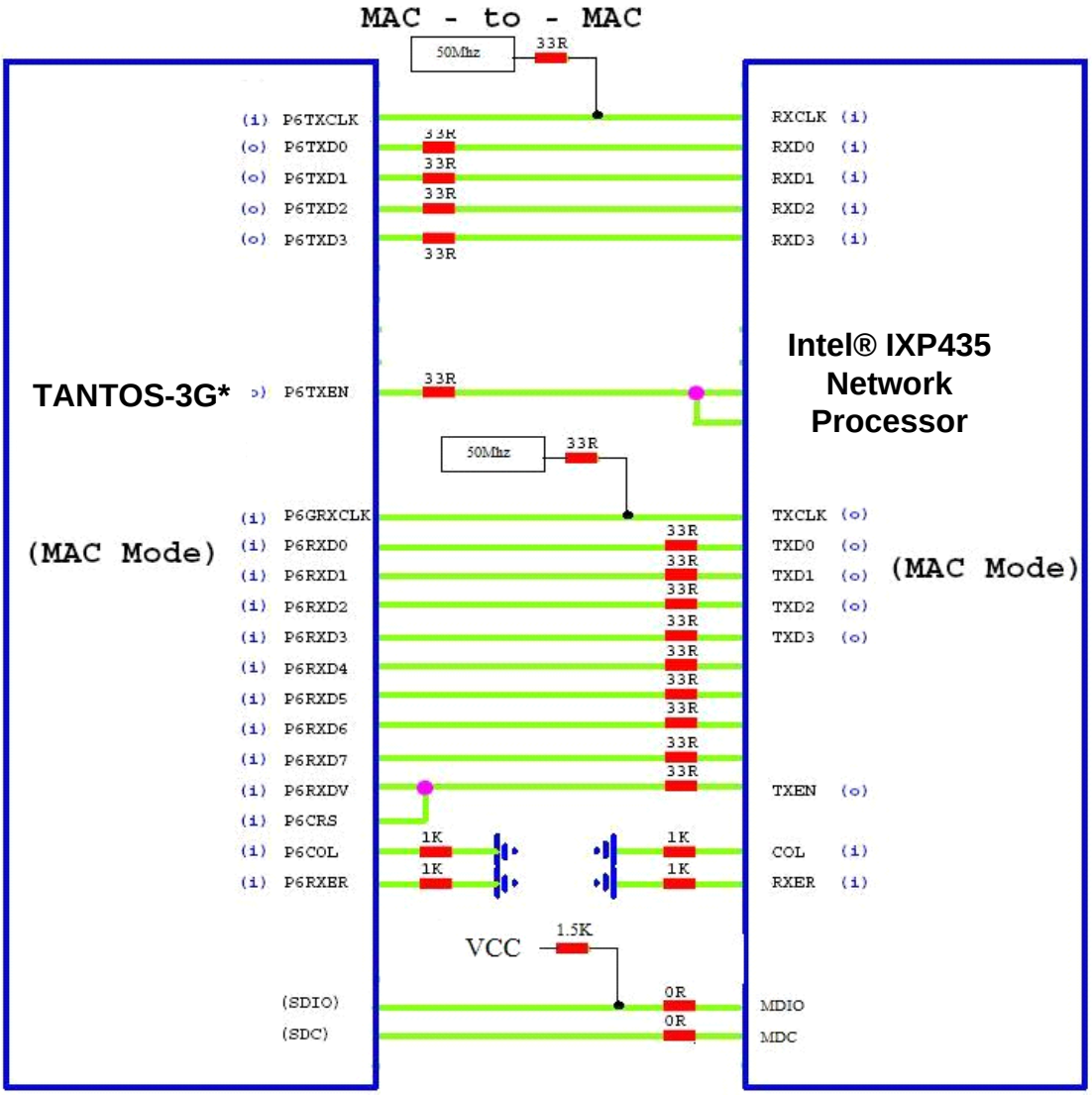
The MDIO/MDC management pins on the IXP435 network processor should be connected to the SDIO/SDC pins on the TANTOS-3G switch. A pull up resistor of 1.5 Kohm to VCC (3.3V) is required on the MDIO pin.

Figure 2. TMII Connection between the Intel® IXP435 Network Processor and TANTOS-3G* Switch (from Infineon*)



4.0 Software Enabling

The enabling TMII software for the Flexcomm CRONUS1000 is available on the Intel Developer web site.

The following software packages are needed:

- Intel® IXP400 Software v3.0
- Intel® IXP400 Software v3.0.1 patch

The required software components are:

- Hardware access library
- NPE microcode
- Ethernet Device Driver

Refer to the *Intel® IXP400 Software v3.0.1 Readme* available on the Intel Developer web site for further information.

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