Intel® IXP42X Product Line and IXC1100 Control Plane Processor: Using the Intel® LXT973 Ethernet Transceiver

Application Note

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Revision History

Date	Revision	Description
July 2004	002	Updated Intel® product branding.
July 2003	001	First release of this document

1.0 Introduction

This application note presents guidelines on how to replace two Intel® LXT971A/972A Fast Ethernet Transceivers with one Intel® LXT973 Low-Power, Two-Port, Fast-Ethernet Transceiver when interfacing with a device from the Intel® IXP42X product line or with an Intel® IXC1100 Control Plane Processor. The procedure is not a totally straightforward component swap.

1.1 Assumptions

It is assumed readers are familiar with the following:

- The Ethernet implementation in the Intel® IXDP425 / IXCDP1100 Development PlatformSchematics
- Intel® IXP400 Software versions 1.1 and 1.2.1
  - The Ethernet access component
  - IxEthAccMii.c/h, in particular
- MII specification described in *IEEE Standard 802.3, Part 3*, 2000 Edition

Note: See the table in "Related Documents and Materials" on page 6.

1.2 Applicability

This application note applies to all the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor, except for the IXP421 network processor. Since the IXP421 only has one Ethernet interface, it makes little sense to use the two-port LXT973 Ethernet Transceiver with it.

This document also applies to the Intel® IXDP425 / IXCDP1100 Development Platform.

The software section applies to Intel® IXP400 Software Releases 1.1 and 1.2.1.

1.3 Related Documents and Materials

Title	Document Number Location
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update	252702
Intel® IXP4XX Product Line Software Release 1.2.1 Software Specification Update	273795
Intel® IXDP425 Development Platform schematics	N/A
Intel® IXP400 Software Versions 1.1 and 1.2.1	http://developer.intel.com/design/network/products/npfamily/ixp425swr1.htm
Intel® LXT971A Datasheet	249414 http://developer.intel.com/design/network/
Intel® LXT972A Datasheet	249186
Intel® LXT973 Datasheet	249426
Intel® LXT971A-to-LXT973 Migration Guide	250014
Intel® LXT973 10/100 Mbps Dual Port Fast Ethernet PHY Specification Update	249737
IEEE Standard 802.3, Part 3, 2000 Edition	N/A http://www.ieee.org

1.4 Definition and Acronyms

ANE	Auto negotiate
CLK	Clock
COL	Collision detect
CRS	Carrier sense
ECL	Emitter-coupled logic
FX	Transmission over fiber-optic cable
GPIO	General-purpose input/output
HW	Hardware
IEEE	Institute of Electrical and Electronics Engineers
IF	Interface
ISR	Interrupt service routine
IXC	Internet Exchange Carrier

IXP	Internet exchange processor
JTAG	Joint Test Action Group
LED	Light-emitting diode
MAC	Media-access controller
MDC	Management data clock
MDDIS	Management data disable
MDI	Media-dependent interface
MDIO	Management data input/output
MDIX	Media-dependent interface crossover
MII	Media-independent interface
NC	Not connected
NPE	Network processor engine
PHY	Physical
RMII	Reduced, media-independent interface
RX	Receive
SW	Software
TX	Transmit
TX_ER	Transmit error
UTP	Unshielded twisted pair

1.5 Overview

The LXT973 Ethernet Transceiver is not a direct, 100%-compatible replacement with two LXT972A Ethernet PHYs. Because of that, swapping the devices will not work “straight out of the box” with the Intel® IXP42X product line and IXC1100 control plane processors.

This application note presents the necessary hardware and software methods needed to interface the LXT973 Ethernet Transceiver — instead of two LXT972A Ethernet PHYs — with Intel® IXP42X product line and IXC1100 control plane processors.

Using the hardware design of the IXDP425 / IXCDP1100 platform as a base, this document details how hardware differences between the two PHYs may be addressed. It also lists PHY errata and how that may be addressed. This document concentrates on the interface between the LXT973 Ethernet Transceiver and the network processor.

Finally, this document addresses why Intel® IXP400 Software Releases 1.1 and 1.2.1 will need modification to work with the LXT973 Ethernet Transceiver. Some suggestions are given on how these modifications may be done.

2.0 Hardware Modifications

This section presents the hardware methods needed on the processor interface to replace the LXT972A Ethernet PHY with the LXT973 Ethernet Transceiver.

The LXT972A Ethernet PHY has a subset of the functionality of Intel® LXT971A Fast Ethernet Transceiver. For more information, see the datasheets of these two components. Since the LXT972A Ethernet PHY is used on the IXDP425 / IXCDP1100 platform, it will be referred to throughout the remainder of this document.

The information presented will be in five main sections:

- MII interface — An overview on how the Ethernet interface is implemented on Intel® IXP42X product line and IXC1100 control plane processors
- LXT973 Ethernet Transceiver — The capabilities of the LXT973 Ethernet Transceiver PHY
- Hardware differences between LXT972A Ethernet PHY and LXT973 Ethernet Transceiver
- Board-design considerations — General board design with the LXT973 Ethernet Transceiver
- Pin Connectivity Interconnect Guide — Pin-by-pin comparison of the Intel LXT972A Ethernet PHY with the LXT973 Ethernet Transceiver PHY

2.1 Device's Ethernet MII Interfaces

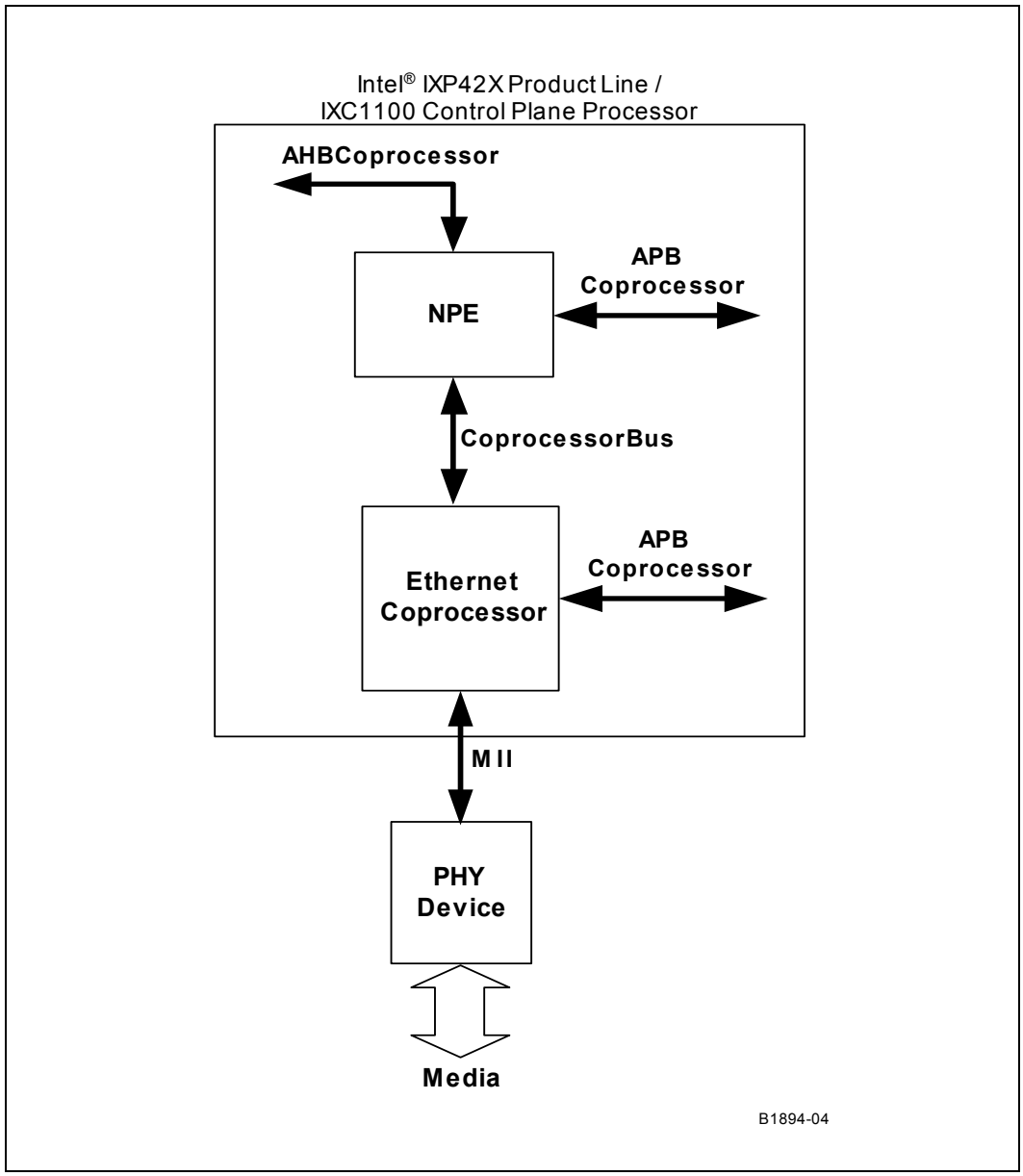
Two standard compliant MII interfaces are provided to the 10/100-Mbps MACs that are internal to Intel® IXP42X product line and IXC1100 control plane processors. The MII interface allows connection of an external, MII-compliant PHY.

Internal to Intel® IXP42X product line and IXC1100 control plane processors, the NPE coordinates all the data transfers between the Ethernet coprocessor and memory. The MAC is internal to the Ethernet coprocessor.

For more details, see *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual* (252480).

Figure 1 shows the architecture of the Ethernet implementation for Intel® IXP42X product line and IXC1100 control plane processors.

Figure 1. Ethernet System Overview



2.2 Intel® LXT973 Low-Power, Two-Port, Fast-Ethernet Transceiver: Overview

The LXT973 Ethernet Transceiver is a dual, 10/100-Mbps Ethernet PHY transceiver with two MII interfaces. The device has:

- Two independent, IEEE 802.3-compliant 10Base-T / 100Base-TX (FX) 10/100-Mbps ports
- Low power consumption – Typically, 250 mW per port

- Independent MII with extended registers for each port
- Automatic MDI/MDIX
- Next-page exchange
- Auto-negotiation on each port
- Integrated termination resistors
- Device configuration via MDIO port or via external control pins
- Fiber-optic support (via Pseudo-ECL) on each port
- 2.5-V and 3.3-V I/O compatibility
- All features supported at cable lengths up to 200 m
- Intel Carrier-Class Ethernet Support

2.3 Hardware Differences Between the Two PHYs

This section describes the hardware differences between the two PHYs.

2.3.1 Management Data Interrupt Signal (972A Only)

An active-low output on this pin indicates a status change. While this signal is used in the hardware design of the IXDP425 / IXCDP1100 platform and each MDINT is tied, by default, to GPIO 4 and 5 of Intel® IXP42X product line and IXC1100 control plane processors, Intel® IXP400 Software does not utilize the interrupts. Instead, the PHY is polled for status changes.

2.3.2 IEEE 1149.1 Boundary Scan Test Port (972A Only)

The LXT972A Ethernet PHY is one of several devices that may be included in a single JTAG chain on the IXDP425 / IXCDP1100 platform. The LXT973 Ethernet Transceiver does not have a JTAG interface. Consequently, if a LXT973 Ethernet Transceiver daughter card is developed and used on IXDP425 / IXCDP1100 platform, leave the following pins as NC (not connected):

- J9/3-4
- J9/5-6
- J9/25-26
- J9/27-28

Also ensure that J8/6 and J8/7 are bypassed in the JTAG chain.

2.3.3 LED Configuration Register (972A Only)

The LXT973 Ethernet Transceiver has limited LED configurability compared with LXT972A Ethernet PHY. This may cause problems in designs where both PHYs have to share the same LED configuration.

The LXT972A Ethernet PHY provides an LED configuration register to allow the software driver to control the LEDs. This allows for a large combination of different functions. For all possible combinations, see *Intel®LXT972A Datasheet* (249186).

On the LXT973 Ethernet Transceiver, LED functionality is controlled by LED configuration pins. There are two configuration pins for each PHY. For all possible combinations, see *Intel®LXT973 Datasheet* (249426).

2.4 Board-Design Considerations

For detailed design practises and design considerations other than the processor interface, see *Intel®LXT973 Datasheet* (249246).

2.4.1 Management-Disable Signal

The signals MDDIS0, on pin 20, and MDDIS1, on pin 19, of the LXT973 Ethernet Transceiver need to be pulled down by external 4.7-KΩ resistors.

As of the release date of this document, the latest version of *Intel®LXT973 Datasheet* (249426-002) incorrectly states that these signals are pulled down internally. The next release of that document will correct this error.

2.4.2 Management Data Input/Output Signal

The signals MDIO0, on pin 25, and MDIO1, on pin 23, of the LXT973 Ethernet Transceiver need to be pulled up to 3.3-V by an external 4.7-KΩ resistor as per the LXT973 Ethernet Transceiver reference design.

2.4.3 PHY-Device Address

IXP400 software releases 1.1 and 1.2.1 use PHY address 0 for PHY 0 and PHY address 1 for PHY 1. This is the default configuration for the LXT973 Ethernet Transceiver.

Thus, ADDR[1:4] configuration on pins 52-55 is not needed. Since unused address pins should not be left floating, these pins can be tied to ground, as stated in *Intel® IXDP425 Development Platform schematics*.

2.5 Pin Connectivity – Interconnect Guide

Table 1 shows the pin connectivity for the devices.

Table 1. Pin Connectivity Inter-Connect Guide

Processor Device	Ethernet 0 Connector (J13)	Ethernet 1 Connector (J6)	Boundary Scan Test Port/TCK TMS Selection Header	LXT972A Ethernet PHY 0	LXT972A Ethernet PHY 1	LXT973 Ethernet Transceiver
Ethernet Interface						
ETH_MDIO	ENET_MDIO	ENET_MDIO		MDIO	MDIO	MDIO0/MDIO1
ETH_MDC	ENET_MDC	ENET_MDC		MDC	MDC	MDC0/MDC1
ETH_TXCLK0	ENET0_TX_CLK			TX_CLK		TXCLK0
ETH_TXDATA0[3:0]	ENET0_TXD[0:3]			TXD[0:3]		TXD0_[0:3]
ETH_TXEN0	ENET0_TX_EN			TX_EN		TXEN0
ETH_RXCLK0	ENET0_RX_CLK			RX_CLK		RXCLK0
ETH_RXDATA0[3:0]	ENET0_RXD[0:3]			RXD[0:3]		RXD0_[0:3]
ETH_RXDV0	ENET0_RX_DV			RX_DV		RXDV0
ETH_COL0	ENET0_COL			COL		COL0
ETH_CRS0	ENET0_CRS			CRS		CRS0
ETH_TXCLK1		ENET1_TX_CLK			TX_CLK	TXCLK1
ETH_TXDATA1[3:0]		ENET1_TXD[0:3]			TXD[0:3]	TXD1_[0:3]
ETH_TXEN1		ENET1_TX_EN			TX_EN	TXEN1
ETH_RXCLK1		ENET1_RX_CLK			RX_CLK	RXCLK1
ETH_RXDATA1[3:0]		ENET1_RXD[0:3]			RXD[0:3]	RXD1_[0:3]
ETH_RXDV1		ENET1_RX_DV			RX_DV	RXDV1
ETH_COL1		ENET1_COL			COL	COL1
ETH_CRS1		ENET1_CRS			CRS	CRS1
GPIO4	ENET0_INT_N			MDINT		
GPIO5		ENET1_INT_N			MDINT	
Debug Signals						
ENET0_TCK			J9 25-26	TCK		
ENET0_TDI			J8 6	TDI		
ENET0_TDO			J8 8	TDO		
ENET0_TMS			J9 3-4	TMS		
ENET1_TCK			J9 27-28		TCK	
ENET1_TDI			J8 7		TDI	
ENET1_TDO			J8 5		TDO	
ENET1_TMS			J9 5-6		TMS	

3.0 Software Compatibility issues

The Ethernet access component in IXP400 software releases up to 1.2.1 is specifically written for the LXT972A Ethernet PHY.

This section describes the reasons why these versions of the IXP42X Ethernet Access software will not operate the LXT973 Ethernet Transceiver Ethernet PHY without prior software modification.

3.1 Programming Differences Between the Two PHYs

One major difference between LXT972A Ethernet PHY and LXT973 Ethernet Transceiver affects the Ethernet access component of the IXP400 software. The LXT973 Ethernet Transceiver does not support Status Register 2 (address 17).

The Ethernet access component of the IXP400 software uses this LXT972A Ethernet PHY status register to read its current status — that is the speed, duplex, and auto-negotiate setting of the PHY at any given time. Because the LXT973 Ethernet Transceiver does *not* support this register, it will return invalid values for the PHY status and, consequently, the Ethernet driver will not function correctly.

For status register listings and comparisons, see "Register Differences Between the PHYs" on page 15. For software-modification recommendations, see "Recommended Software Changes" on page 17.

3.2 Newer PHY's Software-Affecting Errata

Two issues — given in *Intel® LXT973 10/100 Mbps Dual Port Fast Ethernet PHY Specification Update* (249737) — can interfere with the LXT973 Ethernet Transceiver's operation with the Ethernet access component of the IXP400 software.

- Reads of odd registers may randomly return the value of the previous even register.

  This occurs in LXT973 Ethernet Transceiver Version A2 and older, but is fixed in Version A3. The Ethernet access component of the IXP400 software depends on the ability to correctly read some of the odd registers.

  To ensure correct register reads, a software work around must be implemented.

- Incorrect usage of internal clocks in the 10-Mbps, internal-loop-back mode.

  The Port Configuration Register 16, TP Loopback Bit must be cleared manually — according to the connection speed and duplex mode. If not, there may be excessive collisions on the line.

For a status register listings and comparison, see "Register Differences Between the PHYs" on page 15. For software-modification recommendations, see "Recommended Software Changes" on page 17.

3.3 Intel® IXP400 Software, Beyond v.1.2.1

Starting with IXP400 software v.1.2.2, MII access is moved from ixEthAccMii.c into a separate, access-component-independent file (ixEthMii.c) and non-validated support for the LXT973 Ethernet Transceiver PHY is added.

The software will now recognize the attached PHY and work with either type. MII functionality is retained in ixEthAccMii, for backwards compatibility.

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Appendix A Register Differences Between the PHYs

While the IEEE-defined MII register set is implemented in the same way in both PHYs, there are differences in the vendor specific register set. These are shown in Table 2.

Table 2. MII Register Definitions

Reg.	MII Specification	LXT972A Ethernet PHY	LXT973 Ethernet Transceiver
0	Control Register	Implemented	Implemented
1	Status Register	Implemented	Implemented
2	PHY Identifier 1 Register	Implemented	Implemented
3	PHY Identifier 2 Register	Implemented	Implemented
4	Auto-negotiation Advertisement Register	Implemented	Implemented
5	Auto-negotiation Link Partner Ability Register	Implemented	Implemented
6	Auto-Negotiation Expansion	Implemented	Implemented
7	Auto-Negotiation Next Page Transmit	Implemented	Implemented
8	Auto-Negotiation Link Partner Received Next Page	Implemented	Implemented

Table 3. Vendor-Specific Register Definitions and Comparisons

Reg.	LXT972A Ethernet PHY	LXT973 Ethernet Transceiver	Notes
9-15	Not used / Reserved	Not used / Reserved	
16	Port Configuration Register	Port Configuration Register	
17	Status Register 2	Not used	The Intel® IXP400 Software's Ethernet drivers — up to version 1.2.1 — always use this register to read link state, speed, duplex, and auto-negotiate settings
18	Interrupt Enable Register	Reserved	Not used in the IXP400 software
19	Interrupt Status Register	Not used	Not used in the IXP400 software
20	LED configuration Register	Not used	Not used in the IXP400 software
21-29	Not used / Reserved	Not used / Reserved	
30	Transmit Control register	Reserved	Not used in reference design or in the IXP400 software
31	Not used	Reserved	

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Appendix B Recommended Software Changes

This appendix gives an example of basic software changes that can be made in order for the LXT973 Ethernet Transceiver to work with Intel® IXP42X product line and IXC1100 control plane processors.

On the Wind River* Tornado* development platform for Windows* — when IXP400 software up to v.1.2.1 is installed — the software's Ethernet-access software is, by default, stored in:

```
\Tornado\ixp425_xscale_sw\src\ethAcc
```

In the MontaVista* Linux* v.2.1 environment, the Ethernet-access software it is stored in:

```
<working dir>/ixp425_xscale_sw/src/ethAcc>
```

B.1 General Recommendations

An effective way to begin is to add some code that identifies the attached PHY and its version. For this purpose, PHY identification register 1 (address 2) and PHY identification register 2 (address 3) are provided.

- Register 1 and the least-significant 6 bits of register 2 comprise the OUI, which in this case will always be the OUI of Intel, `0x00207B`.
- The next 6 bits indicate the part number"
  - — LXT973 Ethernet Transceiver – `100001`
  - — Intel® LXT971A Fast Ethernet Transceiver — `001110`
  - — LXT972A Ethernet PHY — `011110`
- The remaining four bits indicate the PHY revision level
  - — LXT973 Ethernet Transceiver, A2 silicon— `0000`
  - — LXT973 Ethernet Transceiver, A3 silicon — `0001`

B.2 Replacing Status Register 2

The Ethernet access component uses the Booleans `speed100`, `fullDuplex`, and `autoneg` for PHY status. They are read from Status Register 2 in the functions `ixEthAccMiiShow` and `ixEthAccMiiLinkStatus` in `IxEthAccMii.c`.

For the LXT973 Ethernet Transceiver add code that — providing the link is up — does the following:

- Determines the `autoneg` state from a combination of Control Register 0.12, Status Register 1.3 and Status Register 1.5
- If `autoneg` is true, determines `speed100` and `fullDuplex` from a combination of Status Register 1.[11:14], Auto-Negotiating Advertisement Register 4.[5:8] and Auto-Negotiating Link Partner Ability Register 5 [5:8].
- If `autoneg` is false, determines `speed100` from Control Register 0.13 and `fullDuplex` from Control Register 0.8.

B.3 Resolving MDIO Errors in Earlier Device Versions

If the LXT973 Ethernet Transceiver revision level is `0000` (version A2 or older), all odd-numbered registers must be read multiple times and the return values compared, as they may randomly return the value of the previous even register.

B.4 Resolving Internal Loop-Back Receive Errata

If `fullDuplex` and `speed100` are both false (10-Mbit, half-duplex), Port Configuration Register 16.8 (TP Loopback) must be manually cleared to `0`.