



Enabling DDR2 16-Bit Mode on Intel® IXP43X Product Line of Network Processors

Application Note

May 2008



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or by visiting [Intel's Web Site](#).

Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See http://www.intel.com/products/processor_number for details.

BunnyPeople, Celeron, Celeron Inside, Centrino, Centrino logo, Core Inside, FlashFile, i960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel Core, Intel Inside, Intel Inside logo, Intel. Leap ahead., Intel. Leap ahead. logo, Intel NetBurst, Intel NetMerge, Intel NetStructure, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel Viiv, Intel vPro, Intel XScale, Itanium, Itanium Inside, MCS, MMX, Oplus, OverDrive, PDCharm, Pentium, Pentium Inside, skool, Sound Mark, The Journey Inside, VTune, Xeon, and Xeon Inside are trademarks of Intel Corporation in the U.S. and other countries.

*Other names and brands may be claimed as the property of others.

Copyright © 2008, Intel Corporation. All rights reserved.



Contents

1.0	Introduction	5
1.1	Purpose	5
1.2	Intended Audience	5
1.3	Related Documents	5
2.0	Hardware Configuration and Registers Setting example	6
3.0	Software Enabling	7

Figures

No Figures Used At This Time.

Tables

1	Supported DDRII 16-bit SDRAM Configurations	6
2	Programming codes for DDR-I/II SDRAM Bank Size	6



Revision History

Date	Revision	Description
May 2008	001	Initial release.

§ §



1.0 Introduction

The DDR-I/II SDRAM interface provides a direct connection to a reliable, high bandwidth memory subsystem. The DDR-I/II SDRAM interface consists of a 16-bit/32-bit wide data path to support up to 1.6 GBytes/sec throughput. The Error Correction Code (ECC) for 16-bit wide interface is not supported. The memory controller supports maximum of 64Mbytes of 16-bit DDR-II SDRAM (support 512Mbit technology).

1.1 Purpose

The objective of this application note is to provide reference on configuring the DDR-II to 16-bit mode. The suggestion provided here has been validated on Intel(R) IXDP435 Multi-Service Residential Gateway Reference Platform.

1.2 Intended Audience

This application note is targeted for those who intend to use DDR-II in 16-bit mode, single chip 512Mbit SDRAM device.

1.3 Related Documents

Document Title	Document Number
<i>Intel® IXP43X Product Line of Network Processors Developer's Manual</i>	316843



2.0 Hardware Configuration and Registers Setting example

Table 1 shows the support DDR-II SDRAM configuration.

Table 1. Supported DDRII 16-bit SDRAM Configurations

DDR SDRAM Technology	DDR SDRAM Arrangement	# Banks	Address Size		Leaf Select		Total Memory Size	Page Size
			Row	Column	DDR_BA[1]	DDR_BA[0]		
256 Mbit	16M x16	1	13	9	ADDR[24]	ADDR[23]	32MB	1KB
512 Mbit	32M x16	1	13	10	ADDR[25]	ADDR[24]	64MB	1KB

Example for programming the DDR-I/II SDRAM memory space to Bank 0 = 64 Mbyte and Bank 1 un-populated. The memory is configured to 16-bit mode, so there is no special 32-bit region using S32SR register. The registers can be programmed as follows. Refer to Table 2 for SDRAM bank size.

- Bank 0 Size = 64MB, code = 0000004₂.
- Bank 1 Size = empty, code = 0000000₂
- SDBR = 0000 0000H, SDBR[30:24] = 0000000₂
- SBR0[7:0] = 000000100₂ = 04H (size of Bank 0)
- SBR1[7:0] = 000000100₂ = 04H (size of Bank 0 + size of Bank 1)

Table 2. Programming codes for DDR-I/II SDRAM Bank Size

Bank Size	Code	Bank Size	Code
Empty	00H	128 Mbyte	08H
16 Mbyte	01H	256 Mbyte	10H
32 Mbyte	02H	512 Mbyte	20H
64 Mbyte	04H	1 Gbyte	40H

The following registers must be programmed before using the DDR:

- [DDR SDRAM Control Register 0 SDCR0](#) - Program according JEDEC specs.
- [DDR SDRAM Control Register 1 SDCR1](#) - Program according JEDEC specs.
- Perform DDR initialization sequence using [DDR SDRAM Initialization Register SDIR](#) register.
- [Refresh Frequency Register RFR](#) - Program per JEDEC Spec using MCU clock of 133 or 200MHz

Note: Please refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.



3.0 Software Enabling

Here are the changes required in the Bootloader - Redboot* v2.04 to enable DDR2 16 bit mode for the Intel(R) IXPDP435 Multi-Service Residential Gateway.

1. Changes required in the file
packages/hal/arm/xscale/kixrp435/current/include/kixrp435.h.
#define SDRAM_SIZE 0x04000000 // 64MB.
#define KIXRP435_SDCR0_INIT (0x7222231a) // 16-bit mode.
#define KIXRP435_SBR0_INIT (0x00000002) //13 bits row address size and
10 bits column address size for bank 0.
#define KIXRP435_SBR1_INIT (0x00000002) //13 bits row address size and
10 bits column address size for bank 1.
2. Changes required in the following file
packages\hal\arm\xscale\kixrp435\current\include\pkgconf\mlt_arm_xscale_kirxp435_.h*. Change the macro for SDRAM size change:
#define CYGMEM_REGION_ram_SIZE (0x04000000).
#define CYGMEM_SECTION_heap1_SIZE (0x04000000 - (size_t)
CYG_LABEL_NAME (__heap1)).
3. Change required in file
packages\hal\arm\xscale\kixrp435\current\include\pkgconf\mlt_arm_xscale_kirxp435.ldi*. Change the LENGTH value for SDRAM size change:
LENGTH = 0x04000000
4. Change the following file
packages\hal\arm\xscale\kixrp435\current\include\pkgconf\mlt_arm_xscale_kirxp435_.mlt*). Change the region ram:
region ram 0 4000000 0 !
5. Change the following files:
packages\hal\arm\xscale\kixrp435\current\misc.ecm*.
This is to make sure that Linux * zImage is executed at a valid memory range
which is smaller than 0x4000000.
"CYGHWR_REDBOOT_ARM_LINUX_EXEC_ADDRESS_DEFAULT" value from
0x6000000 to 0x1800000.
6. Rebuild the RedBoot* following the procedures in Intel IXP400 Software:
RedBoot*v2.04 Software Release note at:
http://www.intel.com/design/network/products/npfamily/download_ixp400.htm.



Enabling DDR2 16-Bit Mode on Intel® IXP43X Product Line of Network Processors
-Application Note