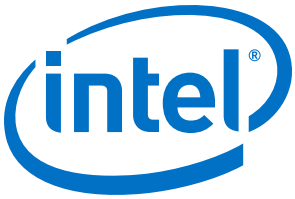

Ethernet Link Inspector User Guide v1.1 for Intel® Stratix® 10 Devices

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1. Overview of the Ethernet Link Inspector for Intel® Stratix® 10 Devices

This user guide describes the Ethernet Link Inspector for Intel® Stratix® 10 devices.

The Ethernet Link Inspector is a inspection tool that can continuously monitor the status and traffic of an Ethernet IP link. If needed, the Ethernet Link Inspector can capture an event with the help of Signal Tap Logic Analyzer to further examine the link behavior during Auto Negotiation (AN), Link Training (LT), or any other event during the link operation. The Ethernet Link Inspector also creates a graphical user interface (GUI) to represent the link behavior.

1.1. Features

The Ethernet Link Inspector consists of two modules:

- Link Monitor
- Link Analysis

The following sections describe in detail the function of each module.

1.1.1. Link Monitor

The link monitor performs real-time status monitoring of an Ethernet IP link.

It continuously reads and displays all of the required status registers related to the Ethernet IP link. The Link Monitor helps to ensure that all of the Ethernet IP link status at various stages are valid. In case of any failure, it narrows down to the type of failure based on the various status bits, which are based in the register bank of an Ethernet IP core. For more information on the register map, refer to respective Ethernet IP user guide.

Examples of the Ethernet link status displayed on the Link Monitor user interface include:

- State of Ethernet IP link (Up or Down)
- State of AN and LT process (Active or Done)
- Number of correct frames received
- Number of frame errors
- Transmitted and recovered clock frequencies etc.

Because the Link Monitor gives out real time link status through Ethernet IP registers, it needs to have a connection with the device that is powered on and configured with the appropriate design file.

1.1.2. Link Analysis

The Link Analysis displays a sequence of events on an Ethernet IP link, which occured in a finite duration of time.

The Link Analysis relies on Signal Tap Logic Analyzer to capture and store database of all required signals. Once the Signal Tap Logic Analyzer creates a database, the Link Analysis performs an analysis on the database to extract all the required information and displays them in a user-friendly graphical user interface (GUI).

The features of the Link Analysis include:

- Ability to capture and display events that occur during Ethernet IP link bring-up. For example, Auto Negotiation and Link Training.
- Ability to capture the link behavior at an intended trigger point and analyze link behavior around that time period.

The Signal Tap Logic Analyzer can store Signal Tap data in a Comma-Separated Value File (`.csv`) format. You must manually configure and capture the Signal Tap data and export the database for use with the Link Analysis. Once the database is generated and stored, import the database through Link Analysis for further processing.

To export a Signal Tap data from Signal Tap Logic Analyzer:

1. Using the Signal Tap Logic Analyzer, select **Files ➤ Export** to export the captured data.
2. Specify the **File Name**, **Directory**, and **Export Format** (in `.csv` file format).
3. Click **OK** to generate the `.csv` database of the captured data.

Related Information

Debug Tools User Guide: Intel Quartus® Prime Pro Edition
More information on Signal Tap Logic Analyzer in Intel Quartus® Prime Pro Edition software.

1.2. Supported IP Cores and Devices

Table 1. Ethernet Link Inspector Supported IP Cores for Intel Stratix 10 Devices

Device	IP Core	Data Rate (Gbps)	IP Type	Auto Negotiation and Link Training (1)	FEC (1)	Link Monitor (2)	Link Analysis (3)
Intel Stratix 10 L-Tile	10GBASE-KR PHY Intel Stratix 10 FPGA IP	10	Soft	Yes	No	Yes	Yes
	Low Latency 40G Ethernet Intel FPGA IP	40	Soft	Yes	No	Yes	Yes
	Low Latency 100G Ethernet Intel FPGA IP	100	Soft	No	No	Yes	No
Intel Stratix 10 H-Tile	10GBASE-KR PHY Intel Stratix 10 FPGA IP	10	Soft	Yes	No	Yes	Yes
	Low Latency 40G Ethernet Intel FPGA IP	40	Soft	Yes	No	Yes	Yes
	Low Latency 100G Ethernet Intel FPGA IP	100	Soft	No	No	Yes	No

(1) Feature details here shows the IP features supported by the Ethernet Link Inspector and not what the IP supports by itself.

(2) Supported in Intel Quartus® Prime software version 17.1 and earlier.

(3) Supported in Intel Quartus Prime software version 17.0 and later.

2. Setting Up the Ethernet Link Inspector for Intel Stratix 10 Devices

2.1. System Requirements and Prerequisites

2.1.1. System Requirements

To run the Ethernet Link Inspector for Intel Stratix 10 devices, your system must meet the following hardware and software requirements:

- Windows PC or Linux workstation
- Intel Quartus Prime Pro Edition software

2.1.2. Enabling Your Design For the Link Monitor

To enable the use of Link Monitor, your design must instantiate JTAG to Avalon® Master Bridge. Refer to the design examples of the Intel Stratix 10 Ethernet IP cores for guidance on how to define the JTAG to Avalon Master Bridge in your design.

Related Information

- Intel Stratix 10 10GBASE-KR PHY IP Core User Guide
  Design example to demonstrate the 10GBASE-KR PHY Intel Stratix 10 FPGA IP core using Intel Stratix 10 PHY.
- Stratix 10 Low Latency 40G Ethernet Design Example User Guide
- Stratix 10 Low Latency 100G Ethernet Design Example User Guide

2.2. Download and Run the Ethernet Link Inspector for Intel Stratix 10 Devices

The Link Monitor and Link Analysis of the Ethernet Link Inspector can be used independently for inspecting ethernet links of the supported IP cores.

To download the Ethernet Link Inspector, follow these steps:

1. Download the `Ethernet_Link_Inspector_v1p1.zip` file for the Ethernet Link Inspector.
2. Open the `Ethernet_Link_Inspector_v1p1.zip` and extract all the script files to a new directory.
3. In the Intel Quartus Prime Pro Edition software, select **Tools ➤ System Debugging Tools ➤ System Console** to launch the system console.
4. Type `cd Ethernet_Link_Inspector` to change directory to `Ethernet_Link_Inspector_v1p1/Ethernet_Link_Inspector`.

You can now run any of the predefined inspection modules (Link Monitor or Link Analysis) of the Ethernet Link Inspector from the System Console.

Running the Link Monitor

Perform the following steps to launch the Link Monitor module.

1. Type the following command in the Tcl Console window:

   For 10G Intel FPGA IP core:

   ```
   source main_LM_S10_10g.tcl
   ```

   For 40G Intel FPGA IP core:

   ```
   source main_LM_S10_40g.tcl
   ```

   For 100G Intel FPGA IP core:

   ```
   source main_LM_S10_100g.tcl
   ```

You can now run the Link Monitor module from the Ethernet Link Monitor toolkit.

Running the Link Analysis

Perform the following steps to launch the Link Analysis module.

1. Type the following command in the Tcl Console window :

   ```
   source link_analysis/main_LA_S10.tcl
   ```

2. To access the Link Analysis, use one of the following methods:
   - User interface
   - Command interface

   In the user interface, the link behavior is represented in a graphical user interface (GUI). In the command line, the link behavior is saved in a report file with `.csv` extension. Run the following command in the System Console to open the Link Analysis in either the user interface or command line:

   `main_LA_S10` *<arg1> <arg2> <arg3> <arg4>*

   Examples:

   a. User interface:

      ```
      main_LA_S10 1 "" "" ""
      ```

   b. Command line:

      ```
      main_LA_S10  0  E:/script/STP_database.csv reportname 10GBase-KR
      ```

Table 2. Command Parameters

Parameters	Description
<arg1>	• '1': User Interface • '0': Command Line
<arg2>	• "": NULL argument for user interface. • <input .csv database>: Name of input .csv database for command line. *Note:* Include the entire directory for input database, including with extension (.csv)
<arg3>	• "": NULL argument for user interface • <output .csv report>: Name of output .csv report for command line. *Note:* Do not include the extension (.csv) for output report.
<arg4>	• "": NULL argument for user interface • <Target IP name>: 10GBase-KR/40GBase-KR4 for command line

3. If you choose to open the Link Analysis in the user interface, a new tab appears, containing the Link Analysis module.
   a. Select the target IP core from the drop-down box.
   b. Click the **Select .csv file** button to import the Signal Tap database (.csv) file. In the Status Bar, make sure the directory to the imported database is correct.
   c. Click the **Start Analysis** button.

   Note: If you want the summary of the Ethernet link capture without using the Link Analysis, enter a report name and click **Generate Report** button to create a report (.csv) file.

You can now use the Link Analysis to analyze the Signal Tap database.

3. Functional Description

This section describes the various parts of the Ethernet Link Inspector user interface and how each part represents the device behavior. The Ethernet Link Inspector consists of two inspection modules: Link Monitor and Link Analysis.

3.1. Link Monitor Module

3.1.1. Link Monitor Tabs and Settings

The Link Monitor module of the Ethernet Link Inspector has three tabs. Each tab implements various Control and Status Registers (CSR) of the selected Ethernet IP core. There is also a Continuous Read All Registers option, which continuously polls the status of all the tabs.

Table 3. Ethernet Link Monitor Toolkit GUI Tabs

Tab	Description
MAC & PHY	Reset the IP core, read the MAC configuration and check the high level PHY status. • Resets: Implements the RESET register 0x310 PHY_CONFIG. • MAC Status: Shows status of TX MAC registers from 0x405 to 0x40A, and RX MAC registers from 0x506 to 0x50A. • PHY Status: Shows status PHY registers from 0x310 to 0x342.
Statistics Counters	Displays registers which characterizes TX and RX traffic.
KR/KR4	Displays the Intel Stratix 10 KR/KR4 registers.

Figure 1. MAC & PHY Tab

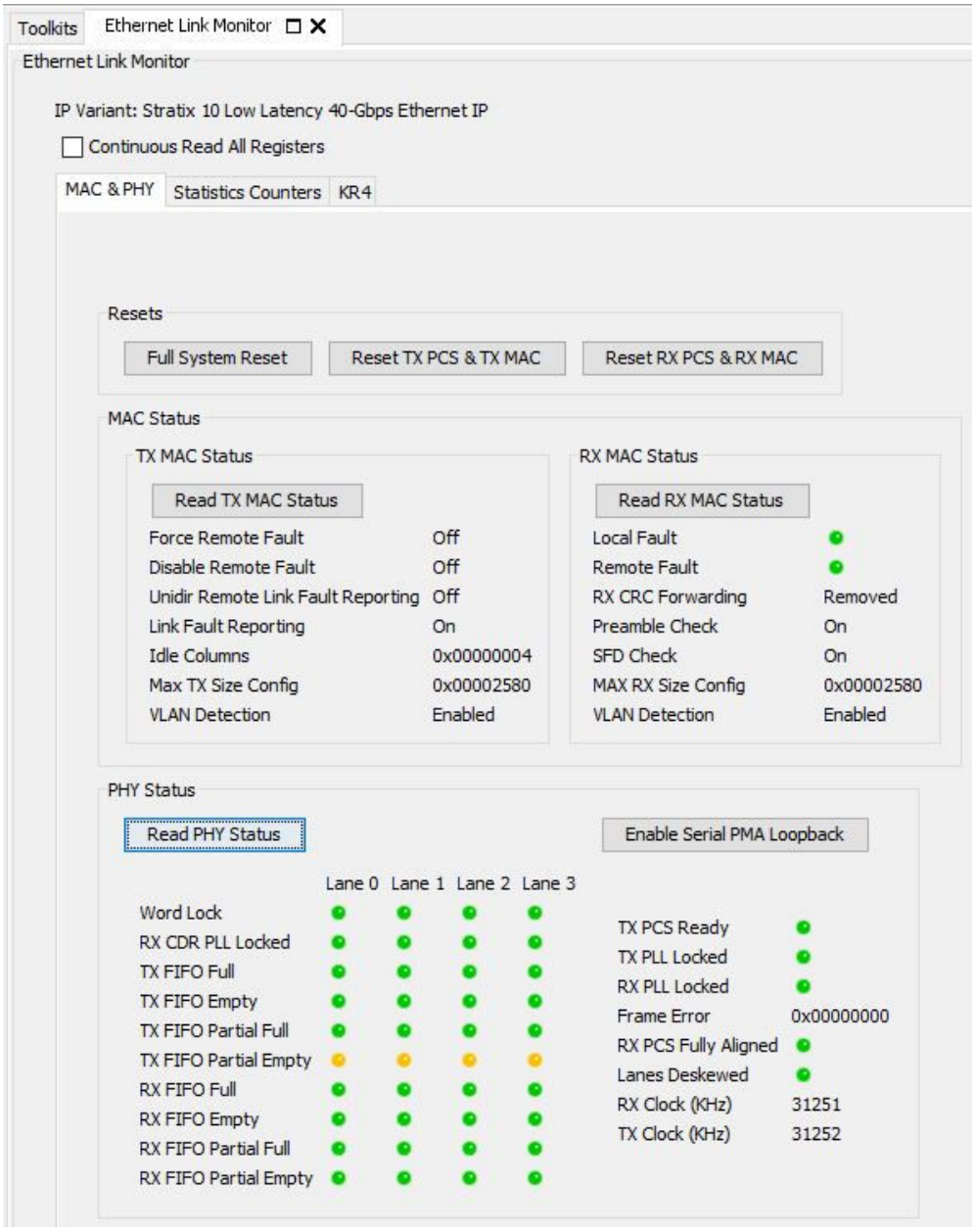


Figure 2. Statistics Counters Tab

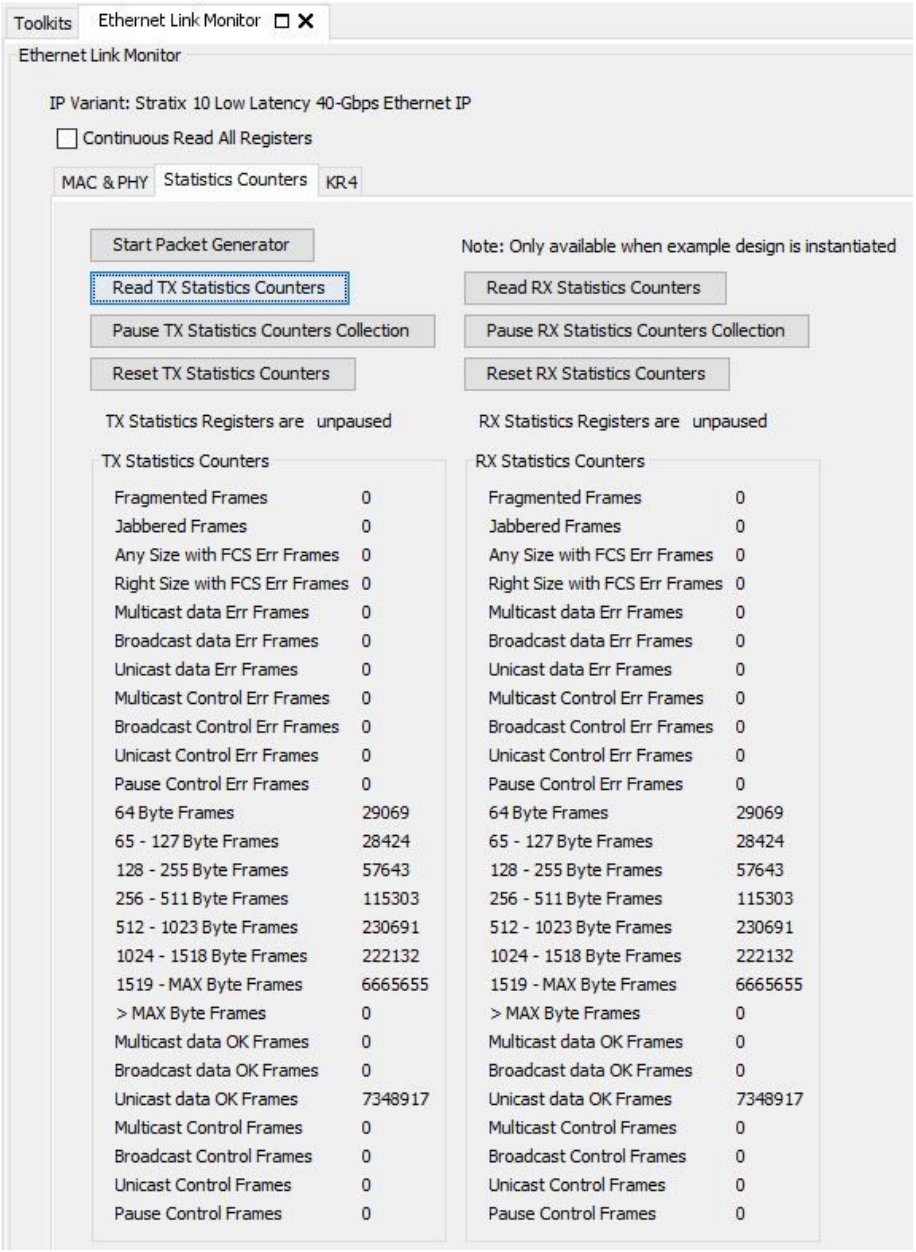


Figure 3. KR4 Tab

Table 4. Ethernet IP Core Support for Ethernet Link Monitor Toolkit GUI Tabs

Tab	Ethernet IP Core		
	10GBASE-KR PHY Intel Stratix 10 FPGA IP	Low Latency 40G Ethernet Intel FPGA IP	Low Latency 100G Ethernet Intel FPGA IP
MAC & PHY	No	Yes	Yes
Statistics Counters	No	Yes	Yes
KR4	Yes	Yes	No

3.2. Link Analysis Module

Link Analysis module of the Ethernet Link Inspector plots the behavior of an Ethernet IP link based on specific signals captured from Signal Tap Logic Analyzer.

When an Ethernet IP core is configured in a 10GBASE-KR or 40GBASE-KR4 configuration, the local device can be in either one of the following four operational modes starting from power-up to the device operation of the IP core:

1. Sequencer Initialize mode (SEQ_Initialize)
2. Auto Negotiation mode (Auto_Neg)
3. Link Training mode (Link_Training)
4. Data mode (Data)

The local device implements various internal states as part of the Sequencer State Machine to represent the four modes above. The local device may use one or more of the internal states to represent any one of the above mode. Refer to Sequencer State Machine on page 13 for more details.

3.2.1. Sequencer State Machine

The 10GBASE-KR PHY Intel Stratix 10 FPGA IP and Low Latency 40G Ethernet Intel FPGA IP cores for Intel Stratix 10 devices implement an internal state machine called Sequencer State Machine (SSM) that represents the Ethernet IP link bring-up. At any point of time, the device should be in one of SSM states.

Figure 4. Flowchart of SSM States

This figure shows the various states of SSM and how these states are mapped to the operational modes.

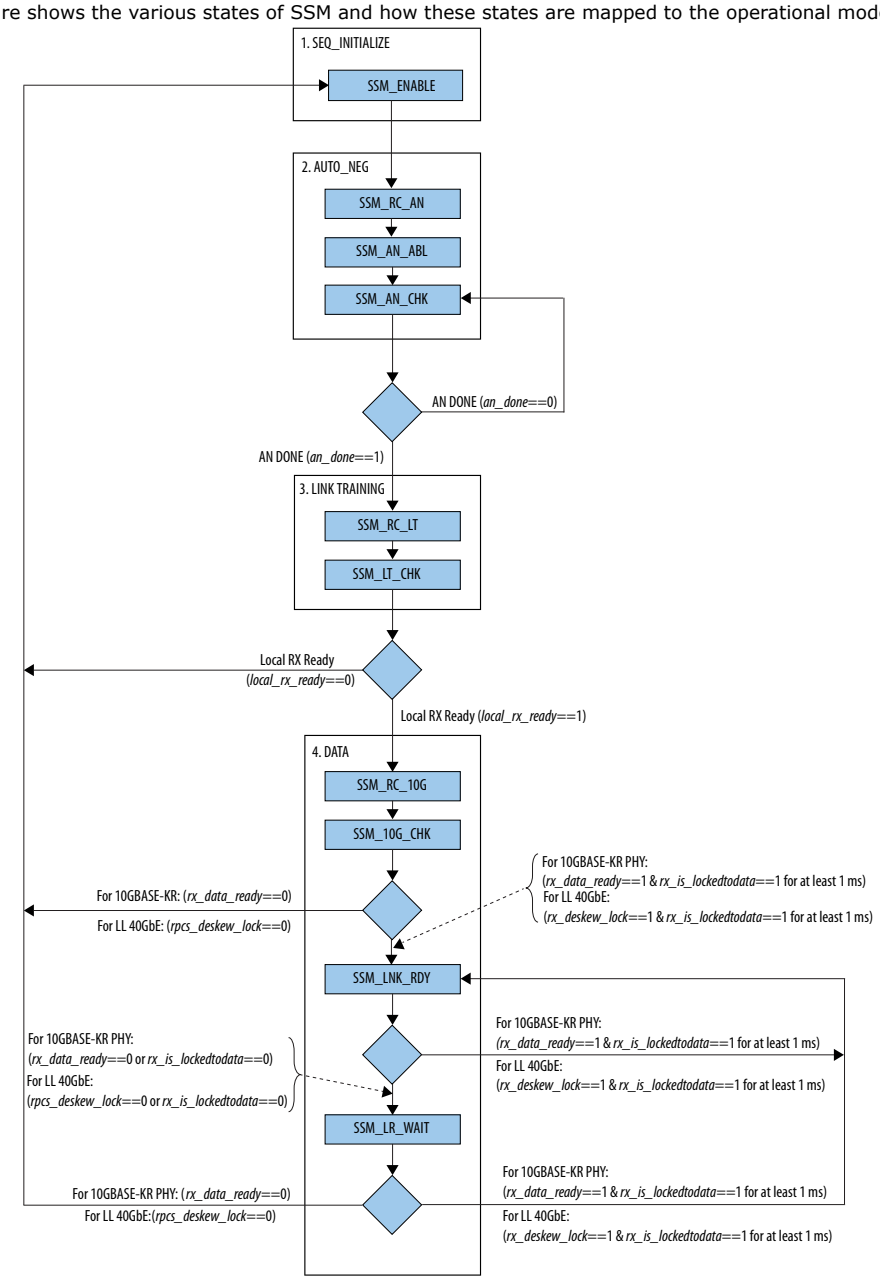


Table 5. SSM State Descriptions

SSM State	Description
SSM_ENABLE	The first state used for Sequencer State Machine (SSM) initialization. This should be the first state of device after a power cycle or a reset. If Auto Negotiation (AN) and Link Training (LT) are enabled, the local device moves to the SSM_RC_AN state after this state is completes.
SSM_RC_AN	Indicates the reconfiguration of PHY for Auto Negotiation operation.
SSM_AN_ABL	After the completion of SSM_RC_AN state, the local device goes into the SSM_AN_ABL state. In this state, the transmitter of the local device is disabled (i.e., no transitions) so that the Ethernet IP link goes down and the Ethernet IP link partner also goes back to Auto Negotiation. Even without any Ethernet IP link partners connected, the local device should complete this state and move to the next state i.e., SSM_AN_CHK. The local device spends an approximate time of 60 to 75 miliseconds (ms) in this state. At the end of this state, the local device starts sending AN Base Page to the remote device
SSM_AN_CHK	Once the local device start sending AN base page, it moves to the state SSM_AN_CHK. The rest of the AN happens in this state. The following are some major AN events that happen in this state: 1. Waiting for AN base Page from Remote Device 2. Waiting for an ACK from Remote Device 3. Sending an ACK to Remote Device 4. Doing NEXT PAGE communication (if any) 5. Asserting the an_done signal Various events during AN are further categorized into a separate state machine called AN Arbiter State Machine. Refer to Auto Neg Tab on page 17 for more details.
SSM_RC_LT	Indicates the reconfiguration of PHY for LT operation.
SSM_LT_CHK	After completion of SSM_RC_LT, device goes into SSM_LT_CHK state. This state includes the LT packet communication between the two devices, local and remote. At the end of this state, both devices should have completed LT and acknowledge each other upon completion.
SSM_RC_10G	Indicates that the reconfiguration of PHY for: • 10G/10GFEC mode for 10GBASE-KR operation. • 40G/40GFEC mode for 40GBASE-KR4 operation.
SSM_10G_CHK	After the completion of the SSM_RC_10G state, the local device goes into the SSM_10G_CHK state. In this state, the local device tries to achieve lock on the received Ethernet packets. The following status signals shows the lock status: 1. 10GBASE-KR PHY Intel Stratix 10 FPGA IP core: `rx_data_ready` 2. For Low Latency 40G Intel FPGA IP core: `rpcs_deskew_lock` The local device will move to the next state called SSM_LNK_RD when the following two lock conditions are met: 1. Achieve lock on the received Ethernet packet. The following signal should be asserted high: a. For 10GBASE-KR PHY Intel Stratix 10 FPGA IP core: `rx_data_ready` b. For Low Latency 40G Intel FPGA IP core: `rpcs_deskew_locked` 2. The clock data recovery (CDR) circuit should lock to received data (`rx_is_lockedtodata`) for at least 1 ms.

continued...

SSM State	Description
	The local device can only remain in this state if the total time, starting from SSM_RC_LT, does not exceed 500 ms. If the total time exceeds 500 ms and the two lock conditions are still not met, the local device goes back to SSM_ENABLE state and redo the AN and LT.
SSM_LNK_RDY	Indicates that the local device has successfully locked on to the received Ethernet packets and processed them accordingly. The local device is expected to be in this state during the entire exchange of Ethernet packets unless it losses lock (`rx_data_ready` or `rx_is_lockedtodata`). If the local device losses lock, it goes to the next SSM state called SSM_LR_WAIT.
SSM_LR_WAIT	The Ethernet IP link goes into SSM_LR_WAIT state if any of the following lock status signals goes low during SSM_LNK_RDY state: 1. For 10GBASE-KR PHY Intel Stratix 10 FPGA IP core: `rx_data_ready` or `rx_is_lockedtodata` 2. For Low Latency 40G Intel FPGA IP core: `rpcs_deskew_locked` or `rx_is_lockedtodata` For example, the local device waits for 1000 clock cycles (8 usec for 125 MHz clock) and checks if lock conditions are met again. If the lock conditions are met, the link goes back into SSM_LNK_RDY state. But if the lock conditions are not met during this time, the link goes into SSM_ENABLE state.

3.2.2. Link Analysis Tabs and Settings

The Link Analysis (LINK ANALYSIS1) module of the Ethernet Link Inspector has five tabs:

- Sequencer State Machine tab
- Auto Neg tab
- Link Training tab
- Data Mode tab
- Help tab

Note: The Link Analysis reads all the data that are being captured and stored by Signal Tap Logic Analyzer. To prevent processing error, it is important that you export and store the Signal Tap waveform database in `.csv` format, which contains a list of signals that the Link Analysis is expecting to receive. For the list of signals expected for a specific Ethernet IP core, refer to the document *S10_ethIP_ReferenceSignals* provided in the `Ethernet_Link_Inspector_v1p1.zip` file.

3.2.2.1. Sequencer State Machine Tab

The Sequencer State Machine (SSM) tab shows the flow of sequencer state machine states that the device goes through in the specific Signal Tap capture for the selected Ethernet IP core.

Figure 5. Example of Sequencer State Machine Tab GUI

Table 6. Sequencer State Machine Tab Parameters

Parameter	Description
Assumed Reference Timer Clock	Shows the assumed value of the clock frequency driving the reference timer. Ensure that the value of this clock is the same as the clock frequency configured in the Platform Designer window of the selected Ethernet IP core. *Note:* If the assumed value of the clock frequency does not match the clock frequency in Platform Designer window of the selected IP core, the timer values displayed in Link Analysis GUI will be incorrect. For example, the Timer values reported in Start, Stop and Delta columns in the Sequencer State machine tab would be incorrect.
States	Shows the flow of SSM states (from SEQ_Initialize to Data modes) that the device goes through in a specific capture. A successful state completion is highlighted in green whereas a state completion failure is highlighted in red.
Start	Timestamp for start time. Shows the reference timer value (in milisecond) corresponding to a specific state of SSM started.
Stop	Timestamp for stop time. Shows the reference timer value (in milisecond) corresponding to a specific state of SSM finished.
Delta	Timestamp for delta time. Shows the total time spent (in milisecond) on a specific state of SSM.

3.2.2.2. Auto Neg Tab

The Auto Neg tab may have one or more subtabs based on number of times the device goes into Auto Negotiation (AN) state during the Signal Tap capture in a finite amount of time. Each subtab displays the Ethernet IP link behavior during the occurrence of AN. Each AN occurrence is also prefixed with a number to distinguish between various AN occurrences.

Table 7. Local Device Status Signals

Name	Signal [4]	Indication	Description
Auto Negotiation (AN) Enable	`an_enable`	LED	• Green: Auto Negotiation is enabled. • Red: Auto Negotiation is disabled.
Auto Negotiation (AN) Done	`an_done`	LED	• Green: Auto Negotiation completed. This LED indication does not mean that the local device has finalized the common technology. Even in case of technology mismatch between the local and remote devices, `an_done` will be asserted. • Red: Auto Negotiation is not completed.
Local Auto Negotiation (AN) Technology	`lcl_tech`	Text	Displays the Auto Negotiation technology broadcasted by the local device.
Final Auto Negotiation (AN) Technology	`hcd_40g`, `hcd_kr`, `hcd_xaui`, `hcd_gige`	Text	• Displays the converged Auto Negotiation technology by the local device. • Shows the corresponding timestamp of technology convergence.

Table 8. Remote Device Status Signals

Name	Signal	Indication	Description
Remote Device Auto Negotiation Technology	`lp_tech`	Text	• Displays the Auto Negotiation technology broadcasted by the remote device. • Shows the timestamp when the local device receives this broadcasted technology.

AN Communication Packet

The AN Communication Packet section displays the AN packets exchanged between two devices. There are two parts to the AN Communication Packets section:

- AN Packets Received—shows the sequence of AN packets (from left to right) received from a remote device.
- AN Packets Sent—shows sequence of AN packets (from left to right) sent to a remote device.

(4) Actual signal names in the IP design file.

Figure 6. AN Communication Packet GUI

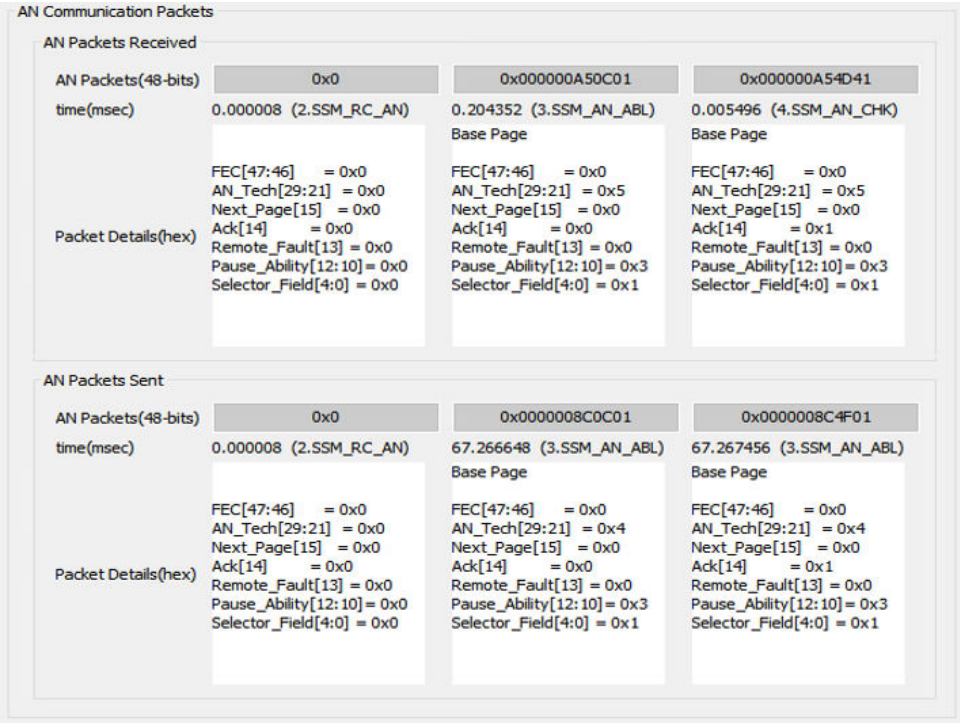


Table 9. AN Communication Packet GUI Parameters

Parameter	Description
AN Packets(48-bits)	Shows the Auto Negotiation packets exchanged between local and remote devices in hexadecimal format.
Time(msec)	Shows the SSM state in which AN packets are sent/received along with the timestamp with respect to reference timer
Packet Details(hex)	Shows the breakout for various bits in an AN packet and displays whether an AN packet in base page or next page. *Note:* The assumption for BASE PAGE or NEXT PAGE only holds true when AN states are captured from the actual start point of Auto Negotiation (i.e., start point of SSM_RC_AN). If the AN states are captured partially in Signal Tap Logic Analyzer, this assumption becomes unreliable.

AN Arbiter State Machine

The AN Arbiter State Machine section displays the AN Arbiter State Machine in the form of time domain waveforms. The AN arbiter state machine represents the entire Ethernet IP link behavior in the AN mode of operation.

Each waveform window represents a timescale for one Sequencer State Machine (SSM) state (i.e., SSM_RC_AN, SSM_AN_ABL or SSM_AN_CHK). The time scale of waveform windows, such as START and STOP time, should match the timestamp of the corresponding SSM state. The waveform windows are also tagged with specific SSM states, as shown in the following figure:

Figure 7. Time Domain Waveforms of the Sequencer State Machine States

Each AN Arbiter SM state is represented as an individual waveform. A logic 1 value on a state waveform at a particular timestamp signifies the current state of the device at that timestamp. Device can possibly be in only one state at a given point of time. To change the magnification level of the waveforms, click the left mouse button and drag the mouse cursor to the bottom right of the waveform windows to zoom in and drag the mouse cursor the top right of the waveform windows to zoom out.

Note: While zooming in and out, the waveform windows may be offset in the vertical scale. This may cause several waveform windows in a row to be misaligned for logic 0 and 1. To remove any misalignments and scale the Y axis of all waveform window to a common scale, click on the **Scale Waveforms (Y-axis)** button.

Figure 8. Flowchart of AN Arbiter State Machine

This figure shows a flow chart of the AN Arbiter State Machine and the conditions that drives the next state, based on the current state.

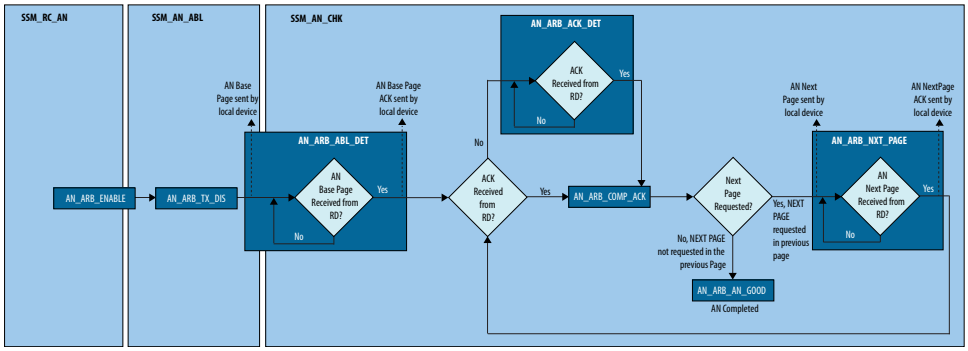


Table 10. AN Arbiter State Machine State and Signal Descriptions

Name	Indication	Description
AN_ARB_ENABLE	Waveform	This is the initial state of the AN Arbiter State Machine. This should be enabled (logic 1 value) during SSM_RC_AN state. This state ends after the start of SSM_AN_ABL and the local device moves to the next state i.e., AN_ARB_TX_DIS.
AN_ARB_TX_DIS	Waveform	In this state, the TX output of the local device is disabled for a finite amount of time to allow the remote device to start Auto Negotiation. This causes to link to go down. The duration of this state can be 60 to 75 ms. Device should always complete this state irrespective if there is a remote device available or not.
AN_ARB_ABL_DET	Waveform	In this state, the local device send out the AN Base Page and waits for the AN base page from the remote device. The local device goes into this state at the end of SSM_AN_ABL. The local device waits in this state until the AN Base page is received and the corresponding Acknowledgement (ACK) is sent out to the remote device. The local device moves to next state after sending ACK to the remote device. If the ACK is not received from the remote device at this time, the local device moves to AN_ARB_ACK_DET where it waits for ACK from the remote signal. Else, the local device moves to AN_ARB_COMP_ACK, which indicates the completion of ACK exchange between the two devices.
AN_ARB_ACK_DET	Waveform	In this state, the local device is waiting for ACK from the remote device.
AN_ARB_COMP_ACK	Waveform	When an acknowledgement is sent to as well as received from the remote device, the local device moves to this state called the Ack Complete state.
AN_ARB_AN_GOOD	Waveform	This state indicates that AN has succesfully completed on local device and is the final state of AN Arbiter State Machine.
AN_ARB_NXT_PAGE	Waveform	This state shows that the local device is sending NEXT page and waits for NEXT page from the remote device. This state remains until the local device send ACK to the remote device.

Table 11. AN Arbiter State Machine Signal Descriptions

Name	Indication	Description
an_enable	Waveform	Displays when AN is enable. This is waveform representation of the AN Enable signal described in Table 7 on page 17.
an_done	Waveform	Displays when AN is completed successfully. This is waveform representation of the AN Done signal described in Table 7 on page 17.

3.2.2.3. Link Training Tab

The Link Training Mode tab may have one or more subtabs based on number of times the device go into Link Training (LT) state during the Signal Tap capture in a finite amount of time. Each subtab displays the Ethernet link behavior during the occurrence of LT. Each LT occurrence is also prefixed with a number to distinguish between various LT occurrences.

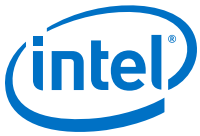


Table 12. Local Device Status Signals

Name	Signal [5]	Indication	Description
Link Training Enable	`lt_enable`	LED	• Green: LT is enabled. • Red: LT is disabled.
Frame Lock	`frame_lock`	LED	• Green: Detected and locked from receiving LT packets. Also shows the timestamp of lock. • Red: Not locked from receiving LT packets.
RX Trained	`rx_trained`	LED	• Green: LT completed. • Red: LT not completed.
Local RX Ready	`lcl_rx_ready`	LED	This signal is a delayed version of `rx_trained` signal. • Green: LT completed. • Red: LT not completed.
Link Training commands sent by Local Device	`rmt_coef_updl`, `rmt_coef_updh`	—	—
Init	—	Label	Indicates the total Initialize commands sent.
Preset	—	Label	Indicates the total Preset commands sent.
Main Incr	—	Label	Indicates the total main-tap increment commands sent.
Main Dec	—	Label	Indicates the total main-tap decrement commands sent.
Post-Tap Incr	—	Label	Indicates the total post-tap increment commands sent.
Post-Tap Dec	—	Label	Indicates the total post-tap decrement commands sent.
Pre-Tap Incr	—	Label	Indicates the total pre-tap increment commands sent.
Pre-Tap Dec	—	Label	Indicates the total pre-tap decrement commands sent.

Table 13. Remote Device Status Signals

Name	Signal [6]	Indication	Description
Remote RX Ready	`rmt_rx_ready`	LED	• Green: LT completed. • Red: LT not completed.
Link Training commands sent by Remote Device	`lcl_coefh`, `lcl_coefl`	—	—
Init	—	Label	Indicates the total Initialize commands sent.

continued...

(5) All the descriptions in Table 12 on page 21 are with reference to local device.

(6) All the descriptions in Table 13 on page 21 are with reference to remote device.

Name	Signal [6]	Indication	Description
Preset	—	Label	Indicates the total Preset commands sent.
Main Incr	—	Label	Indicates the total main-tap increment commands sent.
Main Dec	—	Label	Indicates the total main-tap decrement commands sent.
Post-Tap Incr	—	Label	Indicates the total post-tap increment commands sent.
Post-Tap Dec	—	Label	Indicates the total post-tap increment commands sent.
Pre-Tap Incr	—	Label	Indicates the total pre-tap increment commands sent.
Pre-Tap Dec	—	Label	Indicates the total pre-tap decrement commands sent.

Table 14. Data Mode Status Signals

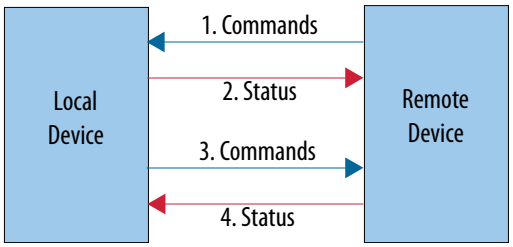
Signal	Indication	Description
`frame_lock`	Waveform	Displays the behavior of `frame_lock` in a time domain. When asserted, it indicates that the local device locked to LT packets. This is a waveform representation of the Frame Lock signal in the Table 12 on page 21.
`rx_trained`	Waveform	Displays the behavior of `rx_trained` in a time domain. When asserted, it indicates that the local device completed LT. This is a waveform representation of the RX Trained signal in the Table 12 on page 21.
`lcl_rx_ready`	Waveform	Displays the behavior of `lcl_rx_ready` in a time domain. When asserted, it indicates that the local device completed LT. This is a waveform representation of the Local RX Ready signal in the Table 12 on page 21.
`rmt_rx_ready`	Waveform	Displays the behavior of `rmt_rx_ready` in a time domain. When asserted, it indicates that the remote device completed LT. This is a waveform representation of the Remote RX Ready signal in the Table 13 on page 21.

LT Communication Packets

The LT Communication Packets section displays the LT packets exchanged between two devices. The LT Communication packets option has to be enabled to start plotting LT packets. A timestamp header is stored with each packet with respect to the reference timer. The transaction of the LT packet plotting may take a few minutes based on the number of packets that are being exchanged. To determine whether the plotting is completed or still in progress, monitor the status bar.

(6) All the descriptions in Table 13 on page 21 are with reference to remote device.

Figure 9. LT Communication Packet Exchange between Local Device and Remote Device



If the **LT Communication Packets** option is checked, the following subsections will be displayed on the tab-window of the Link Training:

1. Commands sent by Remote Device (signals: `lcl_coefh`, `lcl_coefl`)
2. Status to Remote Device (signals: `lcl_coef_sts`)
3. Commands sent by Local Device (signals: `rmt_coef_updl`, `rmt_coef_updh`)
4. Status to Local Device (signals: `rmt_coef_sts`)

For every command sent by the local or remote device, there is an equivalent status being sent back by the receiver end. The statuscorresponding to every command can be mapped by monitoring their time stamps, as shown in the following figure:

Figure 10. LT Training Sequence

This figure shows the timestamps corresponding to Command1 (C1) -> Status1 (S1) and Command2 (C2) -> Status2 (S2) represents the time taken by taken by either device to respond to the LT commands.

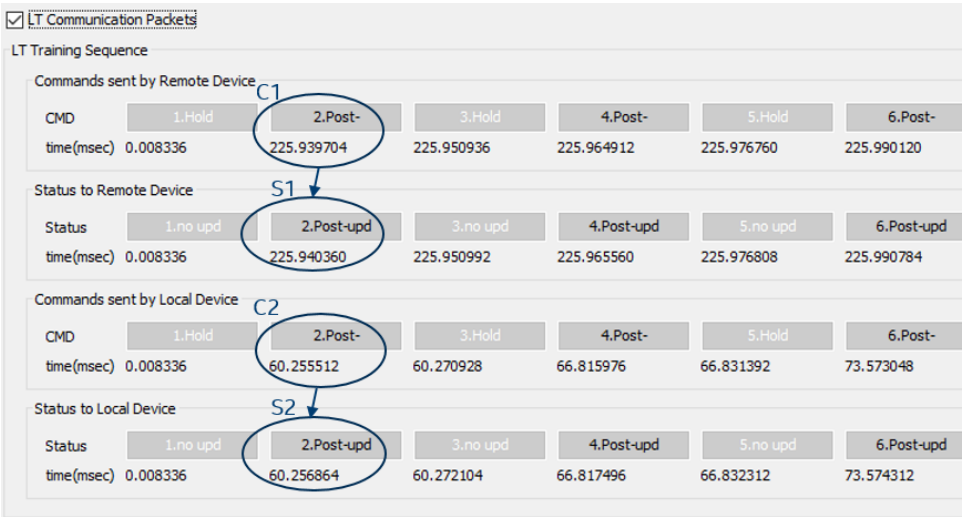


Table 15. Link Training Command Definitions

Command	Description
Post-	Decreases post-tap by 2 and increases main-tap by 1.
Post+	Increases post-tap by 2 and decreases main-tap by 1.
Main-	Decreases main-tap by 1.

continued...

Command	Description
Main+	Increases main-tap by 1.
Pre-	Decreases pre-tap by 2 and increases main-tap by 1
Pre+	Increases pre-tap by 2 and decreases main-tap by 1
Hold	Do not change any tap values.
Preset	Sets pre-tap and post-tap to zero and main-tap to maximum, as defined in Clause 72 of the IEEE 802.3 2015 Standard.
Initialize	Sets the coefficients back to initial (start) values configured in the IP core.

The following figure shows the direction in which the digital values of main-tap, post-tap, and pre-tap move based on commands. For more details on these values, refer to the *Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide*.

Figure 11. Direction of Main-Tap, Post-Tap, and Pre-Tap Based On Link Training Commands

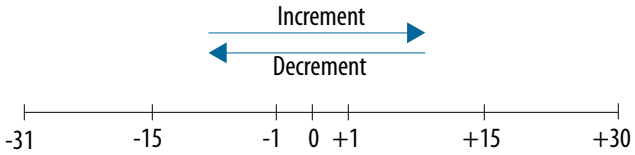


Table 16. Status Definitions

Status	Description
no upd	No taps updated.
Post-upd	Post-tap updated. This status is valid for both increment and decrement command
Post-max	Post-tap incremented and is at maximum value
Post-min	Post-tap decremented and is at minimum value
Pre-upd	Pre-tap updated. This status is valid for both increment and decrement command
Pre-max	Pre-tap incremented and is at maximum value.
Pre-min	Pre-tap decremented and is at minimum value.
Main-upd	Main-tap updated. This status is valid for both increment and decrement command.
Main-max	Main-tap incremented and is at maximum value.
Main-min	Main-tap decremented and is at minimum value.

Note: If the command or status shows "----", this indicates that the values in the LT packet are invalid.

Related Information

Intel Stratix 10 L- and H-Tile Transceiver PHY User Guide

3.2.2.4. Data Mode Tab

Data Mode tab may have one or more subtabs based on number of times the device go into Data Mode state during the Signal Tap capture in a finite amount of time. Each subtab displays the Ethernet IP link behavior during the occurrence of Data Mode. Each Data Mode occurrence is also prefixed with a number to distinguish between various Data Mode occurrences.

Table 17. Local Device Status Signals

Name	Signal	Indication	Description
For 10GBASE-KR mode:			
RX Block Lock	`rx_block_lock`	LED	• Green: Locked from receiving Ethernet packets. Also shows the timestamp of lock. • Red: Not locked from receiving Ethernet packets.
RX Data Ready	`rx_data_ready`	LED	• Green: Represents successful block lock assertion. Also shows the timestamp.an_done will be asserted. • Red: Block lock not asserted.
FEC	`pcs_mode_rc`	LED	• Green: Local device is using FEC. • Red: Local device is not using FEC.
For 40GBASE-KR mode:			
PCS Align Lock	`rpcs_align_locked`	LED	• Green: All 4 lanes are skew compensated and aligned. Also shows the timestamp of lock. • Red: Lanes are not skew compensated and not aligned.
PCS Deskew Lock	`rpcs_deskew_locked`	LED	• Green: All 4 lanes are locked for alignment marker. Also shows the timestamp of lock. • Red: Lanes are not locked for alignment marker.
FEC	`pcs_mode_rc`	LED	• Green: Local device is using FEC. • Red: Local device is not using FEC.
PCS Word Lock	`rpcs_word_locked`	LED	This signal is available per channel basis. There are four signals for 40GBase-KR.

continued...

Name	Signal	Indication	Description
			• Green: Locked from receiving Ethernet packets. • Red: Not locked from receiving Ethernet packets.
RX ENH Block Lock	rx_enh_blk_lock	LED	This signal is available per channel basis. There are four signals for 40GBase-KR. • Green: FEC is locked from receiving Ethernet packets. • Red: FEC is not locked from receiving Ethernet packets.

Table 18. Data Mode Status Signals

Signal	Indication	Description
For 10GBASE-KR mode:		
rx_block_lock	Waveform	Displays the behavior of rx_block_lock in time domain. When asserted, it indicates that the local device is locked from receiving Ethernet packets. This is a waveform representation of the RX Block Lock signal in the Table 17 on page 25.
rx_data_ready	Waveform	Displays the behavior of rx_data_ready in time domain. This represents a successful block lock assertion. This is a waveform representation of the RX Data Ready signal in the Table 17 on page 25.
rx_hi_ber	Waveform	Displays if the device receives invalid sync header for more than 16 times within 125 us time period, as defined in Clause 49 of the IEEE 802.3 2015 Standard.
For 40GBASE-KR mode:		
rpcs_align_locked	Waveform	Displays the behavior of rpcs_align_locked in time domain. When asserted, it indicates that all 4 lanes are skew compensated and aligned. This is a waveform representation of the PCS Align Lock signal in the Table 17 on page 25.
rpcs_deskew_locked	Waveform	Displays the behavior of rpcs_deskew_locked in time domain. When asserted, it indicates that all 4 lanes are locked to alignment markers. This is a waveform representation of the PCS Deskew Lock signal in the Table 17 on page 25.

continued...

Signal	Indication	Description
rx_hi_ber	Waveform	Displays if device receives invalid sync header for more than 16 times within 125 us time period, as defined in Clause 49 of the IEEE 802.3 2015 Standard.
rpcs_word_locked	Waveform	Displays the behavior of rpcs_word_locked in time domain. When asserted, it indicates that the local device is locked from receiving Ethernet packets. This is a waveform representation of the PCS Word Lock signal in the Table 17 on page 25.
rx_enh_blk_lock	Waveform	Displays the behavior of rx_enh_blk_lock in time domain. When asserted, it indicates that FEC is locked from receiving Ethernet packets. This is a waveform representation of the RX ENH Block Lock signal in the Table 17 on page 25.

Table 19. Device Intrinsic Signals

Signal	Indication	Description
rx_is_lockedtodata	Waveform	Shows if clock data recover (CDR) receiver of the Local Device is locked to the incoming data. This is different than rx_is_lockedtodata coming from CDR. This is asserted only when CDR is locked to data for 1 ms.
rx_is_lockedtoref	Waveform	Shows if CDR receiver of the Local Device is locked to a reference clock.
rx_digitalreset	Waveform	A logic 1 indicates the time duration for which rx_digitalreset is applied
rx_digitalreset_stat	Waveform	A logic 1 indicates the time duration for which rx_digitalreset took effect
rx_analogreset	Waveform	A logic 1 indicates the time duration for which rx_analogreset is applied
rx_analogreset_stat	Waveform	A logic 1 indicates the time duration for which rx_digitalreset took effect
tx_digitalreset	Waveform	A logic 1 indicates the time duration for which tx_digitalreset is applied
tx_digitalreset_stat	Waveform	A logic 1 indicates the time duration for which rx_digitalreset took effect
tx_analogreset	Waveform	A logic 1 indicates the time duration for which tx_analogreset is applied
tx_analogreset_stat	Waveform	A logic 1 indicates the time duration for which rx_digitalreset took effect

3.2.2.5. Help Tab

The Help tab provides basic guidelines on:

- Capturing Ethernet link bring-up sequence.
- General recommendations for Signal Tap Logic Analyzer configuration.

4. Document Revision History for Ethernet Link Inspector User Guide for Intel Stratix 10 Devices

Document Version	Ethernet Link Inspector Version	Changes
2018.07.04	1.1	Initial release.