Agenda

- Challenges with the current transceiver debug process
- Why do we need a transceiver debug tool?
- Components and features of the Transceiver Debug Tool
- Steps to run the Transceiver Debug Tool
Challenges with the Current Transceiver Debug Process

- Measure Transceiver Voltage
- Check Transceiver Channel Status
- Measure Eye Quality
Challenges with the Current Transceiver Debug Process

1. Measure Transceiver Voltage
   - Need an external measurement equipment
2. Check Transceiver Channel Status
   - Need an extra FPGA logic analyzer
3. Measure Eye Quality
   - Long test time

* For example, a Signal Tap logic analyzer
Why Do We Need a Transceiver Debug Tool?

- Fast Results
- Fully Automated
- Design or Protocol Agnostic
- Push-Button Results
- No Effect on Data Traffic
Components and Features of the Transceiver Debug Tool

- Transceiver Debug Tool
  - Transceiver Voltage Debug Tool
  - Transceiver Status Debug Tool
  - Transceiver Eye Debug Tool
## Components and Features of the Transceiver Debug Tool

| Transceiver Voltage Debug Tool | Measure VCCER at the data sampling node  
Measure VCCET at the transmitter node |
|--------------------------------|--------------------------------------------------------------------------------------|
| Transceiver Status Debug Tool | Show the following channel status:  
- Locked to data and locked to ref  
- Calibration, Avalon® Memory Mapped (Avalon-MM) busy, and serial loopback  
- Check the cable polarity swap |
| Transceiver Eye Debug Tool    | Measure the height or width of the eye at clock data recovery (CDR) sampling point |
Four Steps to Run the Transceiver Debug Tool

**Step 1:** Enable the Altera® Debug Master Endpoint (ADME) and compile the design

Native PHY Intellectual Property (IP)

PCle* IP

Ethernet IP

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Four Steps to Run the Transceiver Debug Tool

Step 2: Program the device.
Step 3: Load the design in the system console.
Step 4: Use “cd” to change the directory where you have saved the tools script file and source “S10_Ltile_Htile_Transceiver_Debug_Tool_V4p0.tcl”

Note: Refer to the backup slides for steps on how to program the device and load the sof file.
An Example of a Test Setup

Intel® Stratix® 10 H-Tile Signal Integrity Development Kit

- Number of Channels: 4
- Data Rate: 28 Gbps
- Connector: QSFP+
- Cable Length: 3 meters
- Design: Physical medium attachment (PMA) Direct
- RX Adaptation: Adaptive CTLE, VGA, All tap DFE
TRANSCEIVER VOLTAGE TOOL
PCB Trace Properties

PCB trace resistance can be calculated as

\[ R = \rho \frac{L}{A} \]

where:
- \( R \) is the resistance
- \( \rho \) is the resistivity
- \( L \) is the length of the trace
- \( A \) is the area

Voltage Drop

\[ V = IR \]
Intel® Stratix® 10 Signal Integrity (SI) Development Kit

Voltage regulators

HSSI Receiver Voltage

HSSI Transmitter Voltage
Sense Trace

Sense trace measures the voltage nearest to the device.
Problem Statement

- Sense trace does not sense the package IR drop
- Voltage drop from sense point to device is not measured
- Need an external analog-to-digital (ADC) to convert the sensed voltage
Solution

Intel® Stratix® 10
L-Tile/H-Tile Transceiver
Voltage Debug Tool

Measure the voltage internally

Measured voltage value accessed via the JTAG or System Console
Intel® Stratix® 10 L-Tile/H-Tile Transceiver Voltage Debug Tool Algorithm

1. Issue a command to connect the VCCET to the test bus.
2. Issue a command to connect the reference voltage to the test bus.

Loop:
3. Increment the reference voltage to match the VCCET.
4. Measure the output of the comparator.
5. Once the comparator output goes high, report the voltage value.
## Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Voltage Tool

### Measurement Type

<table>
<thead>
<tr>
<th>Device</th>
<th>Voltage 1</th>
<th>Voltage 2</th>
<th>Voltage 3</th>
<th>Voltage 4</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 1</td>
<td>1.1175V</td>
<td>1.1178V</td>
<td>1.1175V</td>
<td>1.1175V</td>
<td>Done</td>
</tr>
<tr>
<td>Device 2</td>
<td>1.1238V</td>
<td>1.1238V</td>
<td>1.1238V</td>
<td>1.1238V</td>
<td>Done</td>
</tr>
</tbody>
</table>

### Proceeding with Measurements
- Click **Measure Voltage Once** to initiate measurements.
- Click **Measure Voltage Once** again to stop the measurement.

### Additional Options
- **Continuous Update**: Check to enable continuous updates.
- **Stop the current measurement**: Stop the measurement if needed.

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## Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Voltage Tool

The tool automatically finds:

1. All the PHY instance
2. All the channels in the instantiated PHY instance
3. All connected cables (USB1 or USB2)

### Table: Voltage Measurements

<table>
<thead>
<tr>
<th>Channel</th>
<th>VCCER</th>
<th>VCCGT</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ch0</td>
<td>1.157V</td>
<td>1.157V</td>
<td>Done</td>
</tr>
<tr>
<td>Ch1</td>
<td>1.157V</td>
<td>1.157V</td>
<td>Done</td>
</tr>
<tr>
<td>Ch2</td>
<td>1.157V</td>
<td>1.157V</td>
<td>Done</td>
</tr>
<tr>
<td>Ch3</td>
<td>1.157V</td>
<td>1.157V</td>
<td>Done</td>
</tr>
</tbody>
</table>

---

To use this tool, the `Intel®` should be enabled.
Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Voltage Tool

- Measure the voltage once
- Continuously measure the voltage
- Stop the current measurement
Intel® Stratix® 10 Device Status Signal

- Transceiver (TX) Calibration Busy
- Counter Enable Pseudo-Random Binary Sequence (PRBS)
- Cable Swap Detect
- Receiver (RX) Serial Loopback
- RX Calibration Busy
- PRBS Done
- Locked to Data
- Locked to Ref

Intel® Stratix® 10 TX

PRBS Generator

Intel® Stratix® 10 RX

PRBS Checker
## Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Status Tool

The Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Status Tool is a graphical user interface (GUI) that provides real-time monitoring and control over the transceiver status in Stratix® 10 devices. This tool is essential for developers and engineers who work with these devices, as it allows them to check the status of various transceivers and configure them accordingly.

### Main Interface

The main interface of the tool is divided into several sections, including a menu bar, a status display area, and a table section. The menu bar provides access to various features, such as saving, loading, and clearing the status data. The status display area shows the current status of the transceivers, and the table section provides detailed information about each transceiver.

### Table Section

The table section is where the detailed information about the transceivers is displayed. Each row in the table represents a transceiver, and the columns show various parameters such as the device ID, channel, and status. The status column includes icons that represent the current status of the transceiver, such as if it is locked or if it has errors.

### Control Panel

The control panel includes buttons for clearing the status data and for loading and saving data. These buttons allow users to manage the data in the tool efficiently.

### Conclusion

The Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Status Tool is a powerful tool that simplifies the process of monitoring and configuring transceivers in Stratix® 10 devices. It is an indispensable tool for developers and engineers who work with these devices, as it provides a comprehensive view of the transceiver status and allows for easy configuration and troubleshooting.
Tool automatically finds the Native PHY instantiated

Tool automatically finds the number of channels instantiated

Click on the button to view debug help

Uncheck the box to detect part number cable swap
TRANSCEIVER EYE DEBUG TOOL
Intel® Stratix® 10 Device Eye Viewer (On-Die Instrumentation (ODI))

- Provides on-chip eye monitoring capabilities
- Helps to optimize link equalization parameters during board bring-up
- Supports in-system link diagnostics and equalization margin testing
Existing Intel® Stratix® 10 Transceiver Toolkit Eye Viewer Algorithm

- Loop 1: Increment the vertical threshold voltage
- Loop 2: Sweep the ODI clock across for different clock phase
- Measure the error count
- Loop end
- Plot the 2-D eye diagram
Intel® Stratix® 10 Device L-Tile/H-Tile Transceiver Eye Debug Tool Algorithm

Step 1: Measure the width of the eye at V=0

Step 2: Measure the height of the eye at CDR sampling point
Transceiver L-Tile/H-Tile Eye Debug Tool
# Transceiver L-Tile/H-Tile Eye Debug Tool

The image shows a screenshot of a software interface for the Transceiver L-Tile/H-Tile Eye Debug Tool. The interface includes several sections:

- **Comms**: Options for selecting the type of connection (e.g., SFP, DAC). The panel includes a speed setting (GP12) and a latency measurement (GP10). There are also options for adjusting the measurement time and enabling or disabling the tool.

- **Measurement Type**: Options for selecting the type of measurement to perform (e.g., Eye Diagram, Eye Closure).

- **Physical Instance**: Displays information about the physical instance, including channel number and status.

- **Test Time**: Displays the time taken for each test. For example, one test took 37 ms, another took 14 ms, and another took 19 ms.

The tool emphasizes a **short measurement time** for efficient debugging. The interface is designed to provide quick and accurate data for optimizing the performance of the transceiver tiles.
### Transceiver L-Tile/H-Tile Eye Debug Tool

- **Measure the width of the eye at vertical ref of 0 volt**
- **Measure the height of the eye at the horizontal step where CDR is sampling at different bit error rate (BER)**

<table>
<thead>
<tr>
<th>Channel</th>
<th>Eye Width</th>
<th>Eye Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel 0</td>
<td>32.49</td>
<td>32.40</td>
</tr>
<tr>
<td>Channel 1</td>
<td>32.49</td>
<td>32.40</td>
</tr>
<tr>
<td>Channel 2</td>
<td>32.49</td>
<td>32.40</td>
</tr>
<tr>
<td>Channel 3</td>
<td>32.49</td>
<td>32.40</td>
</tr>
</tbody>
</table>

**Device Info:**
- **Device Name:**
- **Interface:**
- **Instance:**
- **Link:**
- **Rate:**
- **Channel:**
- **Eye Width:**
- **Eye Height:**
- **Status:**
- **Time:**

**Additional Information:**
- **Measurements:**
- **Data Table:**
- **Graphs:**
- **Visualizations:**

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**Note:**
- Measurements are taken at various vertical and horizontal levels to ensure accuracy.
Transceiver L-Tile/H-Tile Eye Debug Tool

Click to measure and log the eye once

Continuously measure and log the eye

Stop the current measurement
Transceiver L-Tile/H-Tile Eye Debug Tool

Enable or disable the measurement
Choose the horizontal step size
Choose the vertical step size
Choose PRBS or user traffic
Apply global values
Download the Transceiver Debug Tool

S10_Ltile_Htile_Transceiver_Debug_Tool_V4p0.tcl
Summary

- Needs the least user intervention
- The only way to measure internal high-speed serial interface (HSSI) voltages
- Eye debug tools are 5X faster than Transceiver Toolkit eye plots†
- The only tool that can measure eye height and width while running a protocol
BACKUP
Step 1: Program the Device and Open System Console
Step 2: Load the SOF File in the System Console
Step 3: Load the SOF File in the System Console
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