Eureka Technology

EC140 64-bit PCI Target

Product Summary

FEATURES

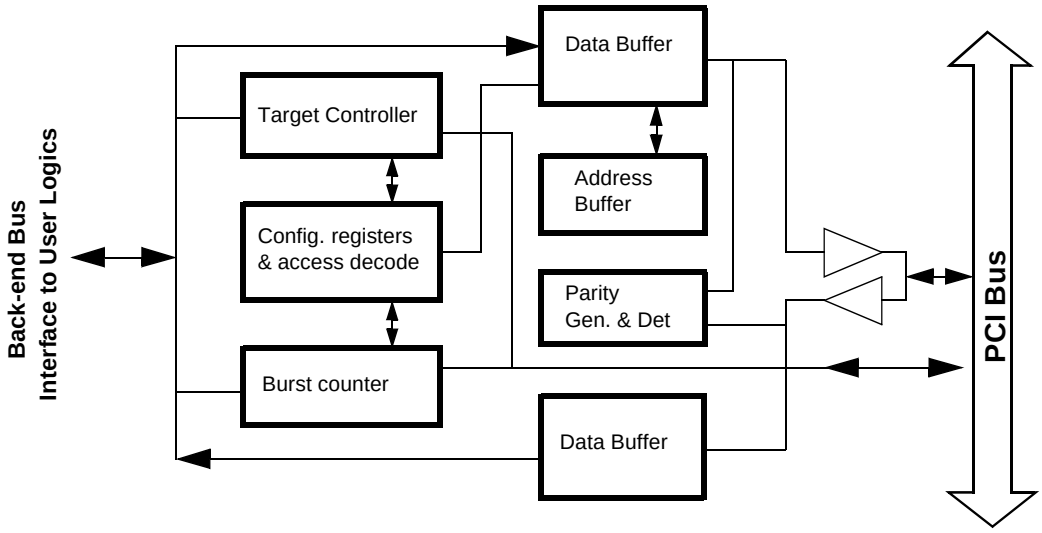
- Fully supports PCI specification 2.1 and 2.2 protocol.
- Supports both 64-bit and 32-bit bus systems.
- Supports dual address cycle (DAC) 64-bit addressing.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Combined bus master and target functions.
- Efficient back-end interface for different types of bus slave and master devices.
- Zero wait state burst data transfer.
- Automatic transfer restart on target retry and disconnect.
- High speed bus request and arbitration.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Optimized for devices with slow output enable control.

DESCRIPTIONS

The EC140 64-bit PCI bus target core is optimized for different applications. The back-end interface is a highly efficient and flexible back-end bus which provides for easy integration with other user logic. The core utilizes double data buffer design approach which minimizes design gate count and achieves highest possible data bandwidth at the same time.

The EC140 is capable of handling both 32-bit PCI transfers and 64-bit PCI transfers. Based on the bus width chosen by the master, the EC140 bus target transfers data with the higher data width whenever possible.

The PCI target controller is capable of handling memory and IO accesses on the PCI. All seven types of PCI memory/IO accesses are supported. Configuration register read and write transactions are supported locally by the bus target without



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assistance from the user logic. Data parity detection and generation are also handled by the core locally.

When a bus master on the PCI bus initiates a PCI transaction, the core decodes the address and the command and claims the transaction if the address is decoded to be within the address space of one of the target devices at the back-end. The PCI transaction is propagated to the proper target device in simple protocol through the back-end bus.

The user interface allows the user to control the characteristics of the access. For example, the user can insert a wait state or transfer data without wait state according to its data bandwidth. Single or burst transfer, retry, disconnect, delay transaction and target abort can all be controlled by user logic.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
Base address registers	Supports multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Address and data multiplexing	Separate or combined back-end address and data buses.
DAC	Dual Address cycle to support 64-bit address space.
Direct FIFO interface	The back-end bus can be made to directly interface a FIFO.
Burst length	Automatically limits the burst size beyond user specific boundaries.
Target burst	Single transfer support to minimize core size.
Target retry, disconnect, and abort	Support for back-end initiated target retry, disconnect and abort.
Asynchronous clock domains	Separate and asynchronous user and PCI clock domains. The core provides re-synchronization and data FIFO.

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