Eureka Technology

EP660 DMA Controller

Product Summary

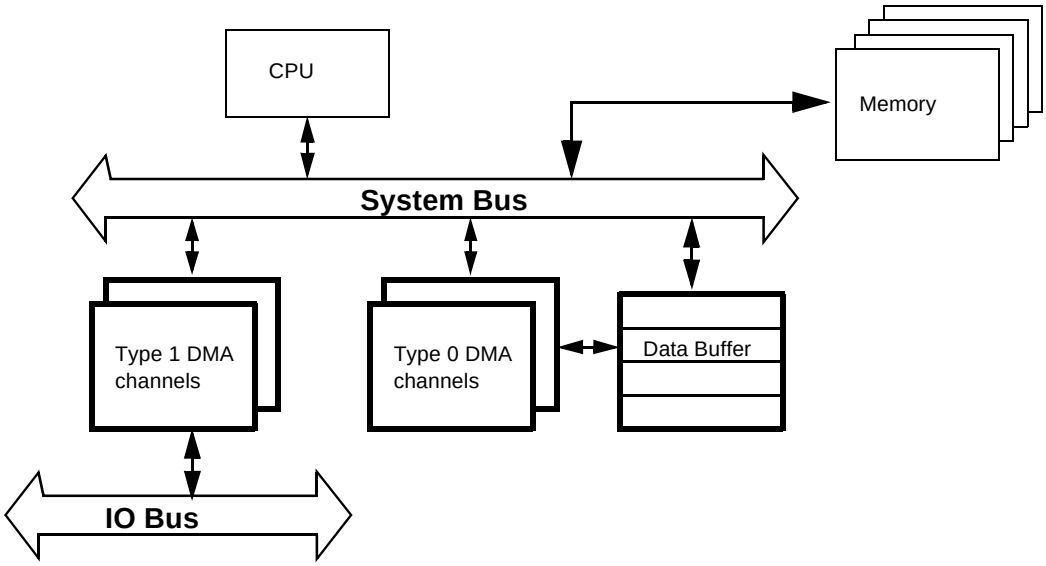
FEATURES

- Multiple independent DMA channels
- Designed with synthesizable HDL for ASIC and PLD implementations in various system environments
- Each channel programmable to two types of DMA transfers: memory-to-memory and memory-to-I/O data transfer.
- Supports both hardware initiated transfer and software initiated transfers.
- Programmable burst and single data transfer.
- Internal arbitration logic for multiple DMA channels.
- Interrupt generation on transfer completion.
- Optional DMA chaining for multiple DMA sessions.

DESCRIPTIONS

The DMA controller is designed for direct data transfer independent of CPU operations. Each channel can be programmed to support two types of DMA transfers. Type 0 transfer is designed for transferring data between devices that reside on the same bus. For example, it can be used to read data out from a memory device and write the data to a different location, where the data transfers take place on the same processor or local bus. Type 1 transfer is designed for transferring data between a memory bus and dedicated I/O bus. Each I/O channel has a dedicated interface to its I/O device. This type of module is particularly useful when the DMA core is integrated with I/O devices on the same chip.

The DMA controller supports multiple channels, each of which can be programmed independently. Each channel has a dedicated DMA request line and channel registers, and can be configured to different priority settings. When the



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DMA controller consists of multiple channels, an internal arbiter is provided with the core to grant bus ownership to one channel at a time according to the priority settings. With DMA chaining, multiple DMA sessions can be programmed at one time by the CPU for successive execution and data gathering and broadcast.

Each channel contains source and destination address registers, control register, and transfer count register. The channel's DMA operation is specified in the control register, and the number of words to transfer is specified in the transfer count register.

A type 0 transfer makes use of an internal buffer to store data to be transferred. A type 0 DMA transfer consists of two transactions, reading from a memory location to the channel's internal buffer, and writing the data to another memory location. A type 1 DMA transfer involves reading from memory and directly writing the data to an IO device, or reading from an IO device and writing the data to memory.

Burst or single data transfers are supported to interface different memory systems and bus masters.

The DMA controller allows both hardware initiated transaction, referred to as synchronized transfers, and software initiated transactions, referred to as unsynchronized transfers. Which mode of transaction a channel is supposed to perform is specified in its control register. If a channel is properly set to synchronized mode, a transaction is started by an IO device asserting its request signal to its channel. If a channel is programmed to unsynchronized mode, a transaction is started by system software setting the start bit in the channel's control register.

OPTIONAL FEATURES

The following table summarizes the optional features which can be provided with the core as required by user application.

Options	Description
Number of channels	User can choose any number of channels as required by application.
Transfer count	Number of bits in the transfer count register.
Arbiter scheme	Fixed or rotating priority scheme can be specified to arbitrate channel requests.

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