Eureka Technology

EP430 32-bit PCI Host Bridge

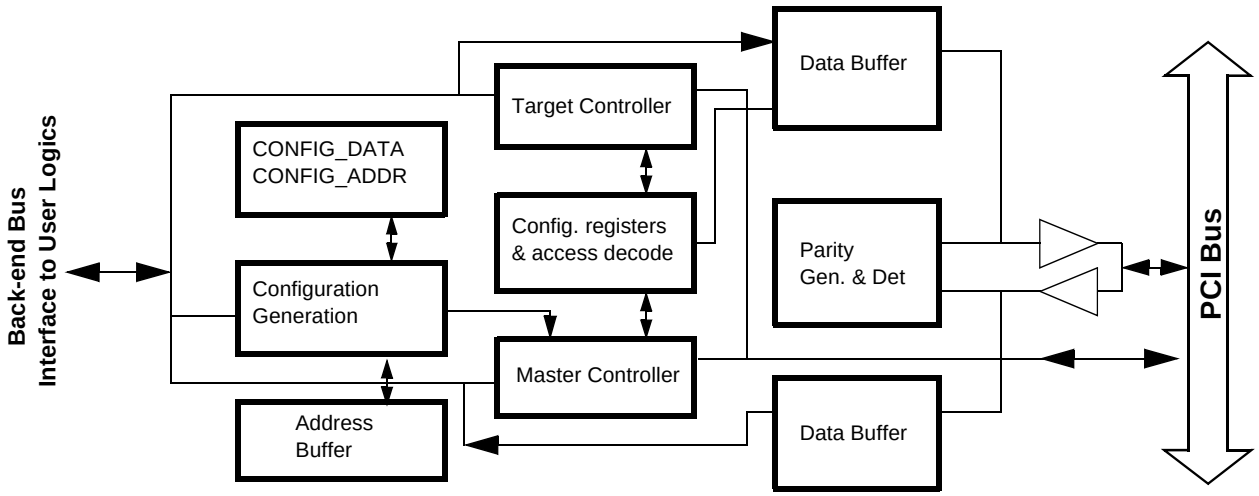
Product Summary

FEATURES

- Fully supports PCI specification 2.1 and 2.2 protocol.
- Designed for ASIC and PLD implementations.
- Fully static design with edge triggered flip-flops.
- Efficient back-end interface for different types of user devices.
- Host bridge design includes bus master, bus target and central system functions.
- Generates standard PCI type 0 and type 1 configuration accesses.
- Combined bus master and target functions.

  Master function
  - Initiate PCI memory and IO read/write.
  - Automatic transfer restart on target retry and disconnect

  Target function
  - Memory or IO read/write
  - Configuration read/write
  - Support for back-end initiated target retry, disconnect and abort.
- Supports Zero wait state and user inserted wait state burst data transfer.
- Dual write buffer supports write data posting.
- User controlled burst and non-burst data transfer.
- Automatic handling of configuration register read/write access.
- Supports user initiated target retry, disconnect, abort and delayed transaction.
- Parity generation and parity error detection.
- Includes all PCI specific configuration registers.
- Supports high speed bus request and bus parking.
- Optional PCI bus arbiter with fix, rotating, and custom priority.



4962 El Camino Real,
Los Altos, CA 94022, USA

Tel: 1 650 960 3800
Fax: 1 650 960 3805
http://www.eurekatech.com

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DESCRIPTIONS

The 32-bit PCI host bridge is designed for interfacing the host CPU with the PCI bus. This core contains options to support 32-bit or 64-bit back-end bus for different CPUs. The host bridge consists of three functions: bus master, bus target and configuration access generation.

A highly efficient and flexible back-end bus interfaces with the system CPU and user defined logics such as DMA and memory controllers. The core utilizes double data buffer design approach which minimizes design gate count and achieve highest possible data bandwidth at the same time.

The host bridge core allows the CPU or user logic to initialize the entire system during power-up reset. Configuration Mechanism #1 as defined by the PCI specification is implemented by the host bridge, and both type zero and type one transactions are supported. The local bus CPU requests configuration access on the PCI bus by writing to or reading from the CONFIG_ADDR and CONFIG_DATA registers which are contained in the host bridge. The location of these registers can be specified by the user. The host bridge initiates configuration read or write transaction to the target device as specified in CFG_ADDR.

BUS MASTER FUNCTION

The PCI host bridge is capable of initiating memory or IO read and write upon back-end requests. The type of command and the burst size are specified by the user for each data transaction. Burst size can be pre-determined by the user for each transaction or changed as the transaction progresses.

Once a master transfer begins, the core monitors the target device's signals on the PCI bus and transfers data to the user logic. All different types of transfer termination are handled by the core. If a transfer is retried or disconnected by the target, the master core re-starts the transfer automatically without the assistance of the user logic. Bus request, bus parking, parity detection and generation all are handled by the core.

BUS TARGET FUNCTION

The PCI target controller is capable of handling memory and IO accesses on the PCI. All seven types of PCI memory/IO accesses are supported. Configuration register read and write transactions are supported locally by the bus target without assistance from the user logic. Data parity detection and generation are also handled by the core locally.

When a bus master on the PCI bus initiates a PCI transaction, the core decodes the address and the command and claims the transaction if the address is decoded to be within the address space of one of the target devices at the back-end. The PCI transaction is propagated to the proper target device in simple protocol through the back-end bus.

The user interface allows the user to control the characteristics of the access. For

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example, the user can insert a wait state or transfer data without wait state according to its data bandwidth. Single or burst transfer, retry, disconnect, delay transaction and target abort can all be controlled by user logic.

The PCI target controller also responds to configuration read and write operations. The PCI configuration registers for the host bridge's own master and target functions are provided by the core and they can be accessed in the same way the host bridge accesses the configuration registers of other PCI devices. When a configuration request targets the host bridge's own configuration register, the host bridge functions as both the master and target for the configuration cycle on the PCI bus.

OPTIONAL FEATURES

The following table summarizes the optional features which are provided with the core as required by user application.

Options	Description
Back-end bus size	32-bit or 64-bit user logic (CPU) interface
Unidirectional host bridge	Remove target function support to minimize gate count.
Back-end bus type	The back-end bus can be either a generic simple user interface or interface directly to specific CPU bus.
Target bus type	The back-end interface for the target function can be directed to a separate memory interface or to the CPU interface.
Bus arbiter	Arbitration for the PCI bus.
Base address registers	Supports multiple base address registers, memory or IO mapped, and expansion ROM base address register.
Address and data multiplexing	Separate or combined back-end address and data buses.
Direct FIFO interface	The back-end target bus can be made to directly interface a FIFO.
Burst length	Automatically limits the burst size beyond user specific boundaries.
Target burst	Single transfer support to minimize core size.
Asynchronous clock domains	Separate and asynchronous user and PCI clock domains. The core provides re-synchronization and data FIFO.

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