DDR MEMORY CONTROLLER

DCM’s DDR Memory Controller is a high performance, flexible, synthesizable core that provides interface to JEDEC JESD79, Release 2 compatible DDR memory modules. The Verilog core is suitable for FPGA and ASIC applications and is available in Source code and Netlist formats.

This is a quality product delivered by a SEI CMM Level-5 certified Design Services and IP Company. The source code version is accompanied by a High Level Design document for the design.

SALIENT FEATURES*:

- Supports JEDEC-standard (JESD79, Release 2) Double Data Rate (DDR) SDRAM
- An easy to use host interface, with AMBA High-performance Bus (AHB) as optional interface
- Fully synchronous core design
- Data transfers at 200/266** MHz
- Burst lengths of 2, 4, or 8 data phases
- Configurable CAS latencies of 1.5 – 3.0 clock cycles
- Automatically generates initialization sequence
- Programmable refresh counter for automatic refresh
- Supports up to eight chip select signals for SDRAM devices
- Supports the NOP, READ, WRITE, AUTO_REFRESH, PRECHARGE, ACTIVATE, and BURST_TERMINATE SDRAM commands
- Supports data mask lines for partial write operations
- Optionally supports SPD and ECC
- Implements Bank management architecture to minimize latency
- Programmable memory size and data width
- Programmable SDRAM access timing parameters
- Supports memory data path widths of 8, 16, 32 & 64 bits
- Targeted to FPGA and ASIC libraries
- Source code license available in Verilog HDL
- Deliverables – User’s manual, Source/Netlist & Synthesis scripts

* Above specifications are subject to change  ** Data transfer at 266MHz is valid for ASIC version