Figure 1. PCI to Local Bridge Reference Design Block Diagram

32-bit PCI IP Core
- Parameterized Configuration Registers
- PCI Address/Data Buffer
- PCI Target Control
- Parity Checker & Generator
- Local Address/Data/Command/Byte Enable
- Local Target Control

Reference Design
- Local Configuration Registers
- Chip Select Control Logic
- PCI User Configuration Registers
- GPIO Control Logic
- Local Bus Control Logic
- Interrupt Generator
- Dynamic Data Bus Width Control Logic
- Endian Control Logic