White Paper

Architectural Differences Between Stratix II and Stratix Devices

Introduction

Stratix® II devices, Altera's next-generation high-density FPGAs, are based on the award-winning Stratix device architecture. Building on the innovations that made Stratix FPGAs an instant success, Stratix II devices provide new and enhanced features that significantly improve device performance and resource utilization.

This white paper explains the differences between Stratix II and Stratix features. For detailed descriptions of each feature, see the *Stratix II Device Handbook*, *Stratix Device Handbook*, and related documentation at **www.altera.com/literature**.

Features

Table 1 compares the features offered by the Stratix II and Stratix architectures.

Table 1. Stratix II & Stratix Features Comparison

Features	Stratix II	Stratix
Process	90-nm, all layer copper SRAM process	0.13-µm, all layer copper SRAM process
VCCINT	1.2 V	1.5 V
VCCPD	Used to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins	N/A
ALMs	6,240 to 71,760	N/A
LEs	15,600 to 179,400 *(1)*	10,570 to 79,040
Maximum RAM bits	9,383,040	7,427,520
TriMatrix™ memory blocks	Yes	Yes
High-speed DSP blocks	Yes	Yes
Q1.15 format rounding and saturation support	Yes	N/A
Global clock networks	Up to 16	Up to 16
Regional clock networks	Up to 32	Up to 16
Fast clock networks	N/A	Up to 8
PLLs	Up to 12	Up to 12
High-speed differential I/O support	Up to 152 channels with DPA circuitry for 1-Gbps performance	Up to 116 channels with 80 channels optimized for 840-Mbps performance
High-speed networking and communications bus standards support	RapidIO™, UTOPIA IV, NPSI, HyperTransport™ technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4), and SFI-4	RapidIO, UTOPIA IV, CSIX, HyperTransport technology, 10G Ethernet XSBI, SPI-4 Phase 2 (POS-PHY Level 4) and SFI-4
High-speed external memory support	DDR and DDR2 SDRAM, RLDRAM II, QDRII SRAM, and SDR SDRAM	DDR and DDR2 SDRAM, RLDRAM II, QDR and QDRII SRAM, SDR SDRAM, and ZBT SRAM
Design security using configuration bitstream encryption	Yes. Using the AES algorithm	N/A
Remote configuration upgrade support	Yes	Yes

Note to Table 1:

(1) Density expressed as equivalent LEs. One ALM provides the logic capacity of 2.5 four-input look-up table (LUT)-based LEs.

Logic Array Blocks

Stratix II and Stratix devices feature a similar logic array block (LAB) architecture. However, Stratix II LABs are built from different building blocks. Each Stratix II LAB consists of eight adaptive logic modules (ALMs), equivalent

to 20 logic elements (LEs), while each Stratix LAB contains 10 LEs. Table 2 compares the elements found in Stratix II and Stratix LABs.

Table 2. Stratix II & Stratix LAB Elements Comparison

LAB Elements	Stratix II	Stratix
Number of modules or elements in each LAB	8 ALMs; equivalent to 20 LEs	10 LEs
LE carry chain	Yes	Yes
LAB control signals	Yes	Yes
Local interconnect	Yes	Yes
Register chain connection lines	Yes	Yes
LUT chain	N/A	Yes
Shared arithmetic chain	Yes	N/A

LAB Interconnect

The LAB local interconnect found in both Stratix II and Stratix devices drives LEs within the same LAB. Sources for the LAB local interconnect consist of row and column interconnects as well as outputs from LEs within the same LAB. The Stratix II direct link connection allows the neighboring LABs; M512, M4K, or M RAM TriMatrix memory blocks; or digital signal processing (DSP) blocks from the left and right to drive an LAB's interconnect. Each Stratix II ALM can drive 24 other ALMs through fast local and direct link interconnects, while Stratix LEs drive 30 other LEs through the same connections.

LAB Control Signals

The Stratix II and Stratix LAB control signal blocks are similar, yet there are three clock signals and three clock enable signals in Stratix II devices, compared with only two of each signal in Stratix devices. With the increased number of clock and clock enable signals, there are a total of 11 LAB control signals in Stratix II devices, while Stratix devices have a total of 10. Stratix II devices do not support the `add/sub` control signal, while Stratix devices do. Table 3 compares the LAB control signals in Stratix II and Stratix devices.

Table 3. Stratix II & Stratix LAB Control Signals Comparison

LAB Control Signals	Stratix II	Stratix
Number of clock signals	3 *(1)*	2
Number of clock enable signals	3	2
Number of asynchronous clear signals	2	2
Number of synchronous clear signals	1	1
Number of asynchronous preset/load signals	1	1
Number of synchronous load preset/load signals	1	1
Number of `add/sub` control signals		1
Total number of control signals	11	10

Note to Table 3:

(1) The three clock signals are derived from two different sources. See the *Stratix II Device Handbook* for more information.

Adaptive Logic Module

The basic building block of logic in the Stratix II architecture, the ALM, provides faster performance and more efficient logic utilization, as compared with Stratix LEs. Table 4 compares the components of Stratix II ALMs with Stratix LEs.

Table 4. Stratix II ALMs & Stratix LEs Comparison

Component	Stratix II ALMs	Stratix LEs
Inputs	Up to 8	4
Logical outputs	Up to 2 combinational and 2 registered outputs	1 combinational and 1 registered output
Programmable registers	2	1
Number of dedicated full adders	2	N/A
Carry chain	Yes	Yes
Shared arithmetic chain	Yes	N/A
Register chain	Yes	Yes
Register packing	Yes	Yes

For more information on the efficiencies of the Stratix II ALM and its comparison to previous architectures, see the *Logic Structure Comparison between Stratix II & Virtex-Based Architectures* white paper.

MultiTrack Interconnect

In the Stratix II and Stratix architectures, the MultiTrack™ interconnect structure connects ALMs or LEs, TriMatrix memory blocks, DSP blocks, and device I/O pins. The interconnects include row- and column based routing resources, summarized in Tables 5 and 6, respectively. R8 and C8 routing resources are not available in Stratix II devices.

Table 5. Stratix II & Stratix Row-Based Routing Resources Comparison

Resources	Stratix II	Stratix
Direct Link interconnects between LABs and adjacent blocks	Yes	Yes
R4 interconnects traversing 4 blocks to the right and left	Yes	Yes
R8 interconnects traversing 8 blocks to the right and left	N/A	Yes
R24 row interconnects for high-speed access across the length of the device	Yes	Yes

Table 6. Stratix II & Stratix Column-Based Routing Resources Comparison

Resources	Stratix II	Stratix
LUT chain interconnects within an LAB	N/A	Yes
Shared arithmetic chain interconnects within an LAB	Yes	N/A
Register chain interconnects within an LAB	Yes	Yes
Carry chain interconnects within an LAB and from LAB to LAB	Yes	Yes
C4 interconnects traversing a distance of 4 blocks in up and down direction	Yes	Yes
C8 interconnects traversing a distance of 8 blocks in up and down direction	N/A	Yes
C16 interconnects for high-speed vertical routing through the device	Yes	Yes

TriMatrix Memory

Stratix II devices feature the TriMatrix memory architecture introduced in Stratix devices and include the following enhancements:

- Byte enable
- Pack mode
- Address clock enable

- Register clears

All Stratix II TriMatrix memory blocks support “asynchronous clear” at the output registers only.

Byte Enable

The byte enable feature in Stratix II and Stratix devices differs in the following ways:

- All Stratix II TriMatrix memory blocks support byte enable, whereas Stratix devices support this feature in only M4K and M-RAM blocks.
- The Stratix II byte enable feature masks specific bytes, nibbles, and bits of data to be written, whereas in Stratix devices the feature only masks a specific byte.
- Stratix II devices do not have a clear port to the byte enable registers. Asserting the clear port of the byte enable registers in Stratix devices, however, drives the byte enable signal to their default high level.

Stratix II devices enable byte write for various data widths, depending on memory type, as shown in Table 7.

Table 7. Byte Enable Data Width for Stratix II Devices

TriMatrix Memory Block Type	Byte Enable Data Width
M512	x1, x2, x4, x8, x9, x16, x18
M4K	x1, x2, x4, x8, x9, x16, x18, x32, x36
M-RAM	x8, x9, x16, x18, x32, x36

Pack Mode

Stratix II devices offer pack mode support, which allows a design to implement two single-port memory blocks in a single M4K or M-RAM block under the following conditions:

- Each of the two independent block sizes is equal to or less than half of the M4K or M4K block size.
- Each of the single-port memory blocks is configured in single-clock mode.

Address Clock Enable

M4K and M-RAM memory blocks in Stratix II devices support the clock enable signal, which holds the previous address value while the signal is enabled. When the memory blocks are configured in dual-port mode, each port has an independent address clock enable.

See the *Stratix II Device Handbook* for more information on address clock enable functionality.

Register Clears

Stratix II devices support register clears at only the output registers in all TriMatrix memory blocks. Stratix M4K and M512 memory blocks, however, allow asynchronous clears on both input and output registers. Table 8 compares the register clears support in Stratix II and Stratix devices.

Table 8. Stratix II & Stratix Devices Register Clears Support Comparison

Memory Blocks	Stratix II	Stratix
M512	Output registers only	Input and output registers
M4K	Output registers only	Input and output registers
M-RAM	Output registers only	Output register only

DSP Blocks

Each Stratix II device has two to four columns of DSP blocks that efficiently implement multiplication, multiply-accumulate (MAC), and multiply-add functions, representing a two to four times increase over Stratix devices in DSP bandwidth for equivalent logic densities. Stratix devices have only two columns of DSP blocks.

Q1.15 Format Rounding & Saturation Support

The multipliers in Stratix II devices support rounding and saturation on the Q1.15 input format. Similarly, the accumulator in Stratix II DSP blocks can be initialized to any value and supports rounding and saturation on the Q1.15 input format. This feature simplifies the porting of DSP-processor-based designs using fixed-point numbers to FPGAs.

Dynamic Input Support

Stratix II devices feature dynamic input support that allows designers to dynamically select whether a particular multiplier operand is fed by regular data input or by the dedicated shift register input using the `sourcea` and `sourceb` signals. A logic value 1 on the `sourcea` signal selects dedicated scan-chain to feed data A; a logic value 0 selects regular data input to feed data A.

Adder & Output Block

Both the adder and output blocks in a DSP block of Stratix II and Stratix devices can be configured as:

- An accumulator that can be optionally loaded
- A one-level adder
- A two-level adder with dynamic addition/subtraction control on the first-level adder

The final stage of a Stratix DSP block can be configured as a 36-bit multiplier. Apart from this mode, Stratix DSP blocks support 9x9-bit and 18x18-bit complex multiplier modes.

The accumulator (a new feature in Stratix II devices) can be initialized or preloaded with a non-zero value using the `accum_sload` signal and the `accum_sload_upper_data` bus with one clock cycle latency. Preloading the accumulator is done by adding the result of the multiplier with the value specified on the `accum_sload_upper_data` bus.

Operational Modes

The DSP blocks in both Stratix II and Stratix devices can be used in any of the four basic operational modes, depending on the application requirements. Table 9 shows the operational modes and the number of multipliers that can be implemented in a single DSP block in Stratix II and Stratix devices.

Table 9. DSP Block Operational Modes in Stratix II & Stratix Devices

Operational Modes	9 x 9	18 x 18	36 x 36
Simple Multiplier	Eight multipliers with eight product outputs	Four multipliers with four product outputs	One multiplier
Multiply Accumulator	Two 34-bit multiply-accumulate blocks *(1)*	Two 52-bit multiply-accumulator blocks	-
Two-Multiplier Adder	Four two-multiplier adder (Two 9x9-bit complex multiplier)	Two two-multiplier adder (Two 18x18-bit complex multipliers)	-
Four-Multiplier Adder	Two four-multiplier adder	One four-multiplier adder	-

Note to Table 9:

(1) This feature is only available in Stratix devices.

In addition to the operational modes shown in Table 9, Stratix II devices support mixed modes and mixed multiplier sizes in the same DSP block. For example, half of a DSP block can implement one 18x18 bit multiplier in multiply-accumulator mode, while the other half of the DSP block implements four 9x9 bit multipliers in simple multiplier mode.

PLLs

The Stratix II enhanced and fast phase-locked loops (PLLs) inherit most of the features found in Stratix device PLLs, and contain additional features, including:

- Counter cascading
- Enhanced lock detect circuit
- PLL reconfiguration
- Reconfigurable bandwidth
- Phase shift stepping using the PLL reconfiguration scan chain

See the *Stratix II Device Handbook* for more information on PLLs and clock networks.

Counter Cascading

The Stratix II enhanced PLLs support counter cascading of the post-scale counters to facilitate larger (>512) counter sizes. This is implemented by feeding the output of one counter into the input of the next counter in a cascade chain. When cascading counters to implement a larger division of the high-frequency VCO clock, the cascaded counters behave as one counter with the product of the individual counter high/low settings. This feature is available with enhanced PLL only.

Enhanced Lock Detect Circuit

The lock output indicates that the PLL has locked onto the reference clock. Without any additional circuitry, the lock signal may toggle as the PLL begins tracking the reference clock. A designer may need to gate the lock signal for use as a system control. Either a gated lock signal or an ungated lock signal from the locked port can drive the logic array or an output pin.

The Stratix II PLLs include a programmable counter that holds the lock signal low for a user-selected number of input clock transitions. This allows the PLL lock signal to stabilize before enabling the lock signal. The designer can use the Quartus® II software version 4.0 and later to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or assertion of `pllenable`. Both the enhanced PLLs and fast PLLs support this feature.

PLL Reconfiguration

In Stratix II devices, both enhanced and fast PLLs support real-time PLL reconfiguration, while in Stratix devices, only enhanced PLLs support this feature. The PLL components that are configurable in real-time and supported in both Stratix II and Stratix devices include the following:

- Pre-scale counter (N)
- Feedback counter and VCO phase tap selection (M, $\Delta\phi_M$)
- Post-scale output counters and VCO phase tap selection (C0-C5, $\Delta\phi_{C0\text{-}C5}$)

The following real time-configurable PLL components are supported in Stratix II devices only:

- The charge pump current, loop filter components can be dynamically adjusted to facilitate on-the-fly reconfiguration of PLL bandwidth.
- Phase-shift stepping is supported, which allows 45° phase shift (of the VCO) stepping using the `scanwrite` signal.

Clock Networks

The Stratix II clock networks differ from Stratix clock networks in the following ways:

- Dynamic clock power down mode is supported

- Dynamic clock source selection is supported
- The number of regional clocks increased to 32 (from 16 in Stratix devices)
- Fast clock networks are not available

Dynamic Clock Power Down Mode

Stratix II devices support dynamic clock network enable/disable, so that the clock networks that are not being used can easily be turned off, reducing the overall power consumption on the device. The Stratix II clock networks can be powered down by both static and dynamic approaches. When power down is enabled, all the logic fed by the clock net is in an off-state.

Static Power Down

The unused global and regional clock networks are automatically powered down through configuration bit settings in the configuration file. The Quartus II software handles this function.

Dynamic Power Down

The dynamic power down control feature is applied on `GCLK` and `RCLK` clock networks, and to `pll_out` pins. It allows the internal logic to control power down/up synchronously on `GCLK` and `RCLK` networks. This function is independent of the PLL and is applied directly on the clock network.

Dynamic Clock Source Selection

The clock source selection of Stratix II global clocks select block can be controlled either statistically or dynamically. The user has the option of statically selecting the clock source by using the Quartus II software to set specific configuration bits in the configuration file (SRAM Object File [**.sof**] or Programmer Object File [**.pof**]) or controlling the selection dynamically by using internal logic to drive the multiplexer select inputs.

When selecting statically, the clock source can be set to any of the inputs to the select multiplexer. When selecting the clock source dynamically, the user can select one of the following:

- Between two PLL outputs (such as the `C0` or `C1` outputs from one PLL)
- Between two PLLs (such as the `C0`/`C1` clock output of one PLL or the `C0`/`C1` c1ock output of the other PLL)
- Between two clock pins (such as `CLK0` or `CLK1`)
- Between a combination of clock pins or PLL outputs. For the regional clock select block, the clock source selection can only be controlled statically using configuration bits. Any of the inputs to the clock select multiplexer can be set as the clock source.

I/O Capabilities

The I/O capabilities of Stratix II devices are well-designed to ensure that the high performance ALMs, embedded memory, high-bandwidth DSP blocks, and extensive routing resources are fully utilized. The following features have significant differences as compared with Stratix devices:

- I/O standard support
- Programmable output drive strength for voltage-referenced I/O standards
- On-chip termination for the HyperTransport I/O standard
- External memory interface

See the *Stratix II Device Handbook* for more information on Stratix II I/O blocks.

I/O Standard Support

Table 10 compares the I/O standards supported in Stratix II and Stratix devices.

Table 10. Stratix II and Stratix I/O Standard Differences

I/O Standard *(1)*	Stratix II	Stratix
AGP 1x	N/A	Yes
AGP 2x	N/A	Yes
SSTL-3 class I	N/A	Yes
SSTL-3 class II	N/A	Yes
Differential SSTL-2 class I	Yes *(2)*	N/A
Differential SSTL-2 class II	Yes *(2)*	*(3)*
Differential SSTL-18 class I	Yes *(2)*	N/A
Differential SSTL-18 class II	Yes *(2)*	N/A
1.8-V differential HSTL class I	Yes *(2)*	N/A
1.8-V differential HSTL class II	Yes *(2)*	N/A
1.5-V differential HSTL class I	Yes *(2)*	*(4)*
1.5-V differential HSTL class II	Yes *(2)*	*(4)*
GTL	N/A	Yes
GTL+	N/A	Yes
CTT	N/A	Yes
PCML	N/A	Yes

Notes to Table 10:

(1) Only those I/O standards with differing support in Stratix II and Stratix devices are included in this table. For a full list of supported I/O standards, see the *Stratix II Device Handbook* and *Stratix Device Handbook*.
(2) Supports both input and output. See the *Stratix II Device Handbook* for more information.
(3) Available as differential SSTL-2 support on the output clock only. See the *Stratix Device Handbook* for more information.
(4) Available as differential 1.5-V HSTL support on either input or output clock only. See the *Stratix Device Handbook* for more information.

Programmable Drive Strengths

Stratix II devices allow designers to determine the output buffer drive strengths not only for single-ended I/O standards, but also for voltage-referenced I/O standards. Table 11 summarizes the options available.

Table 11. Stratix II and Stratix Programmable Drive Strengths Summary

I/O Standard	Stratix II Ioh/Iol Current Strength Setting (mA) *(1)*	Stratix Ioh/Iol Current Strength Setting (mA) *(1)*
3.3-V LVTTL	24, 20, 16, 12, 8, 4	24, 16, 12, 8, 4
3.3-V LVCMOS	24, 20, 16, 12, 8, 4	24, 12, 8, 4, 2
2.5-V LVTTL/LVCMOS	16, 12, 8, 4	16, 12, 8, 2
1.8-VLVTTL/LVCMOS	12, 10, 8, 6, 4, 2	12, 8, 2
1.5-V LVCMOS	8, 6, 4, 2	8, 4, 2
SSTL-2 class I	12, 8	N/A
SSTL-2 class II	24, 20, 16	N/A
SSTL-18 class I	10, 8, 6, 4	N/A
SSTL-18 class II	18, 16, 8	N/A
HSTL-18 class I	12, 10, 8, 6, 4	N/A
HSTL-18 class II	18, 16	N/A
HSTL-15 class I	12, 10, 8, 6, 4	N/A
HSTL-15 class II	20, 18, 16	N/A

Note to Table 11:

(1) The table shows the available settings for column I/Os only. See the *Stratix II Device Handbook* and *Stratix Device Handbook* for more information on row I/O settings.

On-Chip Termination for HyperTransport I/O Standard

Stratix II devices offer the 100-Ω differential HyperTransport termination resistor for HyperTransport technology using on-chip differential termination. The designer can choose to turn on this feature to reduce board space utilization. The differential termination for LVDS is supported in both Stratix II and Stratix devices.

See the *Stratix II Device Handbook* for more information on this feature.

External Memory Interface

The Stratix II external memory interface support differs from the Stratix external memory interface support in the following ways:

- A PLL output can be used as the input reference clock to the delay-locked loop (DLL).
- The shifted DQS signal can go into the logic array.
- The DLL in Stratix II devices has more phase-shift options than in Stratix devices. It also has the option to add phase offset settings.
- The DLL has been enhanced to offer low jitter mode.
- DQS logic blocks with each DQS pin helps fine tune the phase shift.
- The DQS delay settings can be routed from the DLL into the logic array. The designer can also bypass the DLL and send the DQS delay settings from the logic array to the DQS logic block.
- Stratix II devices support DQSn pins.
- The DQS/DQ groups now support x4, x9, x18, and x36 modes.
- Stratix DQS pins have been enhanced with the DQS postamble circuitry for Stratix II.

See the *Stratix II Device Handbook* for more information on external memory interfaces.

Configuration Support

Stratix II devices support the active serial (AS) configuration scheme using serial configuration devices (for example, EPCS4, EPCS16, and EPCS64 devices). Stratix II devices also offer the following features that are not supported in Stratix devices:

- Configuration data decompression to reduce configuration file storage
- Design security using data encryption to protect designs

See the *Stratix II Device Handbook* for more information on configuration support.

Device Configuration Data Decompression

This feature allows the compressed configuration data to be stored in configuration devices or other memory. Stratix II devices support decompression in the fast passive parallel (FPP) when using a MAX® II device/microprocessor + flash, and the AS and passive serial (PS) configuration schemes.

Design Security Using Data Encryption

Stratix II devices are the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm. When the design security feature is enabled, a Stratix II device must be configured with a configuration file that was encrypted using the same 128-bit security key.

New Power Supply in Stratix II Devices

Stratix II devices also offer a new power supply, V_{CCPD}, which must be connected to 3.3 V to power the 3.3 V/2.5-V buffer available on the configuration input pins and JTAG pins. V_{CCPD} applies to all the JTAG pins (TCK, TMS, TDI, TDO, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_PULLUP

DATA[7..0], RUnLU, nCE, nCEO, nWS, nRS, CS, nCS, and CLKUSR. The VCCSEL pin allows the V_{CCIO} setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs.

Therefore, when selecting the V_{CCIO}, the V_{IL} and V_{IH} levels driven to the configuration inputs do not have to be a concern. The configuration input pins (nCONFIG, DCLK [when used as an input], nIO_PULLUP, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V_{CCPD}, while the 1.8-V/1.5-V input buffer is powered by V_{CCIO}.

Conclusion

FPGA performance reaches new heights with the Stratix II device family. Built on a new and innovative logic structure, Stratix II devices are the industry's fastest and highest-density FPGAs. Extending the possibilities of FPGA design, Stratix II devices allow designers to meet the high-performance requirements of today's advanced systems without having to resort to developing costly ASICs. Based on award-winning Stratix device family architecture, Stratix II devices are outfitted with a powerful set of system-level features and incorporate many significant enhancements and new capabilities.

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