

Using Stratix GX Devices for SONET/SDH Backplanes

A backplane connects cards in network systems. Most backplanes have parallel interfaces, such as versa module Eurocard (VME) or compact PCI. However, high-performance systems require serial backplane interfaces. Initially, serial backplane standards did not exist, so many companies created proprietary backplanes. Recent serial backplane standardization efforts will reduce design effort and product inventory. One of the most common serial backplanes is the SONET/SDH interface. This interface has many of the features of the line-side application, including scrambling, framing and parity checking. For SONET/SDH applications the synchronous transport signal STS-48 or synchronous transport module STM-16 interface are becoming commonplace in backplane technology that supports either one or multiple connections, while STS-192 or STM-64 are also gaining some popularity.

The feature-rich architecture of Altera Stratix[®] GX devices provides an implementation of SONET/SDH backplanes. Stratix GX devices incorporate Stratix FPGA architecture with up to 20 flexible transceivers capable of operating at 622 Mbps to 3.125 Gbps over 40" of FR4 printed circuit board (PCB) trace, making them effective for the STS-12/STM-4, STS-48/STM-16, and STS-192/STM64 standards. In addition, designers can implement many functions associated with SONET/SDH processing, which are beyond the backplane interface.

Stratix GX devices can implement SONET/SDH standard backplane features as well as other associated design considerations. Table 1 summarizes these features and design considerations. This white paper explains them in more detail.

Table 1. SONET/SDH Features & Design Considerations Supported by Stratix GX Devices

| SONET/SDH Features | Backplane Support & Signal Integrity | Beyond the Backplane Interface(1) |
|------------------------------------|---|--|
| A1A2 alignment | Programmable drive strength | Traffic management (1) |
| B1/B2 parity checking | Pre-emphasis | Scheduler interface |
| Scrambling and descrambling | Receiver equalization | Central and distributed switch fabric |
| Clocking | On-device termination | |
| H1/H2 Ppointer Pprocessor function | Hot-swap capable | |
| | 40" FR4 PCB Fabric drive capability @3.125Gbps | |

Note to Table 1:

1. Refer to the *Using Stratix GX for Traffic Management* white paper.

System Overview

A typical network system consists of three separate cards:

- Line card
- Switch fabric card
- Host CPU card

The backplane interface from the line or switch card provides the connectivity between the cards and, if designed correctly, allows for system expansion.

The two backplane implementations, central switch and distributed switch, are discussed below. For more information see the *Using Stratix GX in Switch Fabric Systems* white paper. Stratix GX devices can provide the high-speed transceiver technology on the edge of the card as well as traffic and queue management in either a central switch fabric system or a distributed switch fabric system.

The STS-48 standard provides an interface for one 2.5-Gbps channel. However, a card can use redundancy to include more than one channel. For example, the switch card is specified to support N line cards, so the backplane will have N connections. Designers can add lower-speed line interfaces (e.g., STS-3 and STS-12) to an STS-48 interface on the switch card. At high line rates such as with the STS-192 standard, a quad transceiver typically configures the backplane interface, and each channel supports a data rate up to 2.5 Gbps, reaching a total of 10 Gbps. The data is rebuilt at the receiver using channel alignment.

Central Switch Fabric

A central switch system contains a switch fabric card to connect all the line cards in the system in a star topology. Each card uses a high-speed serial link across the backplane to the switch. Generally, the most common topology for SONET/SDH backplanes is for a number line cards to connect to a single switch fabric card. For reliability, this system would probably have two switch cards; one working and one for backup.

Applications requiring higher data rates such as with the STS-192 standard usually align four channels together to provide a 10-Gbps interface. It is likely that most switch fabric cards supporting OC-192 interfaces will require more than one device to support multiple line cards. This is dependant on the complexity of the data processing and the number of ports required.

Distributed Switch Fabric

Distributed switch fabric differs from central switch fabric because it does not have a dedicated switch card. Each line card includes circuitry to provide the switching interface to the other cards in the system. Within a distributed system, each card connects to every other card on the system, resulting in a mesh-type topology on the backplane.

SONET/SDH Backplanes

SONET/SDH backplanes are not designed to a specific standard because different telecom manufacturers have developed their own proprietary busses. The backplane transceiver in a SONET/SDH application requires two types of features: protocol-specific functions, including the framing and scrambling, and electrical features required to ensure the signal can be transmitted successfully. Stratix GX FPGAs can

provide both of these features on a backplane transceiver. Many designers implement a subset of the SONET/SDH standard, including:

- Using A1A2 for frame delineation
- Scrambling with a polynomial
- Using B1 and B2 for error detection
- Clocking options
- Optional pointer processing of H1 H2

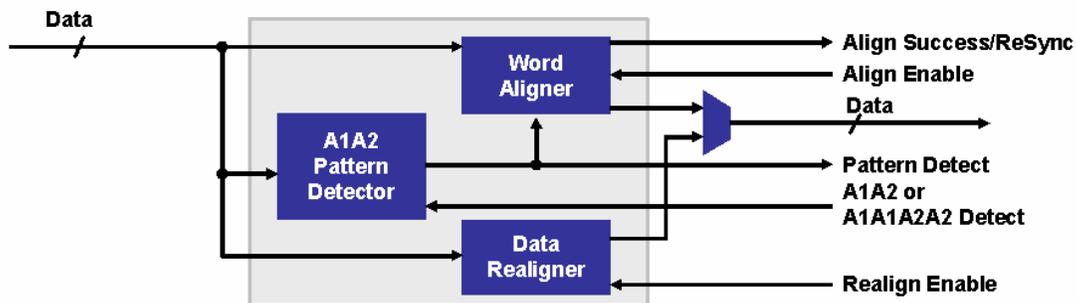
Alignment (A1A2)

High-speed SONET/SDH backplanes use clock data recovery (CDR) techniques to transfer data across one or more serial channels and recover the clock from the input data stream. Then the backplane uses this clock to extract the data. The data is then deserialized using a division of the recovered clock equal to the bit width of the deserializer. In the case of STS-48, the backplane deserializes the 2.5-Gbps input data into an 8-bit word and uses a 312-MHz divided clock to clock the data. This clock is then used by the rest of the transceiver block to process the parallel data.

Since the input is completely serial, it cannot preserve the word boundaries. To signify the start of the frame, the SONET/SDH standards require the characters A1A2 in the frame overhead. The receiver must detect these characters to correctly align the data into 16-bit words.

Stratix GX device transceivers provide dedicated circuits for A1A2 detection and word alignment functions. The transceiver includes a word aligner which can be programmed to detect A1A2 or, in the case of higher data rates, A1A1A2A2. Raw data is passed into the pattern detector, once the transceiver detects the preset pattern, a signal is passed to the word aligner to instruct it to align words to a particular boundary. Figure 3 shows the pattern detector block diagram for the Stratix GX architecture.

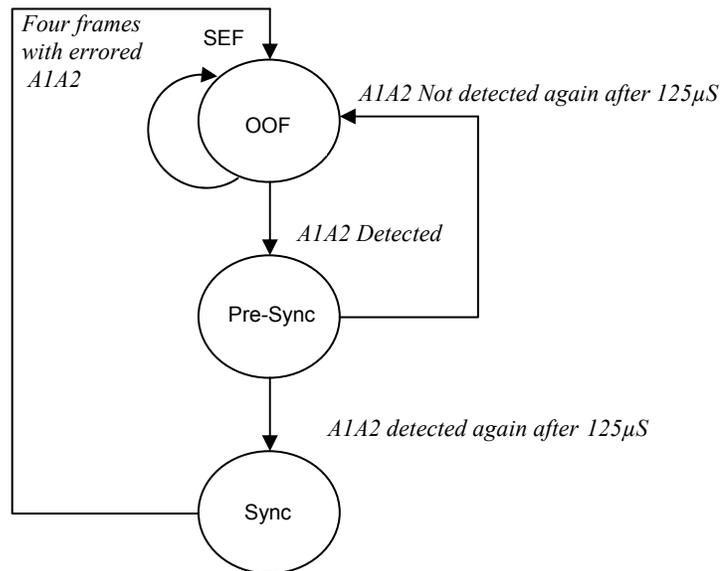
Figure 3. Block Diagram of a Pattern Detector for the Stratix GX Architecture



A finite state machine (FSM) implemented in the FPGA fabric may be used in conjunction with output from the pattern detector to ensure the framing pattern detected is the correct pattern. In a SONET/SDH backplane system, the FSM measures the interval between framing patterns to see if it is the required 125 μ s. The FSM also determines when the framer goes from being in frame to out of frame. This usually occurs if the receiver does not detect the A1A2 pattern in the expected position at the beginning of the frame for several frames. The FSM may also produce severely errored frames (SEF) and loss of frame (LOF) signals if implemented for SONET/SDH backplanes. The FSM for a typical STS-48 application

should use about 300 logic elements (LEs) and be easy to implement in an FPGA. Figure 4 shows a typical FSM implementation.

Figure 4 Finite State Machine to Confirm Frame Pattern



Parity Codes (B1/B2)

Another SONET/SDH standard feature used for backplane applications are the B1/B2 bit interleaved parity 8 (BIP-8) bytes. Each BIP code is used to determine errors in bits transmitted in the previous frames.

- B1 calculates the even parity of every byte in the previous frame, after scrambling.
- B2 is the even parity of every byte in the previous frame, before scrambling, excluding the SONET/SDH section or SDH regenerator section overhead.

Programmable logic is ideal for generating and detecting parity algorithms, and intellectual property (IP) is readily available. The system can use the same circuitry as used in the line side SONET/SDH. The B1 and B2 functions require two separate blocks, since B1 is implemented on scrambled data and B2 is implemented on non-scrambled data. For the STS-48 standard, the B1 function requires less than 100 LEs in each direction, while the B2 function requires less than 100 LEs but will use RAM to store partially calculated B2 values.

Scrambling/Descrambling

SONET/SDH standards use a variety of scrambling polynomials for transmission. Scrambling provides DC-balancing and ensures sufficient transition density for the receivers CDR to operate properly. The Stratix GX architecture does not include a scrambling block inside the transceiver and uses IP to create a

scrambler with standard scrambling polynomials, such as $1+x^6+x^7$. For the STS-48 standard, the scrambling function requires less than 100 LEs in each direction.

Clocking

Although clock and jitter specifications are less stringent on SONET/SDH backplane than line side applications, it is still important to ensure the quality of the clock to guarantee the signal eye can be detected correctly.

Stratix GX dedicated phased-locked loops (PLLs) support high-speed transceivers. The PLLs' flexibility allows a single clock source to support many different standards. This is useful when a card may need to support different rates within a system or when a single card is used in multiple applications. Table 2 outlines the different SONET/SDH standards and the associated clock/data rate. If encoding, such as 8b10b or FEC is added, the frequency may be higher.

Table 2. SONET/SDH Standards & Data Rates

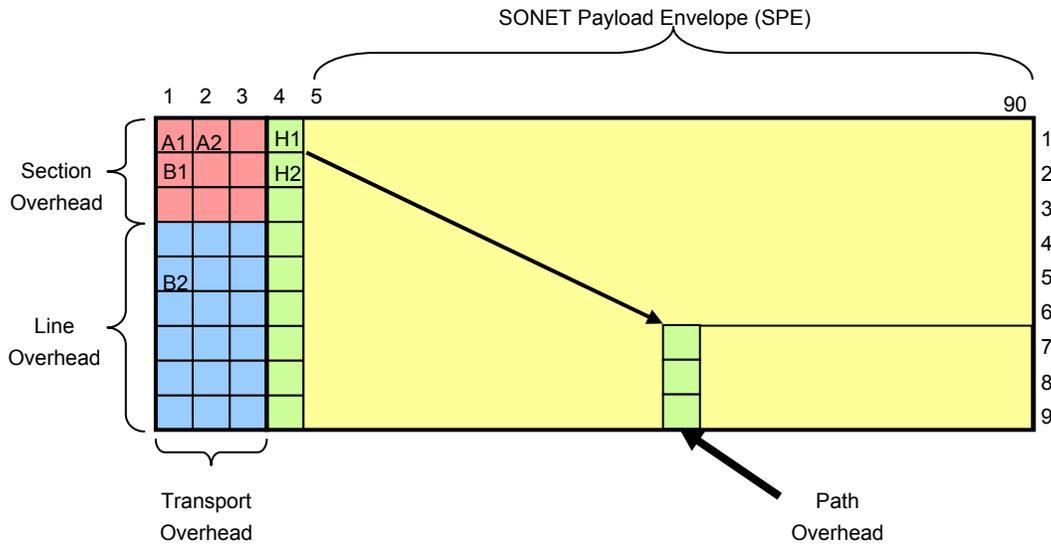
| SONET/SDH Standard | | SDH | Line Rate (Mbps) | Stratix GX Support |
|--------------------|----------------------------|---------|------------------|-------------------------|
| STS Level | Optical Carrier (OC) Level | | | |
| STS-12 | OC-12 | STM-4 | 622.08 | Single channel |
| STS-48 | OC-48 | STM-16 | 2,488.32 | Single channel |
| STS-192 | OC-192 | STM-64 | 9,953.28 | 4 channels at 2,488.32 |
| STS-768 | OC-768 | STM-256 | 39,813.12 | 16 channels at 2,488.32 |

Pointer Processor Function (H1/H2)

The pointer processor function is used when a backplane carries data from line cards with different clock sources. The pointer processor allows data to move within the frame while the backplane uses a single clock. The pointer processor calculates the location of the path overhead column and associated synchronous payload envelope (SPE). The pointer processor holds the location as an offset on the H1 and H2 pointer bytes. The receiver interprets the pointer information to determine the location of the data. In time-division multiplexed (TDM) SONET/SDH applications, the SPE includes virtual containers, which in turn include an additional layer of pointer processing (e.g., the virtual containers are like sub-SONET frames with their own overheads or pointers). The pointer processor is effectively a FSM and requires 500 logic elements (Les) for both directions. The pointer processor requires more resources with increased payloads.

The need to implement the pointer processor function in backplane applications is dependant on the application and the system clocking environment. Figure 5 shows a typical SONET/SDH frame for backplane applications that include the pointer processor function.

Figure 5 Typical SONET/SDH Frame for Backplane Application



FPGA Interface

SONET/SDH data processing is generally performed on a 16-bit or wider parallel data path to reduce system speed and overhead requirements. This requires a flexible interface between the transceiver and the system fabric. The Stratix GX architecture implements a synchronization FIFO interface between the FPGA and transceiver. The advantages to this are it allows:

- The data path to be changed from an 8-bit to a 16-bit path into the CPU, enabling the data to be clocked at a lower speed without the use of additional logic.
- For optional synchronization, if the FPGA clock is independent of the receiver clock.

Once the clock is in the FPGA, it may be necessary to further subdivide the bus to suit the framer application depending on the framer IP and speed of the protocol. For example Altera IP supports an 8-bit interface for an STS-3 and STS12 framer, while an STS-192 framer requires a 64-bit interface.

Beyond the Backplane

The integration of high-speed transceivers into FPGA architecture makes it difficult to define where the backplane interface ends and where the rest of system blocks begin. For the simplistic building blocks described in the sections above, the interface implementation needs less than 5% of a Stratix GX EP1SGX25 device's LEs. This provides a large area of the device for other aspects of the line- or switch-card application.

Table 3. LE Utilization for a STS-48 Backplane Application Implemented with a Stratix GX Device

| Transmitter Functionality | | | Receiver Functionality | | |
|---------------------------|-----|-----------------------------|--------------------------|-------|-----------------------------|
| Function | LEs | Utilization of 1GSX25F FPGA | Function | LEs | Utilization of 1GSX25F FPGA |
| A1/A2 Framing | 100 | 3% | A1/A2 Monitor | 300 | 5% |
| B1 Insertion | 100 | | B1 Extraction | 100 | |
| Scrambling | 100 | | De-scrambling | 100 | |
| B2 Insertion | 100 | | B2 Extraction | 100 | |
| H1/H2 Generation | 200 | | H1/H2 Pointer Processing | 500 | |
| Total | 600 | | Total | 1,110 | |

In a line-card application, the Stratix GX device can implement the backplane functionality as well as the traffic management and buffer manager task. The high-speed memory interface allows connection to double data rate (DDR), FCRAM, SDR, zero-bus turnaround (ZBT), and quad data rate (QDR) memory, providing high-performance external packet buffering. The DPA functionality built into the Stratix GX 1-Gbps source-synchronous I/O channels also provides a high-speed bus to support SPI4.2 or a XSBI interfaces to the packet and network processors.

In a switch-card application, the Stratix GX device can implement the scheduler interface controlling the backplane interface. Stratix GX TriMatrix memory is ideal for crossbar switch fabric designs. The three memory structures are suited to different aspects of the application. For example, the 512Kbit M-RAM blocks can store queue buffer pointers as part of a buffer manager on a switch fabric card, while the 4-Kbit M4K blocks could queue first-in first-out (FIFO) buffers to support the crossbar fabric within the scheduler.

Signal Integrity Requirement

One of the issues of transceiver-based backplanes is that of signal integrity. The transceiver technology must be able to drive a reasonable distance of FR4 fabric. Although FR4 is not an ideal material for transmitting data at high speeds, its price makes it a preferable option. In order to overcome these FR4 issues, transceivers usually include features to use the cheaper FR4 fabrics.

As data rates increase, the faster edge rates raise the transmission line effects on the signals, making it difficult to successfully transmit data between the transmitter and receiver. Some flexibility is necessary within the transceiver to provide accurate signal conditioning, which allows the transceiver to overcome some of these issues. This is particularly true in a chassis environment because the track length can vary due to the different card slots locations and backplane characteristics. Because of this, the card can have different signal integrity characteristics depending on its location or slot in the backplane. Stratix GX devices have a number of features that improve signal integrity:

- Programmable drive strength
- Pre-emphasis
- Receiver equalization
- On-device termination

Programmable Drive Strength

Backplanes are inherently lossy causing signal attenuation. A typical system consists of a PCB trace on the line card to the backplane, a backplane interface connector, the trace across the backplane, another backplane connector, and a trace on the switch card. The drive strength-amplitude of the output buffer can be increased to counteract the attenuation caused by these elements, enabling the receiver to determine the signal. The Stratix GX architecture allows the designer to select drive strength between 4mA and 16mA.

Pre-emphasis

Backplane designs must account for high frequency attenuation (also known as IR losses). This is particularly relevant for FR4 fabric due to skin effect. In this situation, the system cannot boost the entire signal because this also boosts any noise or jitter on the line and results in greater power consumption. The system must use signal pre-emphasis, which effectively boosts the high-frequency component of the transmitted signal by emphasizing the first data symbol after any signal transition. Stratix GX devices provide programmable transmission pre-emphasis, allowing the designer to select the level between 0% and 25%, depending on transmission medium and drive length.

Receiver Equalization

Despite transmitter techniques, transmission losses make it difficult to interpret the data as it arrives at the receiver. Receiver equalization can boost the high-frequency signal lost during transmission. As the input signal passes into the receiver, the signal's high-frequency component is boosted before being passed into the receive detector. Receiver equalization is useful where the transmitter is not capable of pre-emphasis or where the signal is transmitted over a long length of lossy material.

The ideal signal setting for a card may be unclear in a backplane design because the card may reside in a number of different locations. The Stratix GX FPGA interface to the transceiver allows certain settings to be modified without a new program file. This allows the designer to have an ideal configuration setting for each slot, allowing parameters for driver strength, pre-emphasis, and equalization to be set during card initialization.

On-device Termination

One issue facing design engineers for high-speed design is channel termination. Traditionally, termination is resolved by adding n external resistors to the transceiver for each channel used. Although this is an acceptable technique, layout difficulty and power overhead make this solution cumbersome. With the introduction of ball grid array (BGA) packaging and the increase in transmission speeds, this scheme is now extremely difficult to implement. Any external resistor must be connected to a line, requiring a stub and increasing noise onto the signal. BGA packaging also means that it is not always possible to keep stub lengths short because resistors may not always be placed close to the pin. Longer stubs increase transmission line issues.

The Stratix GX architecture provides on-chip termination for both the transmitter and receiver, which are configurable on a channel by channel bases. Stratix GX devices support various resistor values and are also capable of providing AC coupling.

Other Stratix Device Features for Backplane Applications

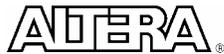
The following Stratix GX devices features also make them ideal for backplane applications:

- Many devices have a limited drive capability restricting their use in backplane applications. In a standard backplane path, the full trace length, including the board traces, the backplane traces, and interconnect, is often over 20". The Stratix GX device is capable of driving in excess of 40" of FR4 fabric at data rates of 3.125 Gbps, making it suitable for most backplane applications
- Stratix GX devices are hot swap capable, making them an ideal solution in applications where line cards would be added or removed without any system downtime.
- Stratix GX devices have a number of built-in test modes, enabling debug of both the internal working of the transceiver via parallel loopback, and also external testing via serial loopback. This simplifies both board testing and debugging during development and system test during installation. The feature also allows for system benchmarking.

Conclusion

Many network-based solutions use the SONET/SDH backplane interface standard. However, interface boundaries and the exact features of the specifications used within the application are usually proprietary. The flexibility of FPGAs makes them an ideal solution for SONET/SDH backplanes because they allow designers to base their designs on common protocols, but also maintain flexibility to support modifications to suit their application. Using programmable logic at the backplane interface also allows easy changes should a different protocol be required in the future.

Stratix GX devices provide the ideal solution due to the embedded features within the transceiver blocks and its advanced FPGA architecture to meet the SONET/SDH specification. The Stratix GX device's flexible buffer also ensures it can overcome many of the transmission effects associated with high speed backplane design.



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