White Paper

Stratix II vs. Virtex-4 Performance Comparison

Altera® Stratix® II devices use a new and innovative logic structure called the adaptive logic module (ALM) to make Stratix II devices the industry's biggest and fastest FPGAs. With the Stratix II ALM architecture, the Quartus® II software can improve the performance of a design by reducing the number of logic levels as well as the routing requirements. The innovative Stratix II logic structure, combined with advanced 90-nm technology from TSMC and the technology leadership of the Quartus II software, allows for a full speed grade performance advantage for Stratix II devices (-3 speed grade, fastest) versus Virtex-4 devices (-12 speed grade, fastest).

Some of the benefits that a high-performance FPGA provides include:

- Reduction in design cycle by meeting a design's performance requirements
- Reduction in cost by using a slower speed-grade device while still meeting the performance goal
- Implementation of high-performance design features that competitive devices cannot support

This white paper provides complete benchmarking data based on an industry expert-endorsed methodology, and detailed architectural analysis demonstrating the technology innovations that provide a performance advantage in Stratix II FPGAs.

Benchmark Methodology

Benchmarking FPGA performance is a complex task, and a poor benchmarking process can result in inconclusive or incorrect results. Altera has invested significantly in developing a rigorous and scientific benchmarking methodology that is endorsed by industry experts as a meaningful and accurate way to measure FPGA device performance. For detailed information on the benchmarking methodology, refer to the *FPGA Performance Benchmarking Methodology White Paper*. Table 1 shows the setup of the experiments.

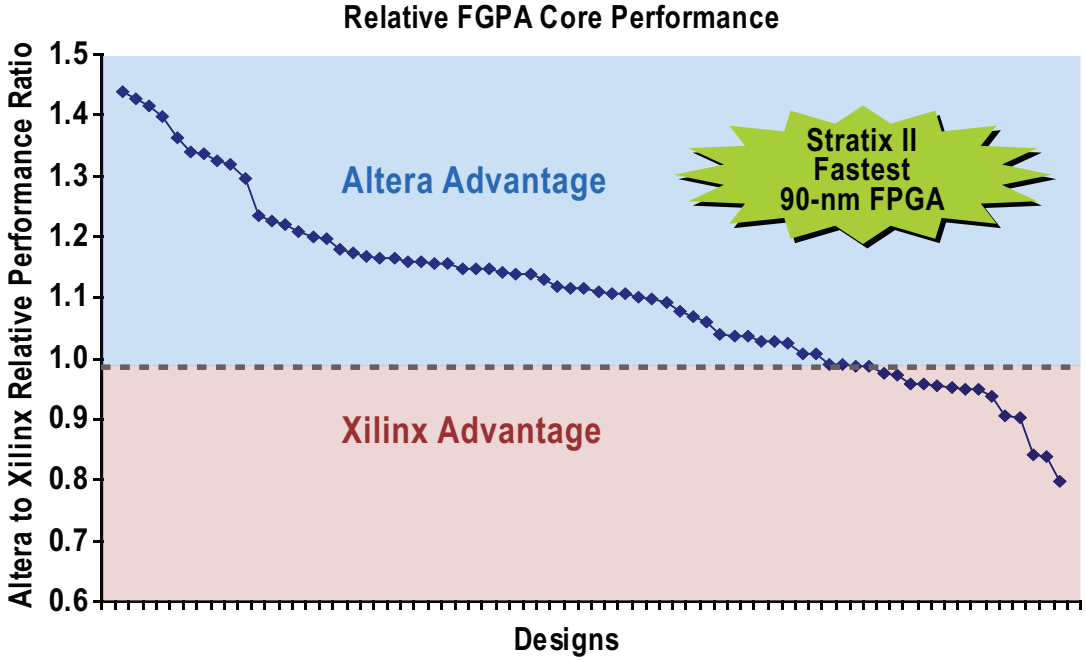
Table 1. Benchmark Setup

FPGA Family	Speed Grade	Synthesis Tool	Place-and Route Tool
Altera Stratix II	-3 (fastest)	Synplify Pro version 8.0	Quartus II software version 5.0
Xilinx Virtex-4	-12 (fastest)	Synplify Pro version 8.0	ISE version 7.1i SP1

Benchmark Data

Over 70 real-world designs were benchmarked, and the results show that Stratix II FPGAs are **a full speed grade faster** than Virtex-4, proving them to be the fastest FPGAs in the 90-nm process node. The Stratix II devices' revolutionary logic structure, high-performance on-chip features, advanced 90-nm process and industry-leading Quartus II software are instrumental in enabling the Stratix II devices' resounding performance advantage. See Figure 1.

Figure 1. Best-Effort Performance Benchmark Comparison Between Stratix II & Virtex-4 Devices



Architectural Analysis

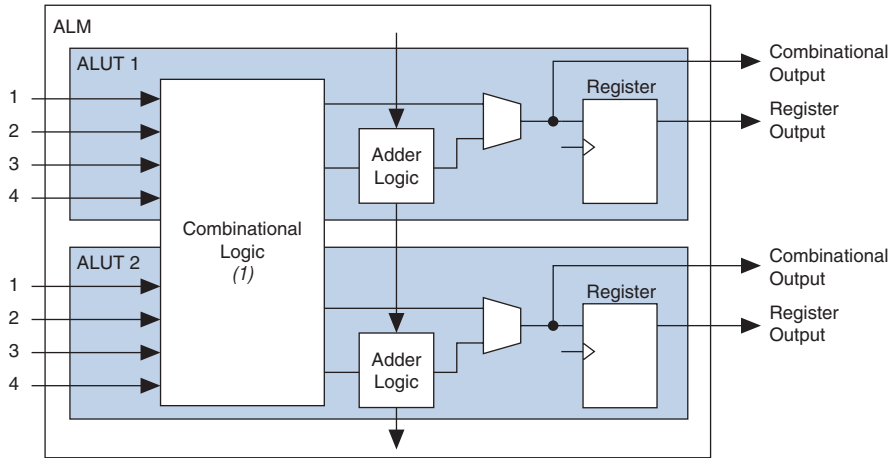
The performance of individual embedded features on an FPGA is important in delivering high system performance. However, if these blocks are not paired with an equally high-performing logic and routing architecture, the individual block's performance does not translate to overall system benefits.

This white paper examines the differences in the logic structure and look-up table (LUT) micro-timing parameters between Stratix II and Virtex-4 devices. The logic structure and LUT parameters represent the bulk of the content in each design and are critical for connecting dedicated features in an FPGA. The analysis is followed by benchmark results and the comparison of simple design building blocks that pin-point how Stratix II architecture improves a design's performance.

Logic Structure Comparison

The Stratix II device logic unit is the ALM. A single ALM contains two adaptive look-up tables (ALUTs), which provide two independent and highly flexible combinational outputs, two adder logic blocks, and two registers. See Figure 2.

Figure 2. Stratix II ALM

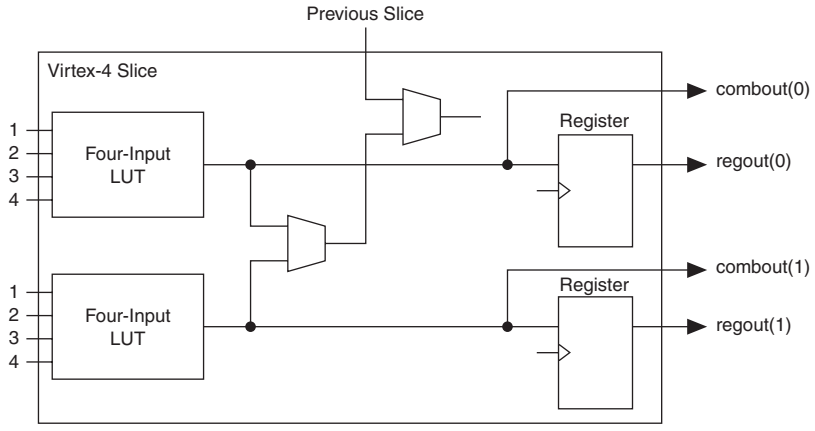


Note to Figure 2:
(1) The combinational logic is adaptively divided between the two ALUTs.

The combinational logic block can be adaptively divided into two LUTs that are either the same or different sizes. For higher performance and reduced area, you can configure an ALM as a large LUT with up to seven inputs. This significantly reduces the logic level and routing delay that impact performance when cascading smaller four-input LUTs. For better logic resource efficiency, you can implement two LUTs of different sizes into a single ALM to reduce the waste of logic resources. The two full adders and the combinational logic block in the ALM provide the ability to combine logic and arithmetic operations into a single level or to perform three-input arithmetic operations for higher performance and less resource usage in arithmetic functions.

The Virtex-4 device logic unit is the slice. A Virtex-4 slice can be divided into two half-slices. Each slice consists of two fixed four-input LUTs, embedded multiplexers, carry logic, and two registers. See Figure 3.

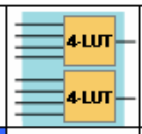
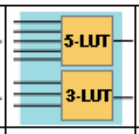
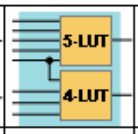
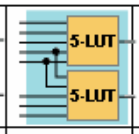
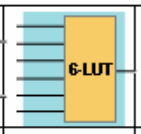
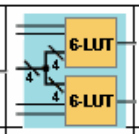
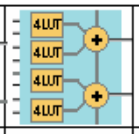
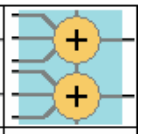
Figure 3. Virtex-4 Slice



To implement functions with greater than four inputs, four-input LUTs are either cascaded together by general routing or combined together using the embedded multiplexers in the slices. In both cases, the speed of the data path is severely impacted by the extra logic levels and routing delays resulting in significant overall circuit performance degradation. In addition, logic resources are wasted because four-input LUTs must be replicated to build larger LUTs

Table 2 compares Stratix II and Virtex-4 implementations of various LUT constructs and arithmetic functions.

Table 2. Stratix II vs. Virtex-4 Implementation Comparison for Various Functions Note (1)

Function								
Stratix II	1 ALM	1 ALM	1 ALM	1 ALM	1 ALM	1 ALM	1 ALM	1 ALM
Virtex-4	1 Slice	1.5 Slices	1.5 Slices	1.5-2Slices	2 Slices	2-4 Slices	1-2 Slices	2 Slices

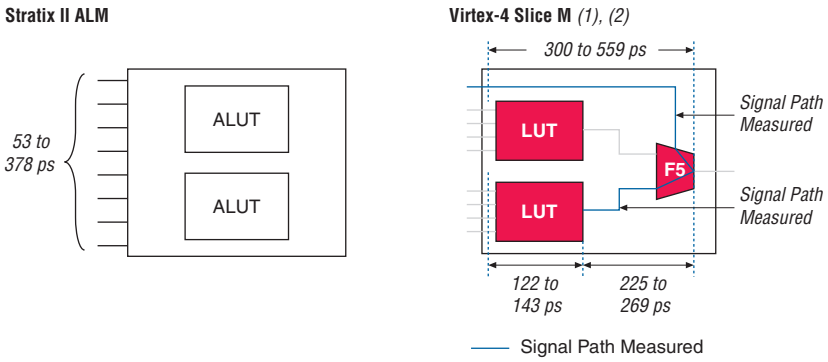
Note to Table 2:
(1) This table applies to Virtex-based devices, including Virtex, Virtex-E, Virtex-II, Virtex II Pro, Virtex-4, Spartan-II, Spartan-IIE, Spartan-3, and Spartan-3E.

LUT Micro Timing Parameter Comparison

Designers can examine the equivalent micro timing parameters between the Stratix II and Virtex-4 LUTs for a good indication of how the logic performance between these FPGA architectures compares.

The Stratix II ALM offers different propagation delays for different inputs. The Altera Quartus II software automatically takes full advantage of this attribute and selects the appropriate ALM inputs so that the circuit's critical path uses the fastest path through the ALM. However, the Virtex-4 slices' LUT delay is the same for each input and the dedicated multiplexers are slower than the LUTs, providing little performance benefit. Figure 4 shows the Stratix II ALM and Virtex-4 slice timing comparison.

Figure 4. Stratix II ALM vs. Virtex-4 Slice M Micro Timing Parameter Comparison



Notes to Figure 4:
(1) This figure does not show the F6, F7 and F8 multiplexers in the Virtex-4 slice because their use requires the data to first pass through the LUT and the F5 multiplexer, resulting in an even larger propagation delay.
(2) The propagation delay range for the Virtex-4 slice is not input dependent. This delay range represents the minimum and maximum value for the associated path.

Design Building Blocks

A set of simple design blocks that commonly appears in real designs is benchmarked and compared between the Stratix II and Virtex-4 devices. This section provides a detailed analysis of these designs and the benchmark result summary.

Generic Six-Input Function

Each Stratix II ALM can be configured to represent any six-input function. A six-input function in a Virtex-4 slice takes as much as two slices and three logic levels. As a result, the Stratix II implementation offers a 40% to 92% reduction in propagation delay, depending on which ALM input is used for the critical path. The Quartus II software automatically places the critical path on the fastest LUT input for the best system performance. Figure 5 shows the implementation comparison. Table 3 compares the logic usage between Stratix II and Virtex-4 devices for a six-input function.

Figure 5. Six-Input Function Implementation Analysis

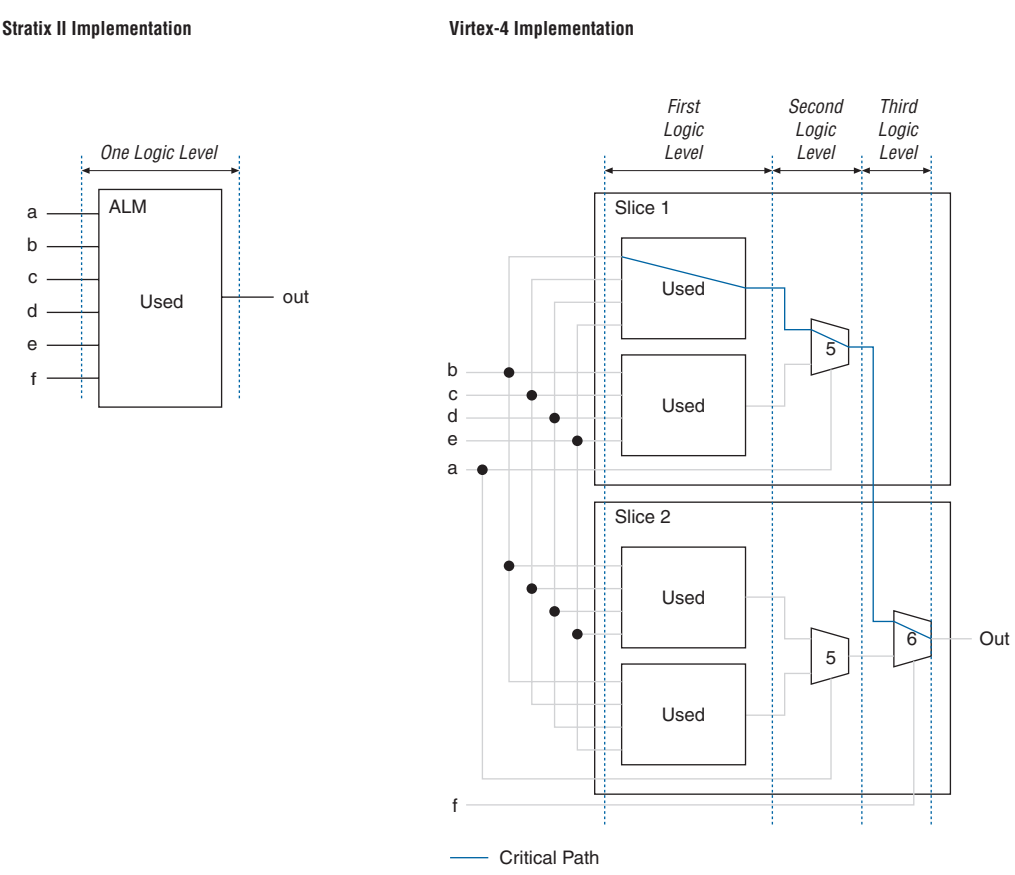


Table 3. Six-Input Function Logic Usage

Parameter	Stratix II Device	Virtex-4 Device	Altera Advantage
Logic levels	1	3	67%
Propagation delay	53 to 378 ps	629 ps	40% to 92%
Logic resource	One ALM	Two slices	50%

If-Then-Else Function

Another common wide function is the cascaded if-then-else statement in the HDL code. The Stratix II logic structure is designed to fit these conditional statements into a single ALM, eliminating extra logic levels and routing delays. Four-input LUTs in Virtex-4 slices need to be cascaded to implement the same function. Figure 6 shows the RTL view of this example. (The source code for this example is available in the Appendix). The results in Figure 7 and Table 4 show that Stratix II devices reduce the logic delay by up to 91% and at least 39% when the design uses the fastest LUT path.

Figure 6. Seven-Input If-Then-Else Function RTL View

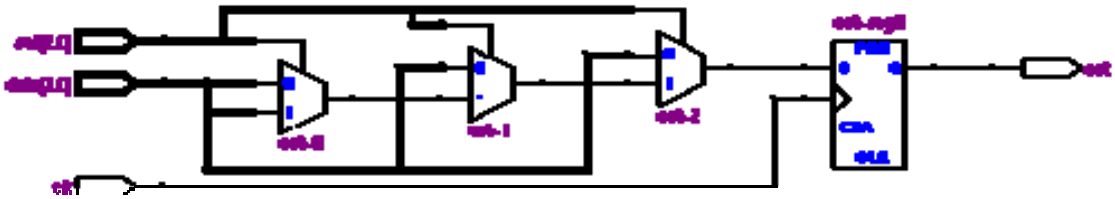


Figure 7. Seven-Input If-Then-Else Function Implementation Analysis

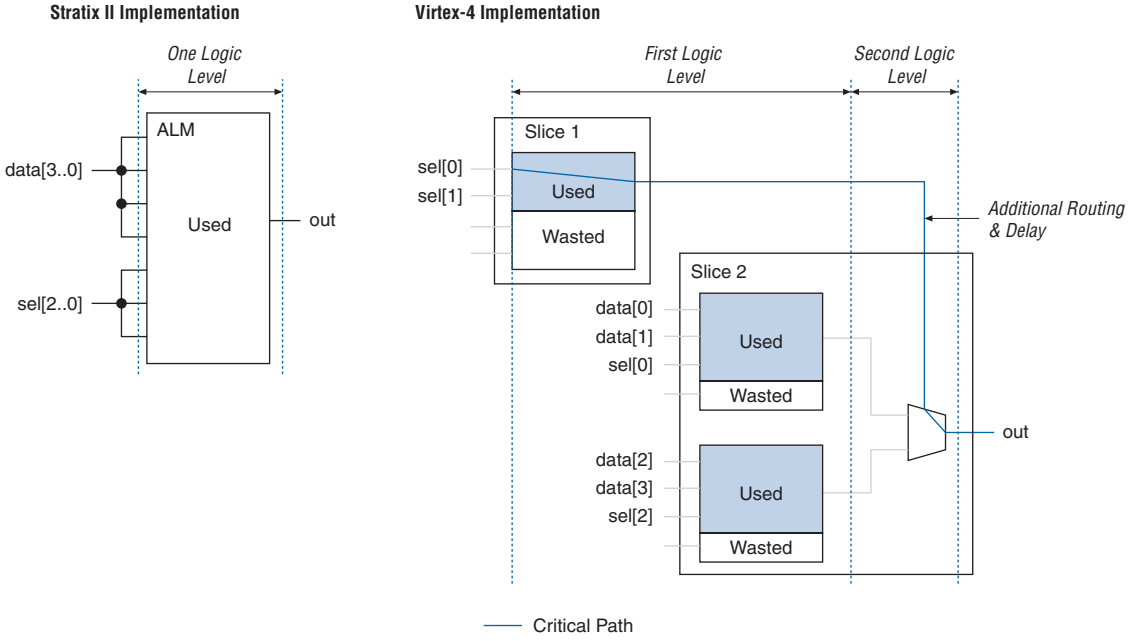


Table 4. Seven-Input If-Then-Else Function Logic Usage

Parameter	Stratix II Device	Virtex-4 Device	Altera Advantage
Logic levels	1	2	50%
Propagation delay	53 to 378 ps	623 ps	39% to 91%
Logic resource	One ALM	1.5 slices	33%

16-Bit Barrel Shifter Comparison

To implement a 16-bit barrel shifter, Stratix II ALMs are configured as six-input LUTs handling the two-stage data multiplexing. Compared to the Virtex-4 implementation, the Stratix II device provides a 50% reduction in logic levels, resulting in twice the performance. In addition to the performance gain, Stratix II devices use only 19 ALMs, while Virtex-4 devices use 34 slices. See Figure 8 and Table 5 for logic usage.

Figure 8. 16-Bit Barrel Shifter Implementation Analysis

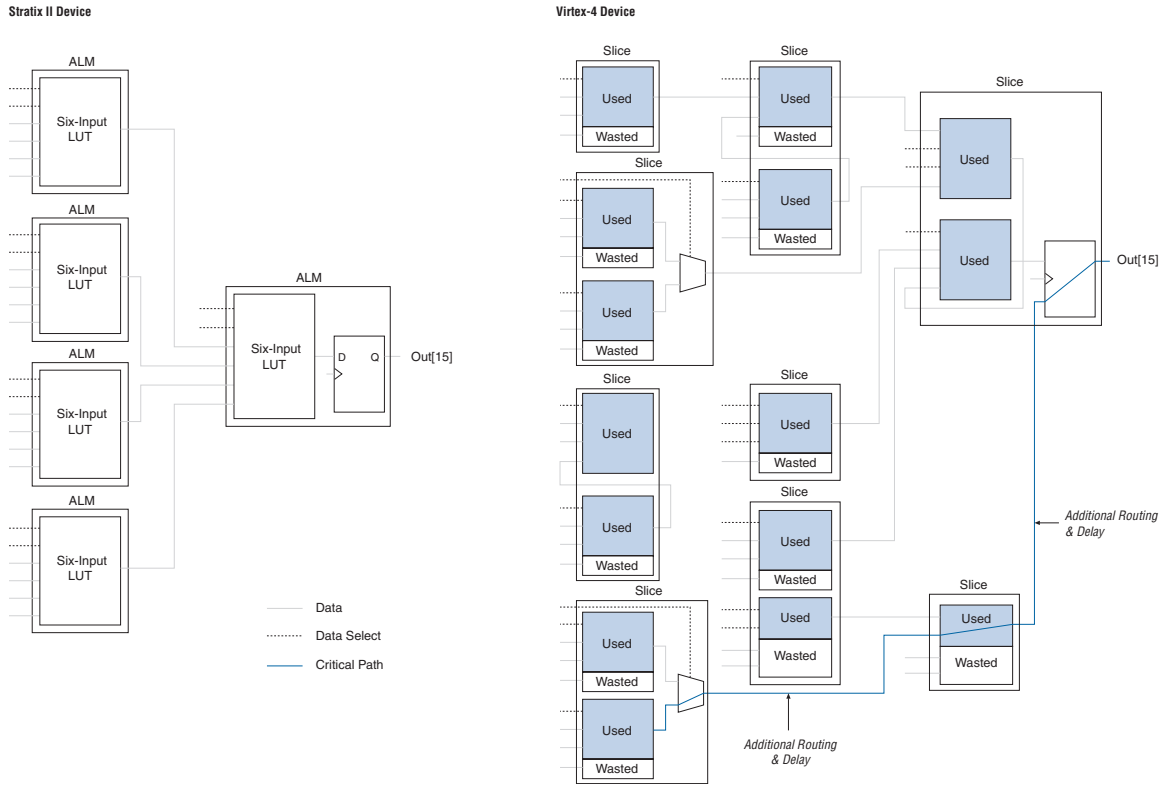


Table 5. 16-Bit Barrel Shifter Logic Usage

Parameter	Stratix II Device	Virtex-4 Device	Altera Advantage
Logic levels	2	4	50%
Propagation delay	1,621 ps	3,050 ps	47%
Logic resource	19 ALMs	34 slices	44%

16-Bit 128-Input Adder Comparison

Adder trees are often found in DSP applications. For example, adders are used in the correlators of 3G wireless base-station channel cards and in the partial-product summation in the logic element (LE)-based multipliers. By offering three-input arithmetic functions, Stratix II ALMs improve performance and reduce the logic resources needed for adder trees. Figure 9 shows that Stratix II three-input summation reduces the adder tree height by 29% and the propagation delay by 19%, while reducing the logic resource usage by 44% when compared to Virtex-4 devices' binary-tree implementation.

Figure 9. 16-Bit 128-Input Adder Tree Implementation Analysis

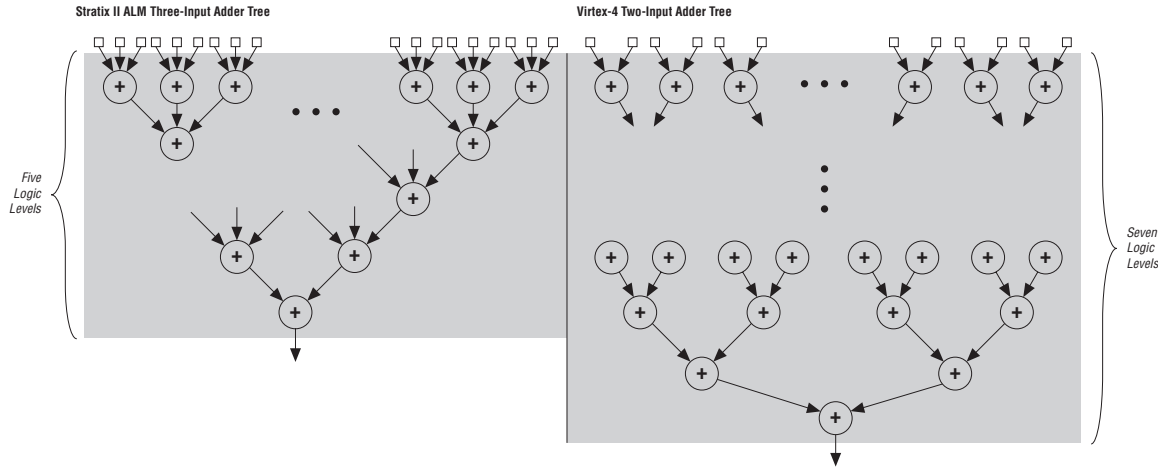


Table 6. 16-Bit 128-Input Adder Tree Logic Usage

Parameter	Stratix II Device	Virtex-4 Device	Altera Advantage
Logic levels	5	7	29%
Propagation delay	8,992 ps	11,050 ps	19%
Logic resource	605 ALMs	1,080 slices	44%

Building Block Design Summary

Table 7 shows the performance and logic utilization summary for different building blocks.

Table 7. Design Building Block Performance & Logic Utilization Comparison Between Stratix II & Virtex-4 FPGAs

Design	Description	Propagation Delay (ps)		Logic Utilization	
		Stratix II	Virtex-4	Stratix II (ALM)	Virtex-4 (Slice)
Five-input function	Two generic five-input logic functions.	53 to 378	334	1	2
Six-input function	Generic six-input logic function.	53 to 378	629	1	2
Seven-input function	Nested if-then-else function.	53 to 378	623	1	1.5
16-bit barrel shifter	16-bit single directional barrel shifter.	1,621	3,050	19	34
16-bit, 128-input adder	128-input adder tree without pipeline. Each input is 16-bit wide.	8,992	11,050	605	1,080

Note to Table 7:
(1) Logic utilization excludes the ALM or slice's input and output register (flip flop) usage.

DSP IP Core Benchmark Data

In addition to the experiments using real-world designs across different market segments, Altera also conducted tests to compare the Stratix II and Virtex-4 FPGA performance when implementing DSP functions. The DSP benchmark includes proprietary IP cores from Altera and Xilinx as well as open core designs from www.opencores.org. Stratix II devices achieved an average of 1.2×, and up to 1.8× higher DSP performance than Virtex-4 devices. For detailed information on the DSP benchmarking methodology and the results, refer to *FPGAs for High-Performance DSP Applications White Paper*.

Quartus II Design Software

The revolutionary ALM architecture was developed along simultaneously with the Quartus II software, enabling the development tool to provide the easiest access to the Stratix II performance advantages. In addition to the state-of-the-art FPGA place-and-route engine that takes full advantage of Stratix II device resources, the Quartus II software also includes two unique tools to make use of Stratix II FPGA's true performance:

- The industry's only vendor-supplied physical synthesis that optimizes designs at the push of a button (see Figure 10).
- The Design Space Explorer (DSE) automatically seeks the best settings for the best performance or area (see Figure 11).

Figure 10. Quartus II Physical Synthesis User Interface

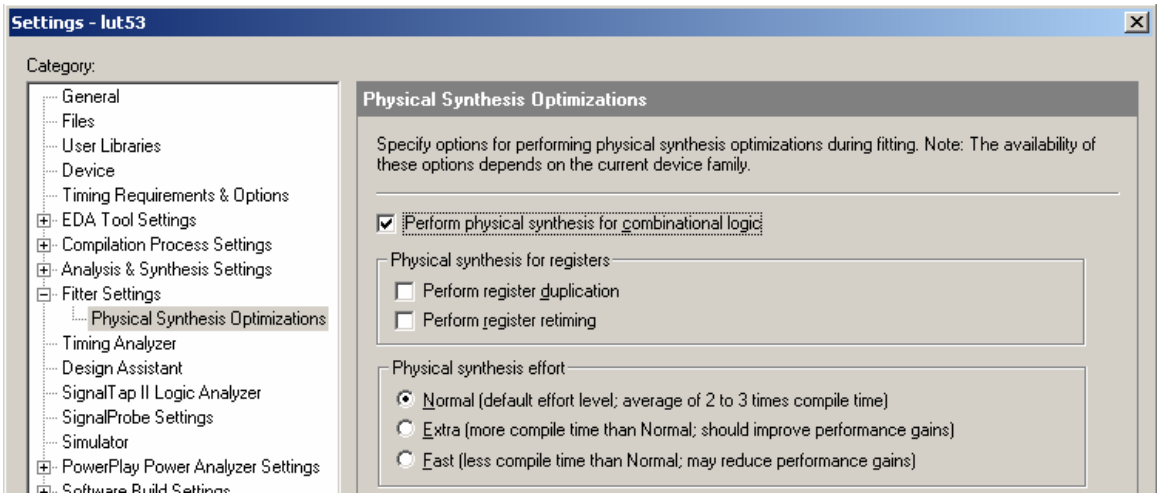
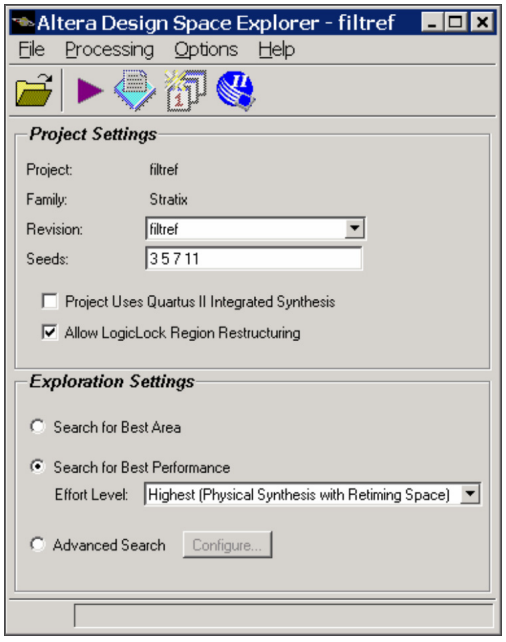


Figure 11. Quartus II DSE User Interface



Conclusion

Stratix II ALMs, routing architecture, embedded features, advanced I/O standards, and external memory interface are well orchestrated by the industry-leading Quartus II software to provide exceptional performance. Based on an industry expert-endorsed benchmarking methodology, Altera benchmarking results show that Stratix II FPGAs are, on average, a full speed grade faster than Virtex-4 devices, making Stratix II devices the fastest FPGAs in the industry.

Appendix

If-Then-Else Example Source Code

```
module lut7(data, sel, out,clk);
  input  [3:0] data;
  input  [2:0] sel; input  clk;
  output out;
  reg out;

  always@ (posedge clk)
  begin
    if (sel[0]) begin
      if (sel[1]) begin
        if (sel[2])
          out=data[2];
        else
          out=data[3];
      end
      else
        out = data[1];
    end
    else
      out = data[0];
  end
endmodule
```

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