Hot-Socketing & Power-Sequencing Feature & Testing for Altera Devices

Introduction

Hot socketing and power-sequence-protection are important for high-availability systems and multi-voltage systems. Hot socketing refers to the ability to insert or remove a board into or out of a system during system operation without causing undesirable effects to the host system or the cards themselves. It is often also referred to as hot swapping or hot plug-in. This feature also allows the PLDs to resume normal operation regardless of the power sequence.

A programmable logic device (PLD) capable of hot socketing must meet the following criteria.

- The device can be driven before power-up without any damage to the device itself.
- The device does not drive out before or during power-up.
- External input signals to the device I/O pins do not power the device's V_{CCIO} or V_{CCINT} power supplies through internal paths of the device.

Altera has a robust design and full support for hot socketing and power sequencing in its advanced FPGA and CPLD devices. This white paper defines the hot socketing feature for FPGA and CPLD devices, discusses their implementations in silicon, and provides characterization work that demonstrates that Altera devices are hot socketable.

This document contains the following sections:

Altera Hot-Socketing & Power-Sequencing Feature Overview

The hot-socketing and power-sequencing feature for Altera FPGA and CPLD devices offers:

- No-hassle, drop-in solution
- No external components or board manipulation are necessary to support hot socketing
- Supported for any power-up sequence
- I/O buffers that are non-intrusive to system buses during hot insertion

Hot-Socketing & Power-Sequencing Feature in FPGA Devices

Altera is the only FPGA vendor offering hot-socketing and power-sequencing support for FPGAs manufactured on a 0.13-µm process. The Stratix, Stratix GX, and Cyclone FPGA families are all based on the 0.13-µm process and each family is designed and has been tested to support hot socketing. Altera will also support the hot socketing feature on devices manufactured on the 90-nm process technology.

WP-HTSCKTNG-1.1

Hot-Socketing & Power-Sequencing Specification for FPGA Devices

Altera's 0.13-µm FPGA devices support hot socketing without requiring any external components. In a hot-socketing situation, a device's output buffers are turned off during system power-up or power-down. Stratix, Stratix GX, and Cyclone devices support any power-up or power-down sequence (V_{CCIO} and V_{CCINT}) to simplify system level design. You can drive signals into the device before or during power-up or power-down without damaging the device. Stratix, Stratix GX, and Cyclone devices will not drive out until the device is configured and has attained proper operating conditions.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF. Altera's 0.13-µm FPGA devices meet the following hot socketing specifications:

The hot socketing DC specification is $| I_{IOPIN} | < 300\ \mu A$

The hot socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less.

This specification takes into account the pin capacitance and not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading needs to be taken into consideration separately.

I_{IOPIN} is the current at any user I/O pin on the device. The DC specification applies when all VCC supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

Hot-Socketing Specification for High-Speed I/O Transceiver Pins on Stratix GX Devices

The high-speed I/O transceiver pins on Stratix GX devices meet the following specifications:

- DC specification for receiver channels is: $| I_{RXPIN} | < 50$ mA
- The hot-socketing AC specification is: $| I_{TXPIN} | < 100$ mA

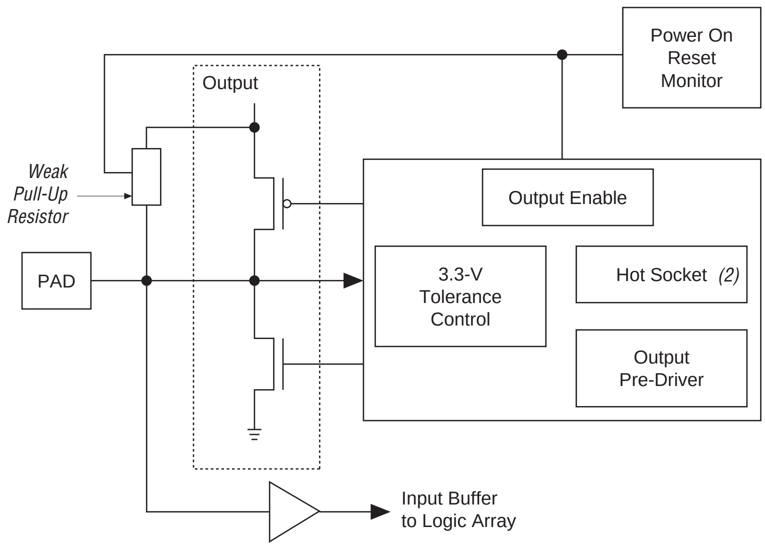
Implementing Hot Socketing & Power Sequencing in FPGA Devices

The fundamental idea behind hot socketing in FPGA devices is to turn off the output buffer during the power-up (either V_{CCINT} or any of the V_{CCIO} supplies) or power down event. The hot-socket circuit will generate an internal `HOTSCKT` signal when either V_{CCIO} or V_{CCINT} is below the threshold voltage. The `HOTSCKT` signal will cut off the output buffer to make sure no DC current (except for leaking current through the weak pull-up resistor) is going through the pin.

When V_{CC} ramps up very slowly, it is still relatively low even after the power-on reset (POR) signal is released and the configuration is finished. If the hot-socketing circuit was implemented on the `CONF_DONE`, `nSTATUS`, and `nCEO` pins, they would fail to respond because the output buffer could not flip from the state set by the hot-socketing circuit at this low V_{CC} voltage. To overcome this issue, the hot-socketing feature is removed on these pins to make sure that the `CONF_DONE`, `nSTATUS`, and `nCEO` pins can operate during configuration. This is expected behavior as these pins are supposed to drive out during power-up and power-down sequences.

Each I/O pin has the circuitry shown in Figure 1.

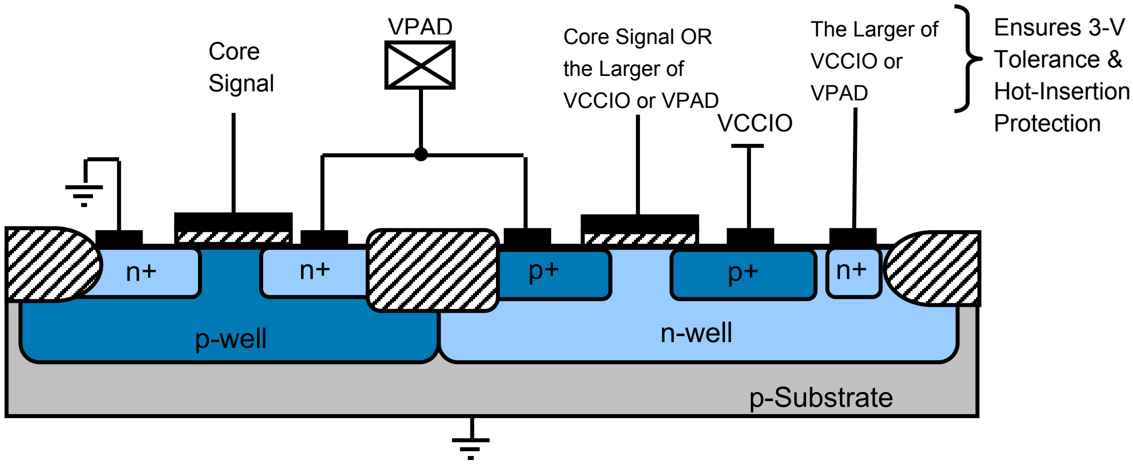
Figure 1. Hot Socketing Circuit Block Diagram for FPGA Devices



The POR circuit monitors V_{CCINT} voltage level and keeps I/O pins tristated until the device is in user mode. The weak pull-up resistor from the I/O pin to V_{CCIO} prevents the I/O pins from floating. The 3.3-V tolerance control circuit allows the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

Figure 2 shows a transistor level cross section of FPGA device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This design also protects the device from sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

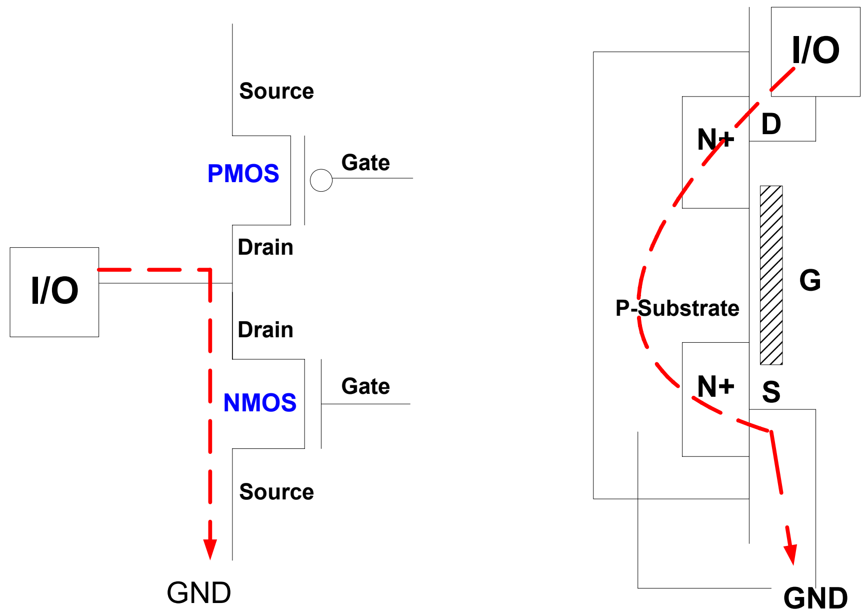
Figure 2. Transistor Level Diagram of FPGA Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electro-static discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turns on to discharge ESD current from I/O pins to GND (see Figure 3).

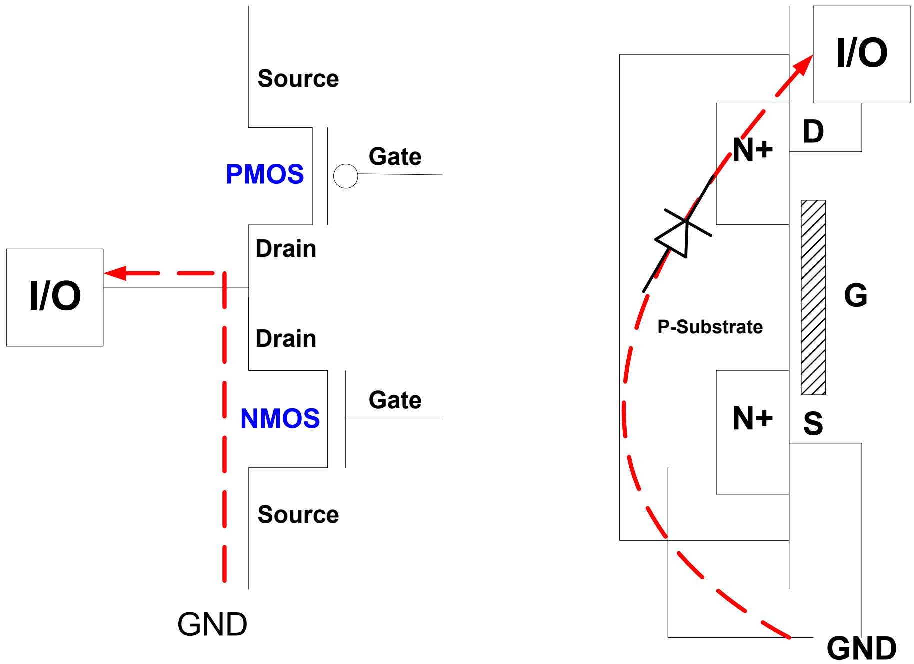
Figure 3. ESD Protection During Positive Voltage Zap



Note to Figure 3:
(1) The dashed line shows the ESD current discharge path during a positive ESD zap.

When the I/O pin receives a negative ESD zap at the pin that is less than -0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Hence, the discharge ESD current path is from GND to the I/O pin as shown in Figure 4.

Figure 4. ESD Protection During Negative Voltage Zap



Hot-Socketing & Power-Sequencing Feature in CPLD Devices

Altera has taken a similar approach to hot socketing support for CPLD devices (MAX 7000AE and MAX 3000A devices) as for the FPGA devices.

Hot-Socketing & Power-Sequencing Specification for CPLD Devices

MAX 7000AE and MAX 3000A devices support hot socketing without any external components. In a hot-socketing situation, a device's output buffers are turned off during system power-up. MAX 7000AE and MAX 3000A devices support any power-up sequence to simplify system level design. You can drive signals into the device before or during power-up without damaging the device. MAX 7000AE and MAX 3000A devices will not drive out until the device is configured and reaches proper operating conditions.

The hot-socketing DC specification ($|I_{IOPIN}| < 300\ \mu A$) is for the worst case current on any I/O pin during hot socketing and power up.

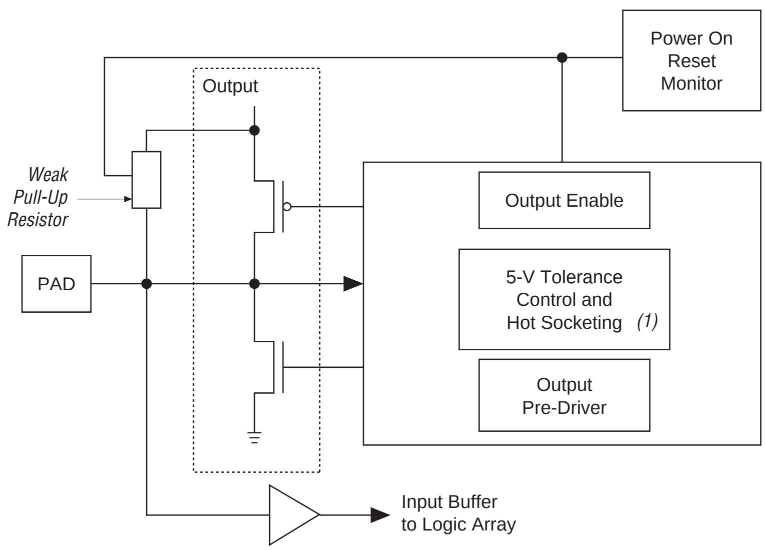
I_{IOPIN} is the current at any user I/O pin on the device.

☞ Fast V_{CCINT} rise times during power up may lead to a short high or low pulse on I/O pins. This is documented and explained in the MAX 7000AE, MAX 7000B, and MAX 3000A Devices Errata Sheet.

Hot-Socketing & Power-Sequencing Feature Implementation in CPLD Devices

Each I/O pin has the circuitry shown in Figure 5.

Figure 5. Hot Socketing Circuit Block Diagram for CPLD Devices

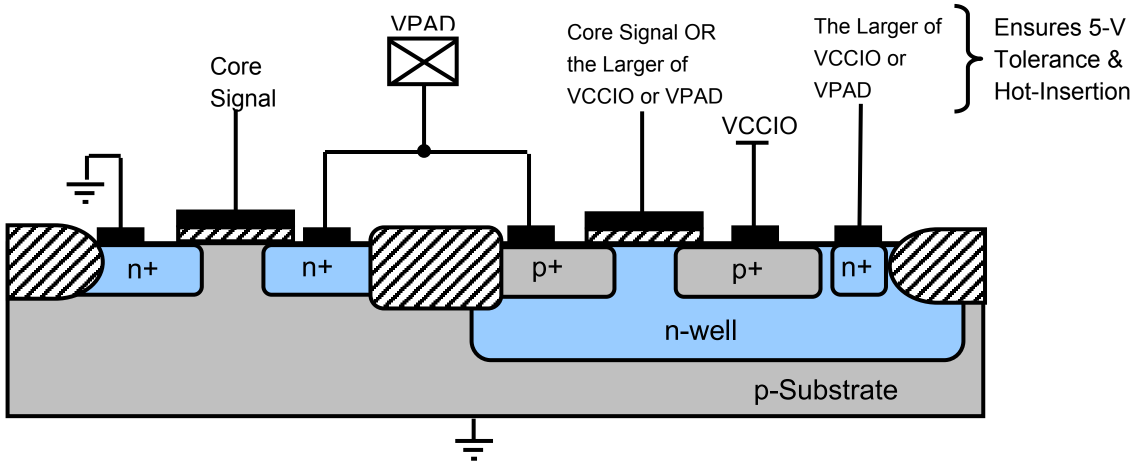


Note to Figure 5:
(1) The OE1 and GCLRn pins in MAX 7000AE and MAX 3000A CPLDs may be driven up to 3.6 V during hot socketing. After V_{CCINT} and V_{CCIO} reach the recommended operating conditions, these pins are 5.0-V tolerant.

The POR circuit monitors the V_{CCINT} voltage level and keeps I/O pins tri-stated until the device is in user mode. The weak pull-up resistor from the I/O pin to the VCCIO pin is present to keep the I/O pins from floating. The 5-V tolerance control circuit allows the I/O pins to be driven by 5.0 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not in user mode. The hot socket circuitry prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

Figure 6 shows a transistor level cross section of the I/O buffer for MAX 7000AE and MAX 3000A devices. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. There is no current path from signal I/O pins to V_{CCINT} or V_{CCIO} during hot insertion. The V_{PAD} leakage current charges the 5.0-V tolerant circuit capacitance.

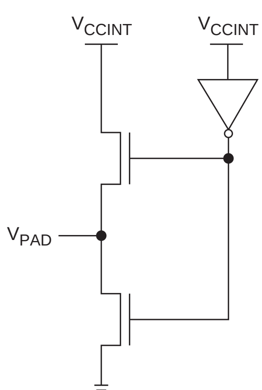
Figure 6. Transistor Level Diagram of CPLD Device I/O Buffers



The two NMOS output drivers (shown in Figure 7) in the I/O pins provide ESD protection. When V_{CCINT} is powered, the transistors shut off. Therefore, there is no path for current to flow between the VCCINT and ground pins.

When V_{CCINT} is 0 V, the transistors are highly resistive to provide ESD protection. Current does not flow from the VPAD pin to the VCCINT pin, even when V_{PAD} is 5.0 V.

Figure 7. ESD Protection Circuitry in CPLD Devices



Hot-Socketing & Power-Sequencing Testing for Stratix & Cyclone Devices

This section provides information on how Altera tested the hot-socketing feature in Stratix and Cyclone devices.

Test Conditions

The conditions used for the test are:

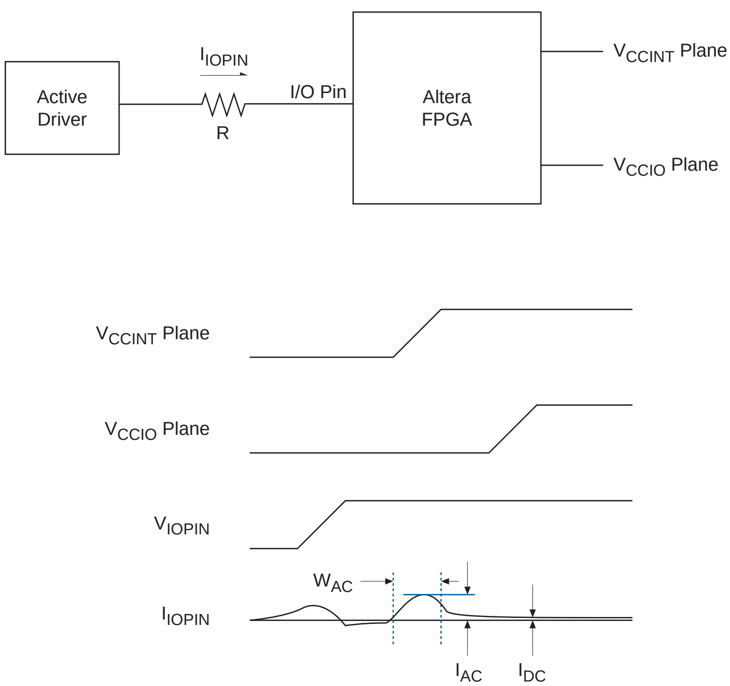
- Temperature: -40° C, 130° C
- V_{CCINT} = 0 to 1.575 V
- V_{CCIO} = 0 to 3.6 V
- V_{IOPIN} = 0 to 3.6 V

Test Setup

The setup for the hot socketing test is shown in Figure 8. The pin being tested is connected to an active driver through a power resistor or current probe. The current through the pin can be calculated from the voltage across the resistor or reading the value from the current probe. Current through the pin will indicate that the pin is driving out. The I/O pins are tri-stated during hot socketing conditions because the device is not yet configured. The circuitry in the I/O pin keeps the pins tri-stated.

One of the six possible sequences of V_{CCINT}, V_{CCIO}, and V_{IOPIN} is shown in the Figure 8 with an example measurement of current on the pin.

Figure 8. Hot-Socketing Test Setup



V_{CCINT}, V_{CCIO}, and V_{IOPIN} are sequenced in six different combinations for all of the different types of pins (LVDS input pin, LVDS output pin, dedicated input pin, regular I/O pin).

Test Results

Table 1 shows the tested combinations and test results for the Stratix and Stratix GX I/O pins (except for transceiver pins). A passing result indicates that the hot-socketing specification is met.

Table 1. Stratix & Stratix GX Hot-Socketing Test Conditions & Results

Pin Type	Power-Up Sequence			Pass or Fail
	First	Second	Third	
DIFFIO_RX	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass
DIFFIO_TX	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass
CLK pins	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass
I/O pins	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass

Table 2 shows the tested combinations and test results for the Cyclone devices. A passing result indicates that the hot-socketing specification is met.

Table 2. Cyclone Hot-Socketing Test Conditions & Results

Pin Type	Power-Up Sequence			Pass or Fail
	First	Second	Third	
CLK0	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass
DQ0L7	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass
DQ0T1 and LVDST1	V_{CCIO}	V_{CCINT}	V_{IOPIN}	Pass
	V_{CCIO}	V_{IOPIN}	V_{CCINT}	Pass
	V_{CCINT}	V_{CCIO}	V_{IOPIN}	Pass
	V_{CCINT}	V_{IOPIN}	V_{CCIO}	Pass
	V_{IOPIN}	V_{CCIO}	V_{CCINT}	Pass
	V_{IOPIN}	V_{CCINT}	V_{CCIO}	Pass

Hot-Socketing & Power-Sequencing Testing for Stratix GX Transceiver I/O Pins

This section provides information on how Altera tested the hot-socketing feature in Stratix GX devices.

Test Conditions

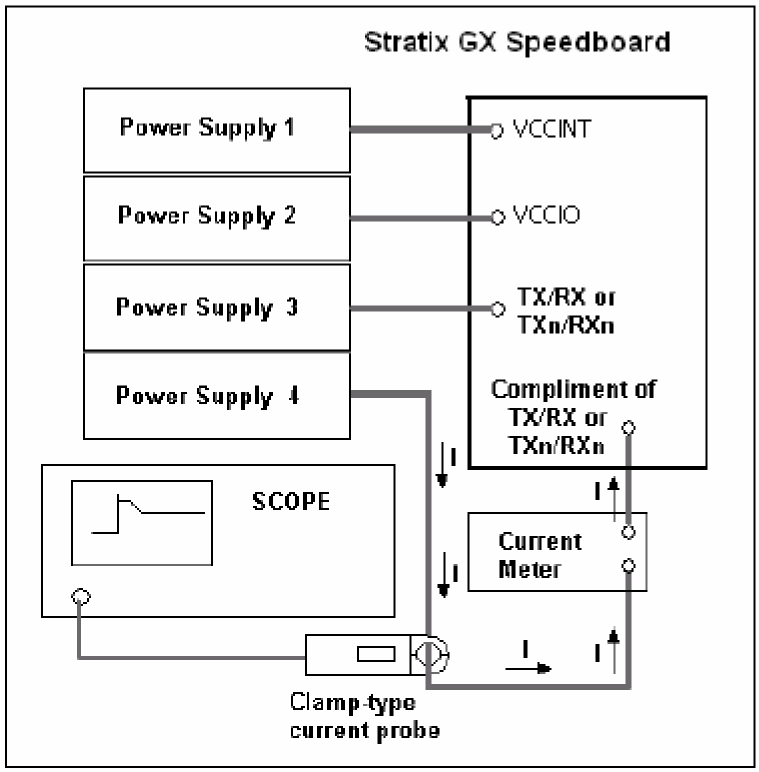
The conditions used for the test are:

- Device: EP1SGX25 Rev B
- Temperature: -40° C, 25° C, 100° C
- V_{CCINT}: = 0 to 1.5 V
- V_{CCIO}: = 0 to 3.3 V
- V_{IOPIN}: = 0 to 3.3 V
- Single Channel

Test Setup

Transceiver pins were tested using the following test setup shown in Figure 9.

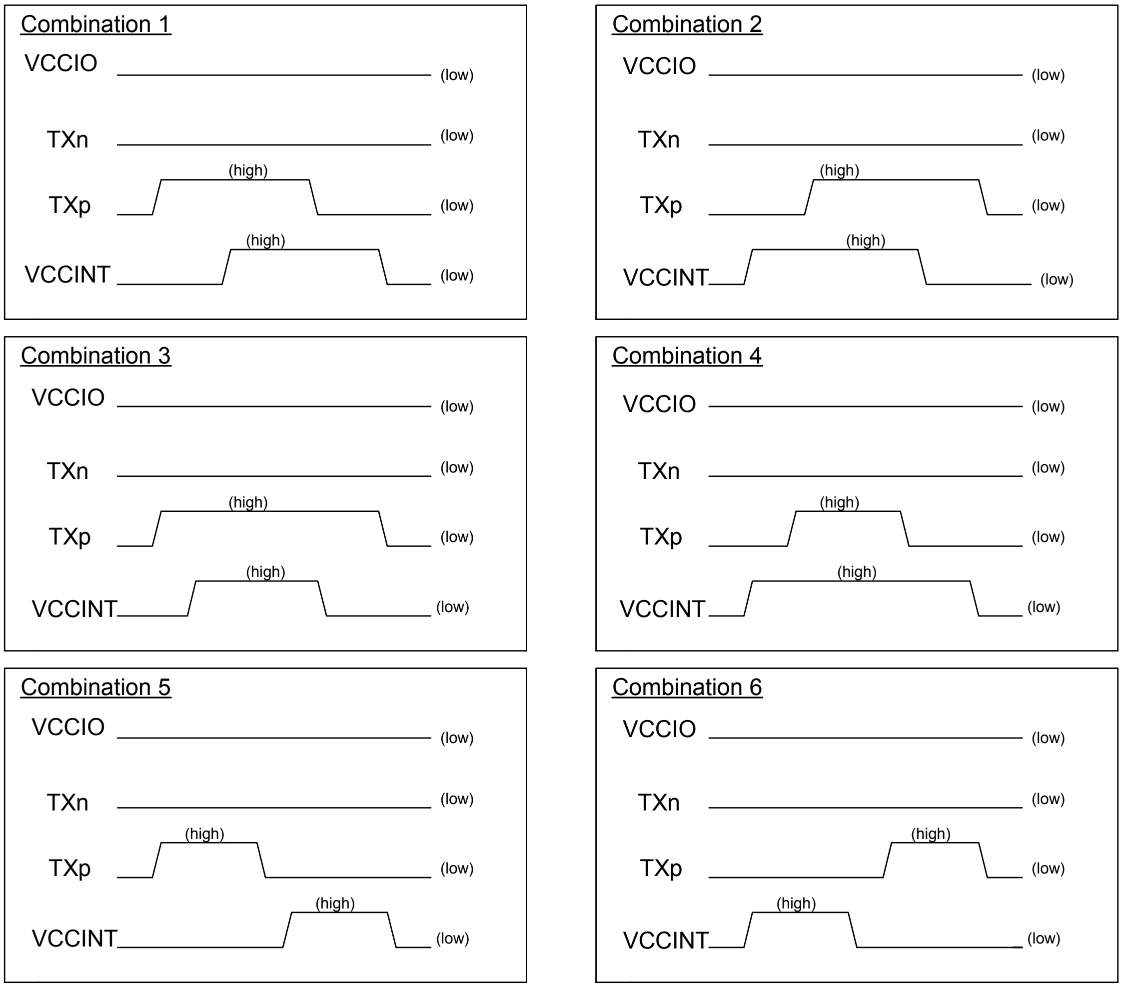
Figure 9. Stratix GX Test Setup for Hot Socketing



Test Cases

The following cases were tested with the transmitter and receiver pins to take into consideration power sequencing for V_{CCINT} and V_{CCIO} power supplies.

Figure 10. Combination of TXp Hot Socket Measurement with Low V_{CCIO} & Low TXn (1), (2)

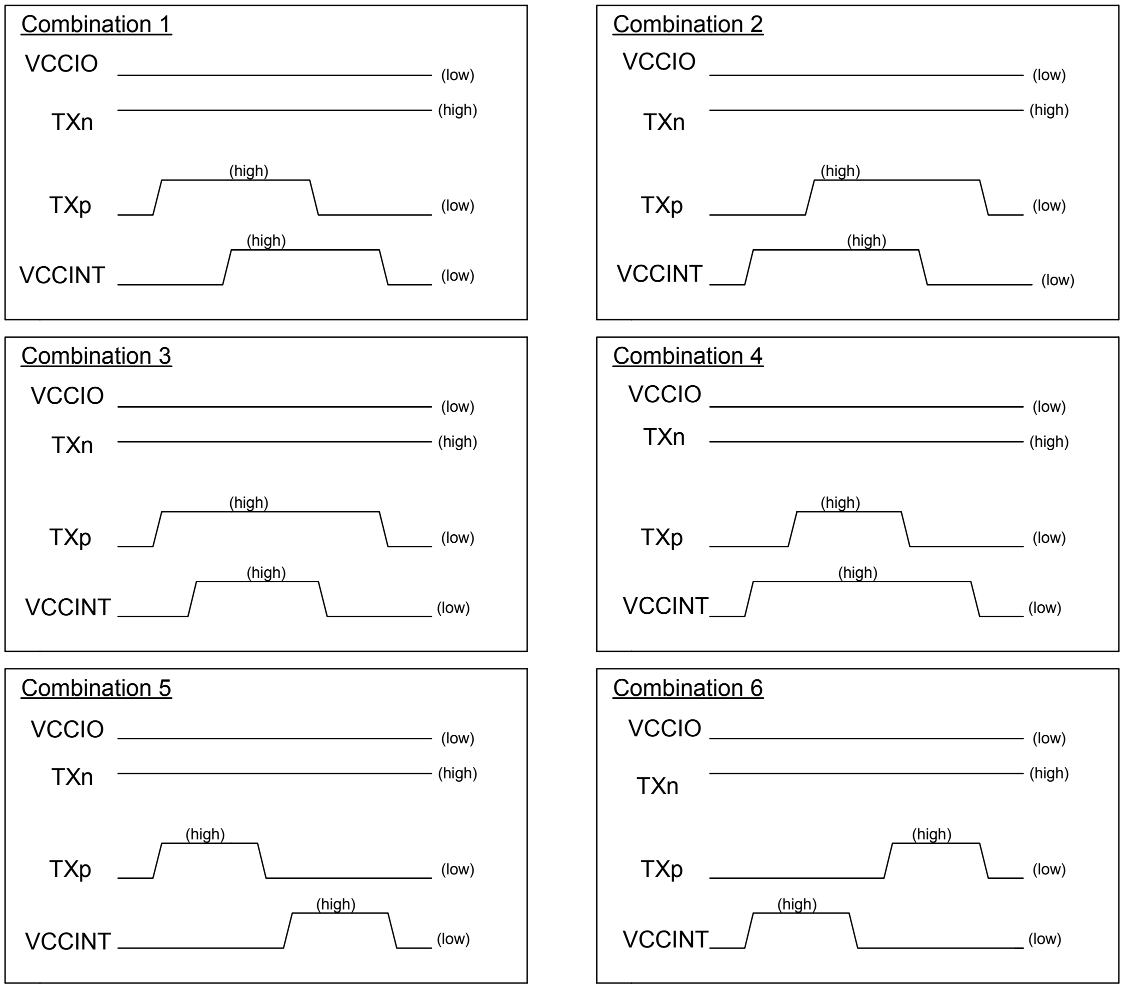


Notes to Figure 10:

(1) These pulses are generated externally by the power supplies shown in Figure 9.

(2) These are the test cases that were used to generate the test results shown in Table 3.

Figure 11. Combination of TXp Hot Socket Measurement with Low V_{CCIO} & High TXn (1), (2)

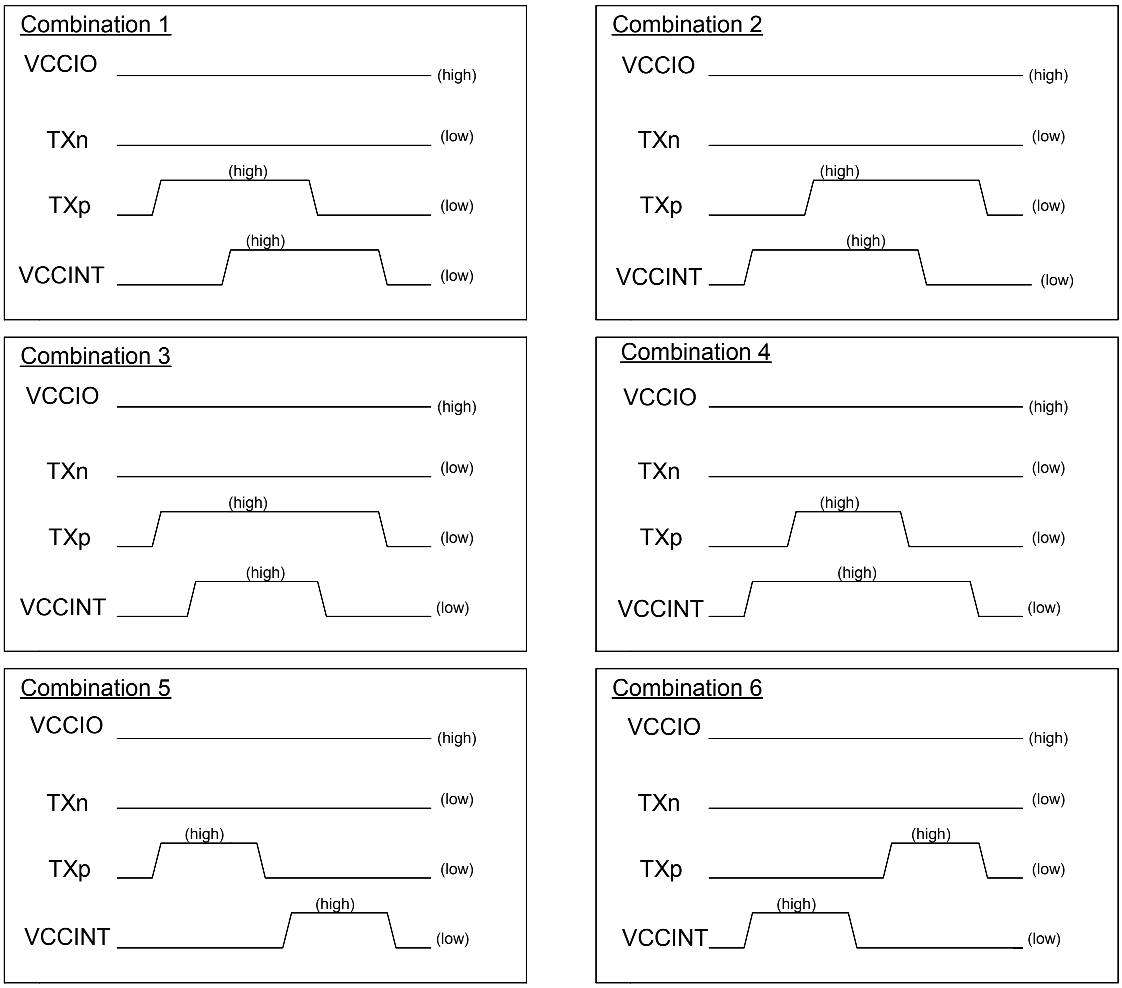


Notes to Figure 11:

(1) These pulses are generated externally by the power supplies shown in Figure 9.

(2) These are the test cases that were used to generate the test results shown in Table 3.

Figure 12. Combination of TXp Hot Socket Measurement with High V_{CCIO} & Low TXn (1), (2)

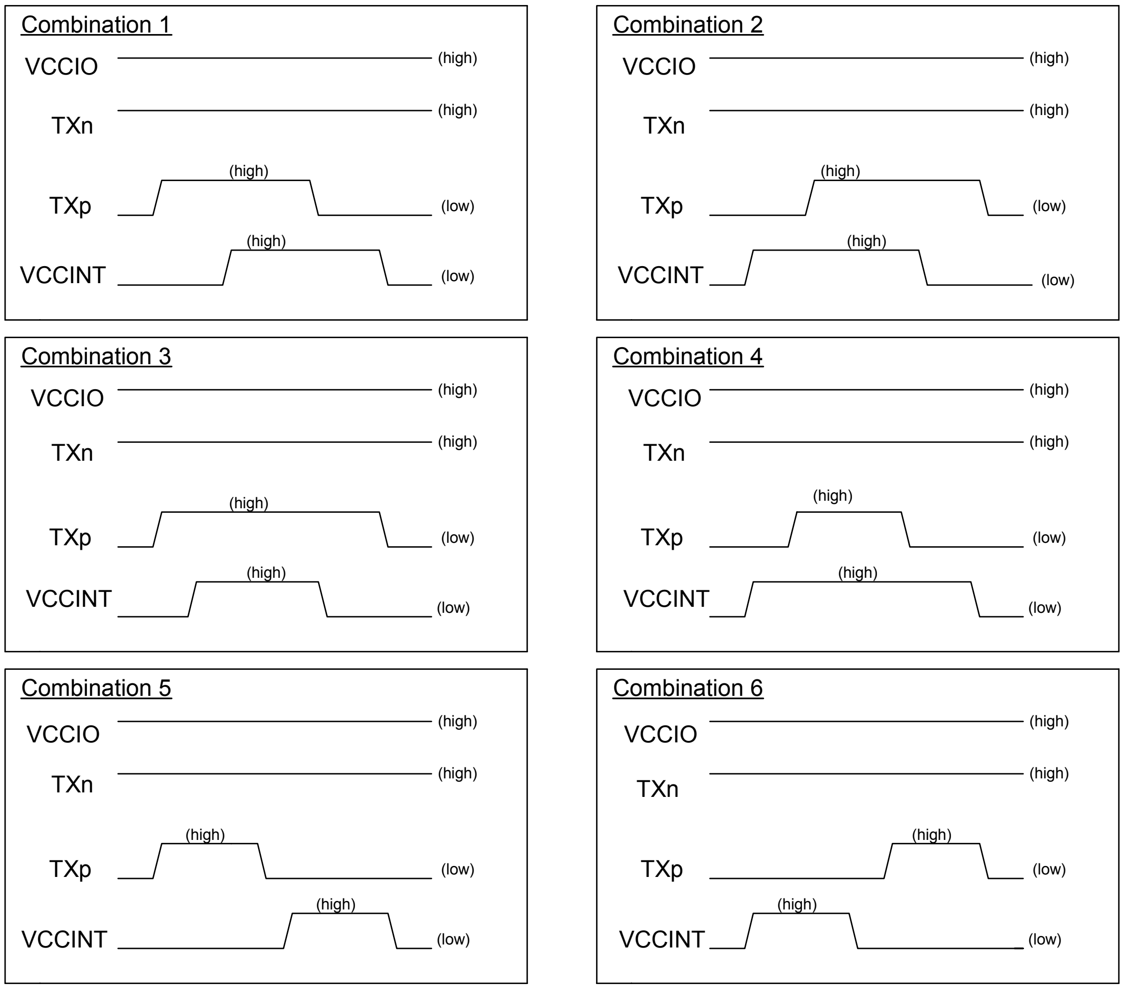


Notes to Figure 12:

(1) These pulses are generated externally by the power supplies shown in Figure 9.

(2) These are the test cases that were used to generate the test results shown in Table 3.

Figure 13. Combination of TXp Hot Socket Measurement with High V_{CCIO} & High TXn (1), (2)



Notes to Figure 13:

(1) These pulses are generated externally by the power supplies shown in Figure 9.

(2) These are the test cases that were used to generate the test results shown in Table 3.

Test Results

Table 3 shows the test results.

Table 3. Stratix GX High-Speed Transceiver I/O Pin Hot-Socketing Test Results			
Test	**Temperature**		
	-40° C	**25° C**	**100° C**
Transceiver Max Steady State Current (mA)	18.68	20.1	12.16
Receiver Max Steady State Current (mA)	48.83	44.04	47.99

Hot-Socketing & Power-Sequencing Testing for CPLD Devices

This section provides information on how Altera tested the hot-socketing feature in CPLD devices.

Test Conditions

The conditions used for the test are:

- Device: EPM7128AE device
- V_{CCINT} = 0 to 3.3 V
- V_{CCIO} = 0 to 3.3 V
- V_{IOPIN} = 0 to 3.3 V

CPLD devices are EEPROM devices, which are non-volatile. Therefore, the device is programmed before the testing to simulate a real application and is not blank. The I/O pins on a blank device are tristated until programming is complete. The behavior of the I/O pins can be programmed to be tristated, driving a signal, or driving GND. For this testing, the I/O pins were programmed to be tristated to identify if the device was driving out during hot-socketing conditions.

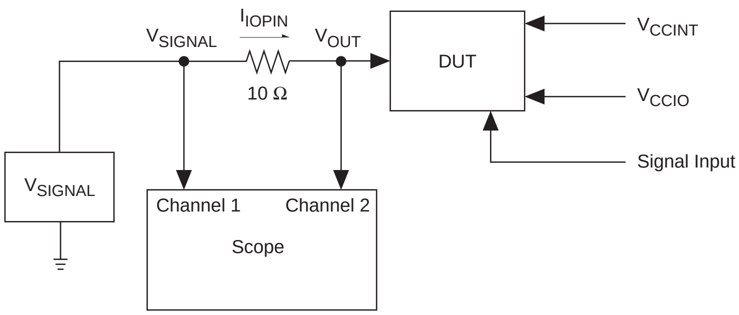
The following test cases were tested:

- Case1: V_{SIGNAL} (3.0 V) => V_{CCINT} (3.0 or 0.0 V) => V_{CCIO} (ramp)
- Case2: V_{SIGNAL} (3.0 V) => V_{CCIO} (3.0 or 0.0 V) => V_{CCINT} (ramp)
- Case3: V_{SIGNAL} (3.0 V) => V_{CCINT} and V_{CCIO} (ramped simultaneously)

Test Setup

The setup for the hot-socketing test is showed in Figure 14. The V_{SIGNAL} voltage supply applies a voltage through a resistor to an I/O pin on the MAX device. The current through the pin can be calculated from the voltage across the resistor probe or by measuring it with a current. Channel 1 (yellow) and channel 2 (pink) monitor the voltage drop across the resistor with an oscilloscope. If the two traces are not the same (overlapping), then the device is driving out.

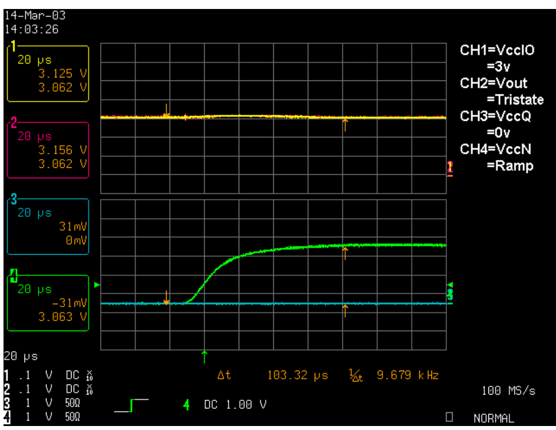
Figure 14. Test Setup for CPLD Devices



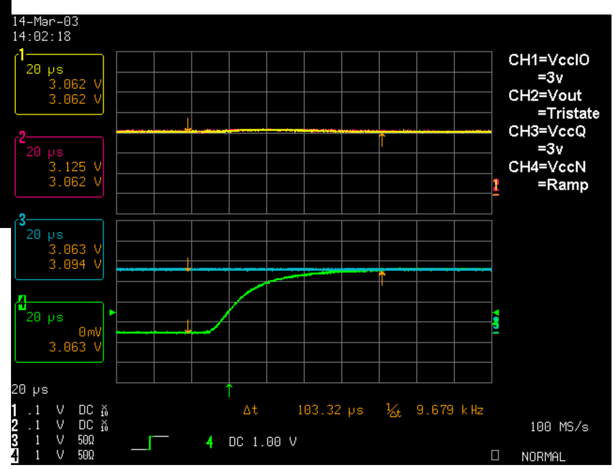
Test Results

Figures 15 through 17 show the results from the CPLD tests.

Figure 15. Case 1, V_{SIGNAL} (3 V) => V_{CCINT} (3 or 0 V) => V_{CCIO} (ramp) Notes (1), (2)



- Device Is Tri-Stated During Power-Up & Operation
- No Current Flow & Voltages at V_{SIGNAL} & V_{OUT} Match

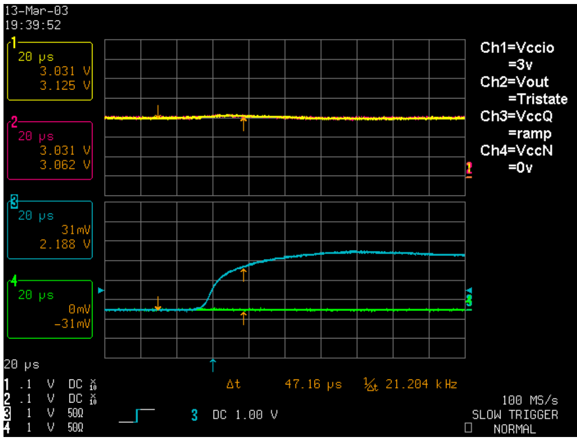


Notes to Figure 15:

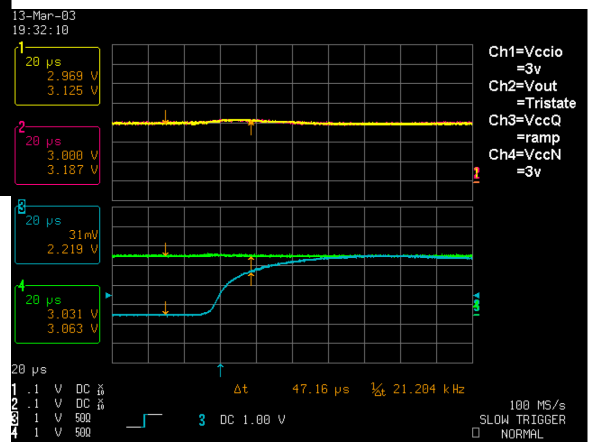
(1) $V_{CCQ} = V_{CCINT}$, $V_{CCN} = V_{CCIO}$

(2) V_{OUT} is the I/O pin on the device

Figure 16. Case 2, V_{SIGNAL} (3 V) => V_{CCIO} (3 or 0 V) => V_{CCINT} (ramp) *Notes (1), (2)*



- In All Conditions, the Device has V_{SIGNAL} Matching V_{OUT}
- Device is Properly Tri-Stated

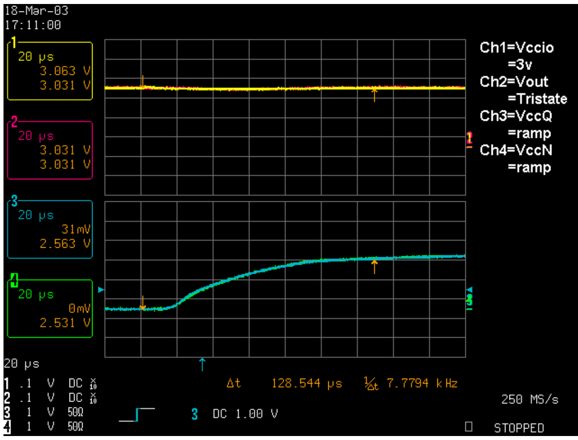


Notes to Figure 16:

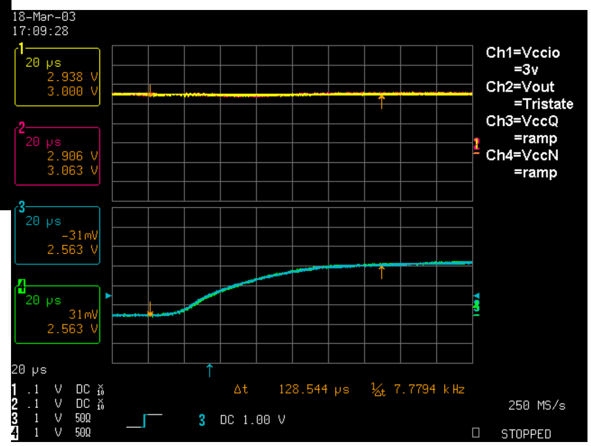
(1) $V_{CCQ} = V_{CCINT}$, $V_{CCN} = V_{CCIO}$

(2) V_{OUT} is the I/O pin on the device

Figure 17. Case3: V_{SIGNAL} (3 V) => V_{CCINT}/V_{CCIO} (ramped simultaneously) *Notes (1), (2)*



■With a Tri-Stated Device, no Current Flow in Either Case



Notes to Figure 17:

(1) $V_{CCQ} = V_{CCINT}$, $V_{CCN} = V_{CCIO}$

(2) V_{OUT} is the I/O pin on the device

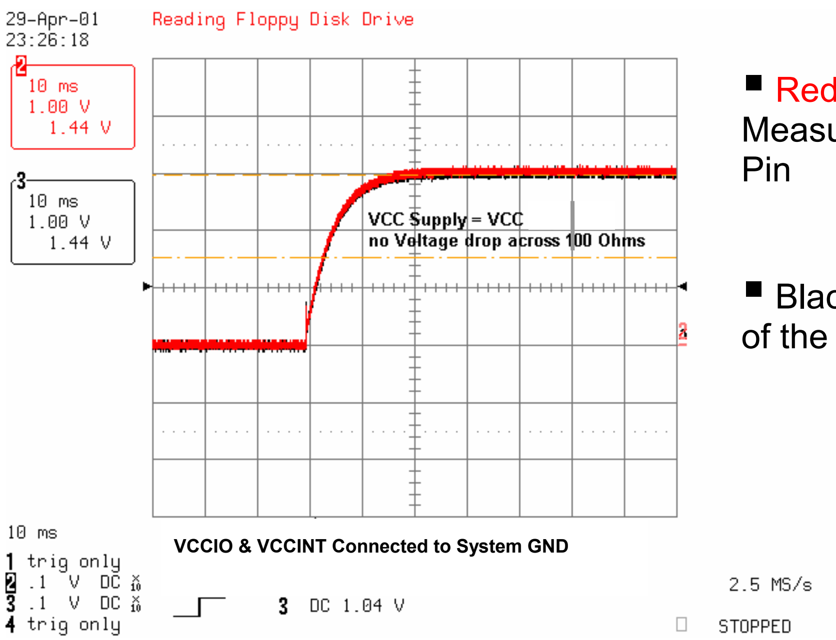
Conclusion

Altera's Stratix, Stratix GX, Cyclone, MAX 7000AE, and MAX 3000A devices are designed for and fully tested to support hot socketing in a multi-voltage system where power supply sequences are not specified. These devices adhere to the hot socketing specifications within this document. The power-up sequence no longer dictates the proper functionality of Altera's PLDs.

Appendix

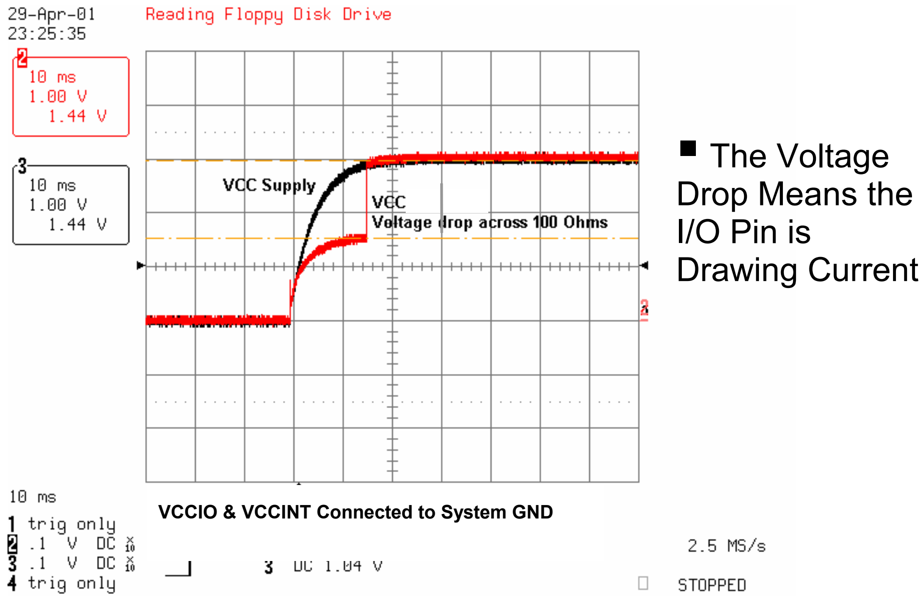
Figures 18 and 19 show examples of passing and failing scope shots, respectively.

Figure 18. Example Scope Shot of a Passing Waveform (Signals Overlap)



- Red: Voltage Measured at I/O Pin
- Black: Voltage of the Supply

Figure 19. Example Scope Shot of a Failing Waveform



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