White Paper

Gain Flexibility, Lower Costs in Display Control Through Integration With FPGAs

Introduction

One of the most common features in electronic equipment today is a graphics display. The most common way to add support for a display is to use an ASSP. Most of the available graphics controller ASSPs do not address all potential requirements sought by hardware developers. For example, the ability to support multiple displays, very high or non-standard resolutions, and changing video content over the lifetime of the product, are all desirable features that are not often supported by ASSPs. This paper discusses a flexible, FPGA-based graphics controller solution that supports up to a 4096 x 4096 resolution and addresses these and other requirements, in some cases at a lower cost than ASSP alternatives.

Limitations of ASSP-Based Graphics Controllers

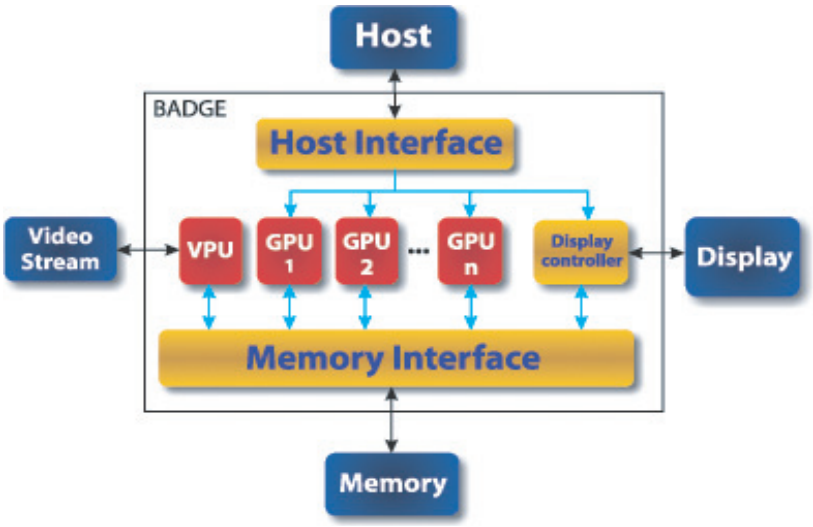
The available ASSP-based graphics controller solutions are limited. First, most do not support multiple displays—an increasingly useful feature to show information simultaneously in several places or act as a single, integrated display. To accommodate this, a controller is often required for each display, adding to both size and production costs of the board. Another limitation is the inability to support very high or non-standard resolutions. One way to address this issue is to use a standard PC graphics card, but this solution introduces heat, size, and potential obsolescence problems, as well as the task of configuration and reliance on drivers which are often proprietary.

Other limitations relate to the lifespan of the product in development. Products or product families may have changing display requirements over time, including the need to show text, 2D or 3D graphics, and/or video. The fixed-function nature of ASSPs generally does not support changing product requirements like these very well. Also, ASSPs often have short lifespans. Graphics controllers developed for the mobile phone industry, for example, can have lifespans as short as 18 months. For applications with long expected lifespans, ASSPs carry the risk that they may go end-of-life, forcing a significant redesign or disrupting product availability.

Programmable Graphics Controller Solution

A programmable graphics controller that addresses these limitations and provides additional advantages has been developed by BitSim, an Altera® partner. The controller, called BitSim Accelerated Display Graphics Engine (BADGE), is an intellectual property (IP) core that can be integrated as a stand-alone block or together with other functions in an Altera FPGA. Adding external memory (for graphics and/or video storage), a display, and a control (host) interface to the FPGA results in a flexible and future-proof display platform. The modular design of BADGE combined with Altera FPGA reconfigurability enables easy adjustments to accommodate different requirements such as new display manufacturers, a bigger display, different resolution, or alternate versions to support market-specific requirements. Figure 1 shows the BADGE solution block diagram, including optional video or graphics processing units (GPUs), interfaces to a host processor and memory, and a display controller module.

Figure 1. BADGE Programmable Graphics Controller Block Diagram



BADGE Processing Module Options

Table 1 shows the processing modules available with the BADGE solution. These modules can be included or excluded in the FPGA design as needed.

Table 1. Processing Module Options for BADGE

Module	Function
Memory Direct Access GPU	Lets the host write and read directly in the graphics/video memory as required for storing image bitmaps, fonts, etc. BADGE may also be used as a frame buffer device to display graphics, while simple enough not to require any 2D acceleration.
Simple Pixel Drawing GPU	Draws points, lines, and rectangles, with specified color, size, etc.
Character GPU	Accelerates text drawing, using customizable fonts, sizes, and colors.
Rectangle GPU	Performs rectangle copying (BitBLT) and Raster OPerations (ROPs). ROPs are often used in GUIs, such as when inverting and shadowing icons.
Video Processing Unit (VPU)	Used for analog video such as composite, S-video, or RGB, and requires an external composite decoder/ADC with parallel digital output. Can also be used for uncompressed digital video such as SDI, which requires an external deserializer. The VPU receives a digitalized video stream (such as the standard format ITU-R BT. 656) and converts this into a digital RGB signal suitable for the selected display. A multiplexer in the display controller outputs data either from the VPU or from the graphics memory (operated by the GPUs) on BADGE.
MPEG GPU	Accelerates decoding of MPEG-1 and -2 encoded video streams. Heavy functions like IDCT, interpolation, and color space conversion are realized in hardware and the video is unpacked with the help of a simple stream parsing software program.

Flexible Interfaces for Host, Display & Memory

The BADGE solution supports interfaces to several different host processor buses as shown in Table 2.

Table 2. BADGE Interface Support

Host Processor	Bus Support
Nios® II	Avalon™
Intel PXA	VLIO
PowerPC	OPB

Additionally, the Nios II processor can be implemented within the same Altera FPGA that includes the BADGE engine, eliminating the need for an external host processor. Each host interface included with BADGE supports

address-mapped graphics/video memory through the Memory Direct Access GPU to make BADGE work as a frame buffer device.

BADGE currently supports two physical interfaces to the display, the parallel LVTTL interface and the serial LVDS interface. The display controller module reads image data from the video memory and outputs it to the display, along with enable, display clock, and sync signals, according to the selected physical interface. For ultimate flexibility, the display controller module contains pointers that are set by the host interface to memory locations used for current work area, display area, font tables, video frames, and so on, enabling swift double-buffering. BADGE users can support multiple displays in their designs by instantiating a display controller module for each one.

To interface BADGE to a particular memory type, the user instantiates a memory controller variant for it. Several different memory types from a number of vendors are supported, including SDRAM and ZBT SRAM.

The modular nature of BADGE enables users to select exactly which processing units and interfaces they want to implement for their specific application, ensuring that they use only the device resources they need without paying for extra, unused functionality. Table 3 lists some of the common BADGE configurations and their functionality.

Table 3. Common BADGE Configurations

BADGE Configuration	Functionality
BADGE Lite	• Display controller module (off-loads host) • Host direct pixel write operations support • Memory Direct Access GPU—for frame buffer support • SDRAM video memory support • 32-bit buses • Up to 24-bit color depth
BADGE Video	• BADGE Lite configuration • Video Processing Unit—for analog video input • Analog video 576 x 720 pixels at 25-Hz framerate • Video shown as sub-window on display Graphics and text overlay
BADGE 2D	• BADGE Lite configuration • Simple Pixel Drawing GPU, Character GPU, and Rectangle GPU • 2D acceleration like BitBLT with ROP, line drawing engine, text (with different fonts, sizes, etc.) • Hardware cursor

Low Cost of Implementation

A complete graphics controller, including a Nios II processor, can be implemented in the smallest of Altera's Cyclone™ II FPGAs using BADGE, resulting in a very low-cost solution. BADGE Lite, which provides the minimum capability set, combined with a Nios II processor, occupies less than 4,000 logic elements (LEs), the basic building blocks of Altera FPGAs. Table 4 shows the Altera FPGA device utilization of these BADGE configurations and a host Nios II processor, including their LE and I/O pin requirements (for memory interface, LVTTL, LVDS, etc.). The table also shows the smallest Cyclone II device required for implementation, and the remaining LEs and I/O pins available in the device for additional functions.

Table 4. Altera FPGA Device Utilization

BADGE Configuration	Altera FPGA Device Utilization*(1)*	I/O Pins Needed	Minimum Cyclone II Device Required	Additional Logic Available	Additional I/O Pins Available
BADGE Lite	3,600 LEs	88	EP2C5	1,008 LEs	70
BADGE Video	5,600 LEs	163	EP2C8	2,656 LEs	19
BADGE 2D	6,500 LEs	163	EP2C8	1,756 LEs	19

Note:
(1) Includes Nios II processor

The cost of implementing a complete graphics controller solution based on BADGE and implemented in a Cyclone II device includes three elements: the price of the Cyclone II device, the price of the external SDRAM device, and the price of the BADGE IP core. For a typical application (1024 x 768 resolution at 60Hz, color depth of 16 bits per pixel), the slowest speed grade EP2C5 device and a 2M x 32 SDRAM memory would fit the requirements.

Table 5. Cost per Device

Item	Cost per Device*(1)*
EP2C5	<US$5
2M x 32 SDRAM	<US$4
BADGE Lite	<US$1
Total	**<US$10**

Note:
(1) Assuming 10K unit volumes

Depending on volumes, the slowest speed grade EP2C5 can cost less than US$5 and the SDRAM device can cost less than US$4. The price of the BADGE IP starts at US$8,500 (for the Lite configuration), which adds less than US$1 per device in volumes of 10K or more. As shown in Table 5, the resulting cost of implementation per device is less than US$10—the lowest cost for a flexible graphics controller and substantially lower than some fixed-function graphics ASSPs available today providing similar capabilities but with no flexibility. For applications requiring higher resolution, more features, more color depth, etc., a larger FPGA can be used. The cost-effectiveness of this solution is increased by using a Nios II processor instead of an external host microprocessor, thus eliminating an extra device, reducing board space, and simplifying manufacturing.

Ease RoHS Transition With Altera Lead-Free Products

Altera maintains one of the most extensive lead-free product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million lead-free products since 2002. Altera's lead-free devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances ("RoHS Directive") No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera's PLDs.

Conclusion

Adding a visual display is essential for most contemporary systems in order to achieve user friendliness and interactivity. Using an Altera FPGA-based solution increases your ability to customize the solution for a specific product, and provides a platform for easy development of a next-generation product with additional or more advanced display features. As the industry's lowest-cost FPGAs, Cyclone II devices provide a cost-effective way to implement standard display functions, in some cases delivering lower costs than existing ASSP-based solutions. In applications where higher graphics performance or more features are desirable, or where larger or higher-performance Altera FPGAs are already on the board, BADGE provides an easy and economical means of adding graphics display support.

Resources

For additional information, refer to the following resources on the Altera website.

- More System Integration Solutions
  www.altera.com/technology/integration/int-index.html

- BitSim BADGE IP Core
  www.altera.com/products/ip/iup/additional_functions_iup/m-bitsim.html
- More Information About the Cyclone II Device Family
  www.altera.com/cyclone2
- More Information About the Nios II Processor
  www.altera.com/niosII

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