White Paper

Increase Performance in Video and Image Processing Applications With FPGA Integration

Introduction

The JPEG2000 standard was developed to address a wide range of video and imaging applications, including medical imaging, military and security systems, and digital cinema. To enable these applications, JPEG2000 has many unique features, including scalability, support for regions of interest, lossless support, and low latency. Digital signal processor-based JPEG2000 solutions are available, but hardware acceleration is needed to achieve the best price/performance implementation. Accordingly, ASSP-based JPEG2000 solutions have been developed, but their fixed nature prevents them from achieving the highest performance, and their long-term availability is a concern in several of the end markets in which this technology is of interest. This paper describes an FPGA-based JPEG2000 implementation that addresses these needs and demonstrates the significant performance, cost, and integration benefits that it provides.

The Need for JPEG2000

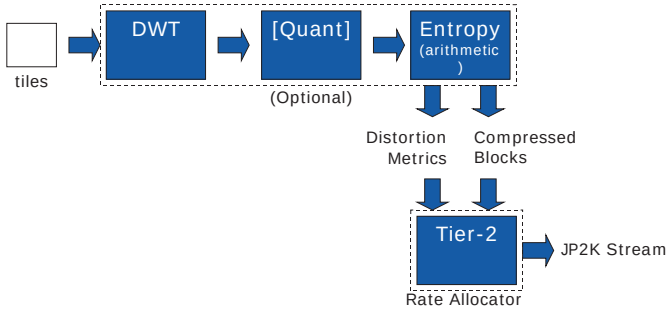
Many video and imaging applications are moving from the analog to the digital domain for a number of reasons, including ease of storage and manipulation, as well as the ability to create perfect copies and control transmission quality. One major challenge to implementing this transition is created by the large file size required for raw digital images. For instance, a 640 x 480 VGA RGB image is 1 Mbyte; a 2048 x 1536 8-bit grayscale medical image is 3 Mbytes; and a 4096 x 2160 36-bit digital cinema image is 38 Mbytes. Also, each of these applications has slightly different requirements that are not well served by earlier compression standards. To address the need for high-quality image compression as well as the disparate needs of different end applications, the JPEG2000 standard was developed.

JPEG2000 has support for both lossy and lossless compression in a single algorithm. It offers improved quality at the same compression ratio due to its removal of block artifacts, support for regions of interest, and non-iterative optimal rate control. It has been designed to facilitate on-screen display and computer imagery. It has significantly improved bit-stream scalability. This scalability includes embedded fast preview with further refinements and adaptability to instantaneously available bandwidth. All the features and compression efficiency, however, have significantly increased the algorithm complexity. JPEG2000 is up to six times more complex to implement than JPEG, making hardware acceleration a requirement for an efficient solution. FPGAs provide the ability to accelerate arithmetic operations via parallel processing, making them much better suited for JPEG2000 applications than solutions that rely solely on digital signal processors.

Identifying Elements for Hardware Acceleration in the JPEG2000 Algorithm

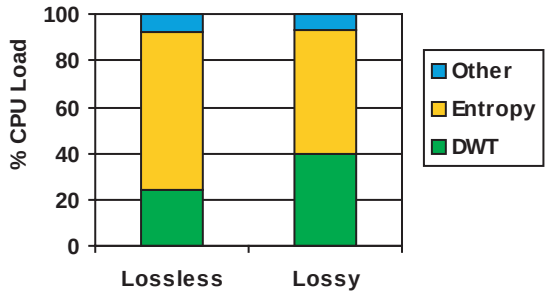
The JPEG2000 algorithm is shown in Figure 1. The processing is divided into two separate stages highlighted with dashed boxes. The first stage performs the encoding via discrete wavelet transform (DWT)-based compression, optional quantization, and entropy encoding. The second stage (Tier-2) builds up the JPEG2000 stream and includes an *a posteriori* rate allocator.

Figure 1. JPEG2000 Block Diagram



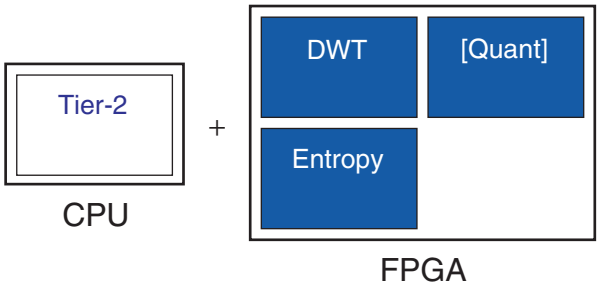
Due to its powerful features, JPEG2000 requires more computational resources than the classic JPEG standard to achieve similar encoding and decoding speeds. Figure 2 illustrates a software benchmark of the JPEG2000 algorithm for lossless and lossy compressions, where a large part of the processor time is spent on entropy encoding. This is particularly true for lossless encoding, which requires many encoding passes.

Figure 2. Software JPEG2000 Benchmarking



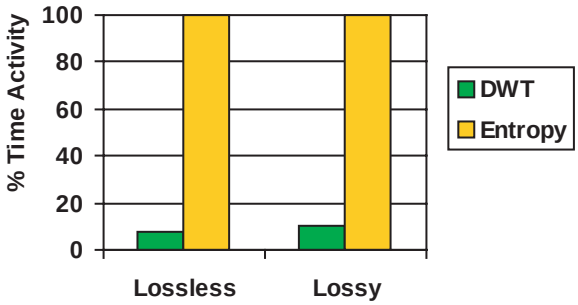
To increase the JPEG2000 performance, Barco Silex has developed an architecture where the computationally intensive wavelet, quantization, and entropy encoding tasks are off-loaded to an Altera® FPGA coprocessor, as illustrated in Figure 3.

Figure 3. Coprocessing Architecture



Hardware FPGA implementations can accelerate DWT compression and quantization by pipelining these operations. Entropy encoding, however, is more difficult to optimize due to its bit-serial structure. The graph in Figure 4 illustrates the amount of time spent on DWT and entropy operations by the Altera FPGA coprocessor architecture. The bottleneck is the entropy-encoding stage showing a permanent activity (graphed as 100 percent). The hardware DWT is only active 7 to 10 percent of the time needed to entropy encode the corresponding data.

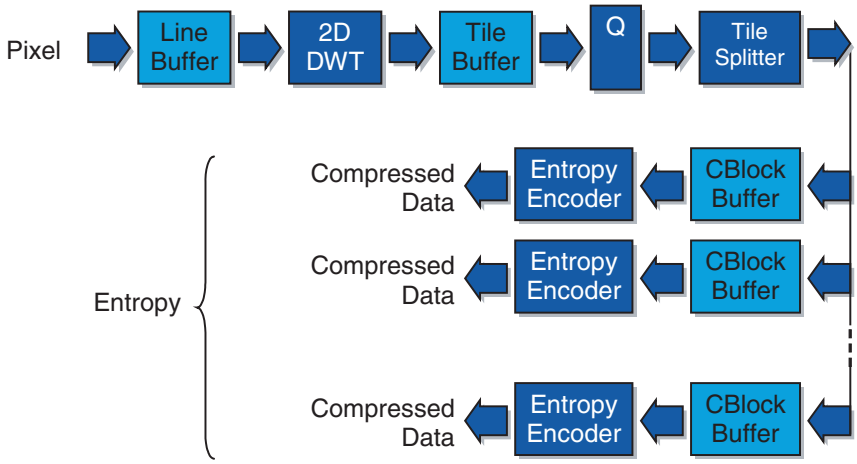
Figure 4. Hardware JPEG2000 Benchmarking



To compensate for this slow entropy encoding and to better balance the activity of the various blocks of the JPEG2000 encoding, several entropy encoders must be placed in parallel to independently process the code blocks generated by a single wavelet engine.

Figure 5 shows a block diagram of the Barco Silex JPEG2000 Encoder implemented in an Altera FPGA. This figure illustrates the main functional modules and provides a simplified view of the interfaces. The block diagram shows the parallel structure of the core, where several entropy encoders process the data generated by the wavelet engine. Pixel data is input through the pixel interface, and compressed streams are made available at the compressed interfaces, together with distortion metrics.

Figure 5. Block Diagram of Barco Silex JPEG2000 Encoder Algorithm Implemented in an Altera FPGA



Altera's FPGAs offer a number of features that make them well-suited for implementing JPEG2000 solutions, including fast and numerous RAM blocks, hardware multipliers, and large numbers of logic elements (LEs). The low cost of Cyclone® II devices makes them a highly cost-effective solution, while the abundance of memory in Stratix® II FPGAs enables them to implement complete, higher-performance solutions without using external memory. Table 1 shows the device utilization and performance of the Barco Silex JPEG2000 Encoder core when implemented in Cyclone II and Stratix II families.

Table 1. JPEG2000 Encoder Utilization and Performance Analysis in Altera FPGAs(1)

Device Family	Device Speed Grade	Number of Entropy Channels	Logic Utilization	Internal Memory Required*(2)*	External SDRAM Bandwidth Required	Performance
Cyclone II	-6	3	13,500 LEs	64-M4K RAM Blocks	81 Mbps	16 MSPS*(3)*
Stratix II	-5	8	22,000 LEs	124-M4K RAM Blocks 2-MRAM Blocks	None	56 MSPS

Notes:
(1) Results are for worst-case 9/7 (lossy) encoding of 8-bit samples.
(2) M4K RAM blocks and M-RAM blocks are embedded memory resources available in Altera FPGAs. M4K RAM blocks provide 4 Kbits and M-RAM blocks, which are available only in Stratix series FPGAs, provide 512 Kbits.
(3) MSPS = megasamples per second

These results can be compared to the estimated performance of software implementations. The minimum Stratix II device required for the JPEG 2000 Encoder in terms of memory requirements, the EP2S60C-5, can achieve 56 MSPS, while a Cyclone II device that can fit the JPEG2000 Encoder, such as the EP2C35-6, can achieve 16 MSPS. These Altera devices provide significantly better performance than the 600-MHz Texas Instruments TMS320DM642-600 digital signal processor at 6 MSPS or the 3-GHz Pentium IV at 10 MSPS.

In terms of price/performance ratios, Altera also delivers a better solution. The digital signal processor estimated 10K-unit price of US$40 results in a price/performance ratio of 6.7 US$/MSPS. The best FPGA-based price/performance ratio comes from the Stratix II device. Based on a EP2S60C-5 10K-unit price of US$125, this ratio is 2.2 US$/MSPS, significantly better than the digital signal processor solution. The FPGA-based solutions can achieve even higher performance with the addition of more entropy encoder channels in parallel, enabling designers to trade off performance for device utilization. Another option for achieving higher performance and lower cost for volume production is to use Altera HardCopy® II structured ASICs, which can deliver up to 50 percent greater performance than Stratix II FPGA-based designs at up to one-tenth the cost.

Ease RoHS Transition With Altera Products

Altera maintains one of the most extensive RoHS-compliant product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million RoHS-compliant products since 2002. Altera's devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances ("RoHS Directive") No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera's PLDs.

Conclusion

The JPEG2000 standard defines an algorithm that is able to offer a large spectrum of features, such as progressive bit stream, precise rate control, region of interest, and high-quality lossless and lossy compression. While digital signal processor- and ASSP-based JPEG2000 solutions are available, these features come at the expense of algorithm complexity. Altera FPGA-based implementations of the JPEG2000 algorithm are the most cost-effective way to tackle this complexity while achieving the performance required by real-world applications.

Resources

For additional information, refer to the following resources on the Altera website.

- More System Integration Solutions:
  www.altera.com/technology/integration/int-index.html
- Altera DSP Solutions:
  www.altera.com/technology/dsp/dsp-index.jsp
- Barco Silex JPEG2000 Encoder Core:
  www.altera.com/products/ip/dsp/image_video_processing/m-bar-jpeg_2000_enc.html
- Barco Silex JPEG2000 Decoder Core:
  www.altera.com/products/ip/dsp/image_video_processing/m-bar-jpeg_2000_dec.html
- Image and Video Processing Solutions From Altera's IP Megastore:
  www.altera.com/products/ip/dsp/image_video_processing/ipm-index.jsp
- Customer Applications of Altera Code: DSP Solutions:
  www.altera.com/corporate/cust_successes/customer_showcase/view_product/csh-vproduct-codedsp.jsp

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