Increase Performance in Imaging Applications by Integrating DSP Functions With FPGAs

Introduction

Intevac is a leading developer of photonics products for commercial and military markets. This white paper describes the development of the embedded electronic systems for their NightVista product, a compact, high-performance, ultra low-light camera. The initial implementation of this camera was based on a popular digital signal processor, several ASSPs, and external memory devices. The requirement to increase system performance led the engineering team to explore an alternative based on a configurable soft-core processor implemented in programmable logic. This decision resulted in the following gains:

■ Achievement of target performance
■ Integration of discrete components and digital signal processing (DSP) functionality into a single FPGA
■ Nearly 80% decrease in power consumption
■ Significant cost reduction by reducing five boards of components to one
■ Shorter development time

DSP Processor-Based Approach

A partial list of the functions of the NightVista electronic systems includes the following:

■ Camera power-on test and initialization
■ Video sensor calibration and characterization
■ Automatic gain control for image intensification management
■ On-screen display of graphics, text, and watermarks
■ Real-time adaptive contrast adjustment
■ Gamma correction, video freeze-frame capture, and storage to flash memory
■ Real-time clock
■ Programmable user-defined preset configurations
■ Communication with the host PC via RS-232
■ Remote update of camera features and parameters, and video data transfer from camera to host PC

Intevac's initial approach for developing the NightVista electronics was based on a digital signal processor. In addition to the processor, several other major components were required, including a NTSC video encoder, an RS-232 interface, multiple phase-locked loops (PLLs), a CPLD for miscellaneous logic, and several memories (FIFO, SDRAM, and flash). In addition, these components needed four different operating voltages (requiring four power regulators and PCB layer domains) as well as four separate clock systems and their associated oscillators and power decoupling. All together, these components occupied five PCBs, each of which was almost 2-inches square, and stacked together into a 2-inch cube that was the housing for the camera electronics.

After a few months of hardware development, it became clear that this solution would miss the performance targets Intevac sought for NightVista, and the weight and power consumption were unacceptably high. In addition, there were significant thermal management problems due to the high power dissipation in the high-density stacked PCB configuration. Intevac decided to discontinue the digital signal processor-based design in favor of a hybrid systolic logic and soft-core microprocessor implementation based on an FPGA. Intevac had no prior experience with using microprocessors integrated into programmable logic, but an evaluation using an Altera demonstration kit was very promising, since it was apparent the latest low-cost FPGAs had the capacity to integrate a complete 32-bit RISC processor with memory blocks, PLLs, and plenty of logic resources for implementing video-specific signal processing functions. The use of PLLs integrated into the FPGA looked to solve numerous problems associated with board-level multi-clock systems.

The engineering team considered a number of factors, including the following:

- Performance and feature sets of multiple FPGA families
- Availability of intellectual property (IP) cores
- Technical and business implications of integrating elements from multiple vendors
- Availability of proven hardware and software development tools
- Credibility of vendor support resources

Analysis of these elements resulted in the decision to pursue a solution based upon the Altera® Nios® processor implemented in an Altera Cyclone® FPGA. The FPGA functionality is shown in Figure 1.

Figure 1. Block Diagram of Cyclone Series FPGA Functionality Within Intevac's NightVista Camera
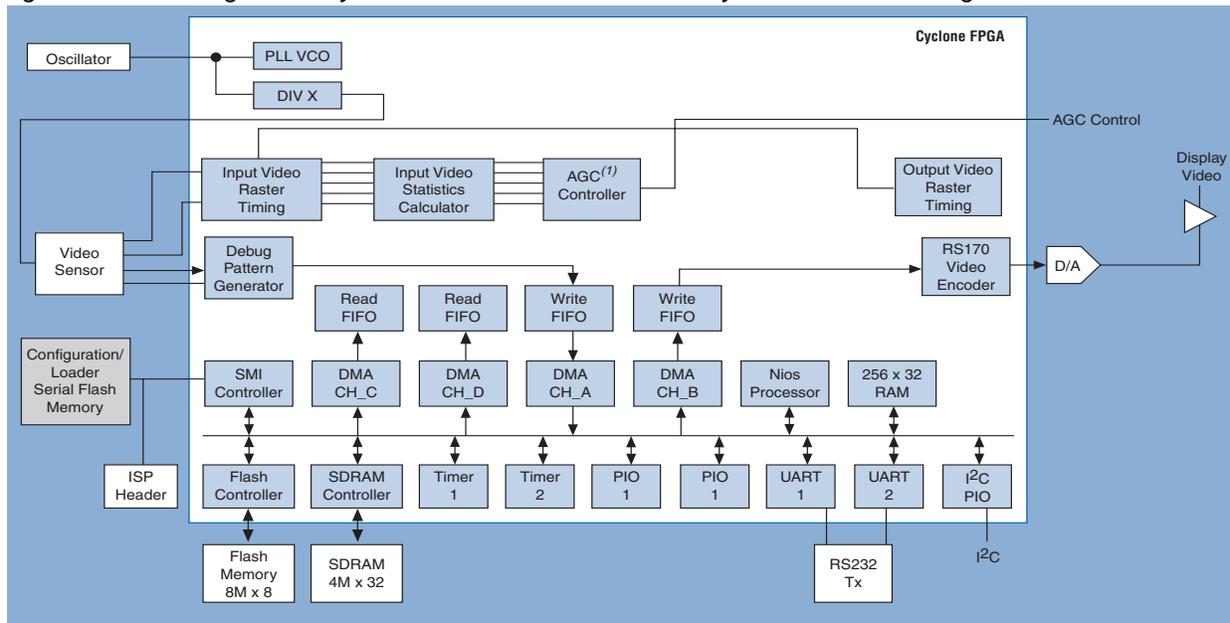
Transitioning the Design

After making the decision to use the Altera solution, Intevac had to determine how much of their existing DSP software could be ported over to the Nios processor. An 18 man-month effort of software development with the prior digital signal processor solution had brought the team to the point of passing image data through the processor to the output, with no video processing. The role of the Nios processor in the FPGA-based camera design was so dramatically different that only the RS-232 serial communication protocol used to communicate with the host PC and the video sensor configuration protocol could be reused. Fortunately, software development for the Nios processor was straightforward, and by using a Nios development board, Intevac established communication between the processor and the host PC within a matter of hours.

The circuit boards for the new FPGA-based design were completed in a month, during which time Intevac continued to create and exercise its code using a Nios processor development board. Intevac had originally anticipated using the digital signal processor's real-time operating system (RTOS) to manage the complex timing of the video processing algorithms. Because the Nios processor did not include an RTOS out of the box, the software team was unsure if they would meet all timing requirements. After consulting with the hardware team, the software team soon discovered that the configurable nature of the Nios processor allowed for a high degree of control over the timing of signals, and often only minor changes to the FPGA design were needed to reach timing goal requirements. The highly integrated nature of the hardware and firmware processing within the same FPGA environment allowed quick and easy optimization of control and video processing tasks.

FPGA-Based Approach Enables Customization and Targeted Performance Boosts

Further exploration of these possibilities led Intevac to develop custom functions and peripherals to meet its exact needs. Whenever a bottleneck was encountered in the software, the hardware team was able to develop a coprocessor to increase performance, and often the solution was up and running within an hour. The hardware team designed a custom video encoder, FIFO blocks to buffer video data, and specialized DMA controllers to keep the encoder fed with a constant video data stream, eliminating the need for an external encoder and FIFO buffers. In addition, a custom SDRAM controller was built to improve performance by allowing all video, attribute, and Nios processor command-fetch and data-storage needs to share the same memory device. Several of these functions required their own clocks, so the FPGA's on-board PLLs were employed to generate three different clocks from a master clock: one for the video encoder, a second for SDRAM timing, and a third for the external pixel sensor.

Integration Increases Capabilities

In addition to implementing functions previously requiring external devices, Intevac added functionality beyond what was possible with the original DSP processor implementation. Video test pattern generators were added to simulate camera operation, allowing the software team to perfect various algorithms for video processing and to assist in system alignment. Another addition was a statistics generator, used to analyze the nature of the video data in order to make decisions about image enhancement and image intensification. The image statistics generator required several mathematical operations that would have been too slow if implemented in software. Intevac used logic resources in the FPGA to build it from logic, setting it up to pass its results to the processor.

After receiving finished circuit boards, it took only a few hours to transfer the code from the development board and to get the code up and running on the new board. For the next few months, software and hardware development continued in parallel while Intevac further refined and debugged their design. Both the processor and the rest of the FPGA design were modified many times, without any impact on the board layout. In the end, using the Cyclone device and Nios soft-core processor reduced five boards of components to a single board. This integration lightened the camera, reduced the required number of supported voltages from four to two, and achieved nearly an 80 percent reduction in power consumption. It also enabled Intevac to efficiently produce multiple products using the same PCB set.

Ease RoHS Transition With Altera Products

Altera maintains one of the most extensive RoHS-compliant product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million RoHS-compliant products since 2002. Altera's devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances ("RoHS Directive") No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera's PLDs.

Conclusion

The simplification of the design allowed Intevac to achieve their performance targets, greatly reduced component and manufacturing costs, and increased NightVista quality and reliability. This solution also brought increased functionality beyond the initial product specification. By leaving additional resources in the FPGA, Intevac has the opportunity to further upgrade the camera while it is in the field. This solution enabled Intevac to explore and refine a more rapid and efficient design development flow, saving a great deal of time and resources in future product development.

Resources

For additional information, refer to the following resources on the Altera website.

- Intevac NightVista Camera in Altera's Customer Showcase:
  www.altera.com/corporate/cust_successes/customer_showcase/csh-intevac_lp.html
- More System Integration Solutions:
  www.altera.com/technology/integration/int-index.html
- Customer Applications of Programmable Logic:
  www.altera.com/corporate/cust_successes/customer_showcase/csh-index.html
- Altera DSP Solutions:
  www.altera.com/technology/dsp/dsp-index.jsp
- Information on Nios Embedded Processors:
  www.altera.com/products/ip/processors/nios2/ni2-index.html

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