White Paper

Reduce System Costs by Integrating PCI Interface Functions Into CPLDs

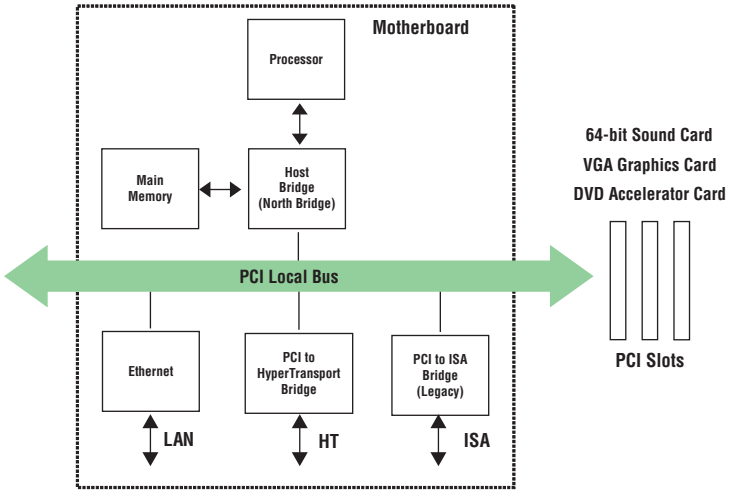
Introduction

Many of today's PCI bus interfaces are implemented using ASSPs. However, the most common functions of PCI target interfaces can be implemented at lower costs using CPLDs, resulting in cost savings and potential reductions in board space. These benefits are readily available via complete, easy-to-use PCI interface solutions.

PCI Bus Overview

Expansion buses are connections that allow peripheral controllers to use system resources, such as hard disks, memory and I/O space, and audio/video hardware. The PCI bus is the most commonly used expansion bus. It provides a shared data path between the CPU and peripheral controllers in a wide range of electronic systems. Figure 1 shows a typical PCI local bus system architecture.

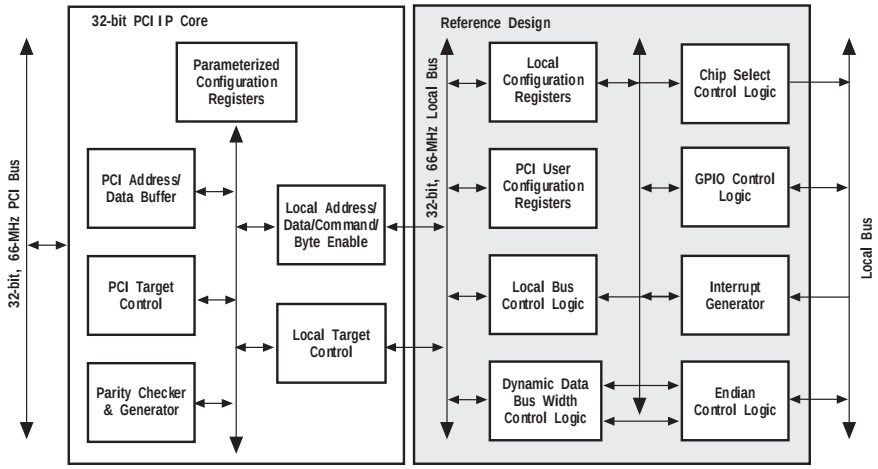
Figure 1. Typical PCI Local Bus System Application



Low-Cost PCI Interface Implementation in Programmable Logic

An Altera® MAX® II CPLD can function as a 32-bit, 66-MHz PCI target interface by integrating Altera's PCI target interface intellectual property (IP) core and a reference design that acts as a local bus interface. The reference design implements a local bus interface similar to common ASSP-based PCI interfaces. The Altera PCI target interface core is compliant with the requirements specified in the PCI Special Interest Group (PCI-SIG) PCI Local Bus Specification, Revision 3.0 and the PCI Compliance Checklist, Revision 3.0. Figure 2 shows a block diagram of Altera's MAX II CPLD-based PCI target interface solution.

Figure 2. Altera's MAX II CPLD-Based PCI Target Interface Solution Block Diagram



The reference design for the local bus interface has the following features:

- PCI local bus specification r2.2 vital product data (VPD) configuration support
- Flexible local bus provides 32-bit multiplexed or non-multiplexed protocol for 8-, 16-, or 32-bit peripheral and memory devices
- Nine programmable general purpose I/O elements (GPIOs)
- Five programmable local address spaces
- Four programmable chip selects
- Programmable local bus wait states
- Two programmable local-to-PCI interrupts
- Endian byte swapping
- Local address remap

Altera's MAX II CPLD-based PCI target interface solution can be implemented at a lower cost than ASSP-based PCI target interface solutions. Table 1 compares the cost to implement a 32-bit PCI target interface in an ASSP and in a MAX II device. The table compares the component cost of a PLX PCI9030 ASSP to the cost of implementing PCI target interface functionality in two different MAX II devices: the EPM1270 and the EPM2210. The component cost of the function in either MAX II device is based on the number of logic elements (LEs) that are required to implement the function. LEs are the basic building blocks of MAX II CPLDs.

Table 1. Comparison of PCI 9030 ASSP and MAX II CPLD-Based PCI Target Interface Solution

Supplier	MAX II Device	PCI Target Interface Features	Logic Available in Device	Logic Required for PCI Target Interface	Additional Logic for User Designs	Component Cost*(1)*
Altera	EPM2210	32-bit/66-MHz PCI + reference design for 32-bit local bus*(2)*	2210 LEs	~920 LEs	~ 1,290 LEs	US$14.65
Altera	EPM1270	32-bit/66-MHz PCI + reference design for 32-bit local bus*(2)*	1270 LEs	~920 LEs	~ 350 LEs	US$15.25
PLX Technology	PCI9030	32-bit/33-MHz PCI + 32-bit local bus	None	N/A	None	US$19.25

Notes:

(1) Based on 100-unit price and logic utilization required to implement PCI interface function; does not include cost of IP license.

(2) Altera's MAX II device PCI target interface solution includes the majority of functions used in standard PCI target interfaces, but does not support PCI target read-ahead mode, programmable burst, delayed write modes, and posted memory writes.

Additional Advantages of the MAX II CPLD-Based PCI Target Interface

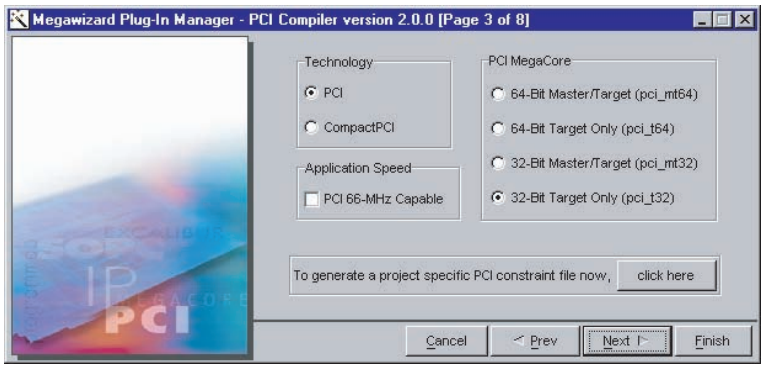
Implementing a PCI target interface does not require all of the logic resources in either the EPM1270 or EPM2210 device. As shown in Table 1, there is additional logic available in the devices that can be used to integrate other board components, such as memory controllers, proprietary bus controllers, and general purpose I/O elements. MAX II CPLD-based PCI interfaces allow designers to reduce board space by using a single-chip solution, unlike ASSP-based PCI interfaces, which may require the use of multiple discrete devices to achieve the same functionality.

Additionally, using programmable logic protects the design from obsolescence. Because ASSPs are on older process nodes and become more expensive to support, they become obsolete over time, eventually being discontinued. These business conditions cannot justify continued manufacture by the ASSP vendor. As a result, system designers using ASSPs-based solutions can be forced into costly and time-consuming hardware and software redesigns. The MAX II CPLD-based PCI target interface solution helps to prevent this kind of system obsolescence, since it can be migrated to future-generation CPLDs and low-density FPGA families, thereby ensuring that the system will remain compatible across several generations of hardware.

Easy-to-Use, Low-Cost Development Flow

Using the MAX II CPLD-based PCI target interface requires Altera's Quartus® II development software and PCI Compiler, a development tool that provides an easy way to customize a PCI target interface IP MegaCore® function for implementation in a MAX II device. Figure 3 shows an example of the PCI Compiler's graphical user interface.

Figure 3. PCI Complier Graphical User Interface



Altera's OpenCore Plus evaluation feature allows users to evaluate the PCI interface IP MegaCore function in hardware and simulation prior to licensing. The PCI Compiler, reference design, and Quartus II Web Edition software can be downloaded at no cost from Altera's website. Also, Altera's low-cost MAX II development kit can be used to develop and evaluate the MAX II CPLD-based PCI target interface in hardware.

Ease RoHS Transition With Altera Products

Altera maintains one of the most extensive RoHS-compliant product offerings in the industry, with over 1200 products in lead-free packages. As a preeminent supplier of environmentally friendly programmable logic solutions, Altera has shipped over 25 million RoHS-compliant products since 2002. Altera's devices comply with the maximum concentration restrictions, as required in the EU Directive on the Restriction of Hazardous Substances ("RoHS Directive") No.2002/95 with respect to lead (Pb), mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Help ease your RoHS transition by integrating non-compliant ASSPs with Altera's PLDs.

Conclusion

Programmable-logic based solutions for PCI target interfaces offer significant advantages over ASSPs in terms of cost, board-space reduction, flexibility, and obsolescence-proofing. Proven solutions for the PCI target interface are

readily available from Altera for demonstration and evaluation free of charge. See the "Further Information" section of this document for information on where to download the reference design and PCI core, as well as PCI Compiler and Quartus II software.

Further Information

- PCI to Local Bridge Reference Design
  https://www.intel.com/content/www/us/en/programmable/products/reference-designs/all-reference-designs/wireline/ref-dexcel.html
- PCI Compiler User Guide
  https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_pci.pdf

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