Introduction

Data center requirements are rapidly evolving in the wake of next-generation applications and networking features, such as Network Functions Virtualization (NFV), cloud computing (CC), and the build-out of 5G wireless infrastructure. It is likely that in the next few years, virtually every industry from communications to automotive will rely heavily on cloud computing and the new data economy. The backbone of this is data centers, which are now facing the need to shift to higher bandwidth operation while enhancing the ability to adapt to new requirements and maintaining backward compatibility.

Intel® Stratix® 10 DX FPGAs and SoCs are an enabling technology that can meet next-generation high-bandwidth requirements for emerging applications, such as cache-coherent accelerators, higher performance SmartNICs, and custom servers for cloud service providers (CSPs). These features are designed to unleash SmartNIC acceleration, memory expansion, and data center disaggregation applications.

However, these high-performance devices also require extremely efficient and compact power solutions that are also robust and easy to use, so that systems designers can focus their valuable time on the FPGA design and operation and not on power solutions. This is the reason why Intel offers Intel Enpirion® Power Solutions that are designed and validated for Intel FPGAs, CPLD, and SoCs, along with a suite of tools and methods to ease the path of achieving a quality power solution.

This white paper describes how to use the tools and resources from Intel to realize an optimized power solution for Intel Stratix 10 DX FPGAs and SoCs. If an immediate solution is needed, you can reuse the reference design from the Intel Stratix 10 DX FPGA Development Kit. If you would like to reuse the development kit design, but desires a lower capacitor count, then you can use the Power Delivery Network (PDN) tool to optimize the bulk and decoupling capacitor quantities. If a lower power design is needed, a custom design is desired, or you would like to take another approach other than using the development kit, follow the step-by-step guide below to achieve a high-performance power delivery solution for Intel Stratix 10 DX FPGAs. For assistance with choosing which approach to power delivery solutions, consult an available Intel technical support specialist via www.intel.com/power.

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Tools and Resources for Designing a Power Solution

This section highlights the tools and resources you need to design an optimized power solution for an Intel Stratix 10 DX FPGA or SoC using Intel Enpirion Power Solutions. The following tools include:

- Intel Quartus® Prime Software
- Early Power Estimator
- Intel Enpirion Power Solutions Data Sheets
- Power Distribution Network or Power Delivery Network Tool
- Designer's kit
- FPGA data sheet
- FPGA design resources and development kit

Intel Quartus Prime Software

The Intel Quartus Prime software is a design tool that includes all the necessary features to design and program Intel FPGAs, SoCs, and CPLDs. This includes features that enable entry and synthesis level design, as well as optimization, verification, and simulation. The software can be downloaded from the Intel Quartus Prime Software page, also found in the links at the end of this section.

Relevant links

- Intel Quartus Prime Software

Early Power Estimator

The Early Power Estimator (EPE) is a helpful tool in estimating the power requirements of an Intel Stratix 10 FPGA based on preliminary and characterized power data. The EPE provides power estimates and current estimates based on typical conditions programmed by the user, which include parameters such as room temperature and nominal voltage. It is important to note that the EPE provides estimates only and is not a guarantee of performance or a specification of performance.

Relevant links

- Early Power Estimators and Power Analyzer
- Download Page for Early Power Estimator for Intel Stratix 10 Devices
- Early Power Estimator For Intel Stratix 10 FPGAs User Guide

Intel Enpirion Power Solution Data Sheet

The Intel Enpirion Power Solutions data sheets are essential for selecting the appropriate devices for a given design. Data sheets for a specific Intel Enpirion solution can be found on the device's page or from the links at the end of this section.

Relevant links

- Intel Enpirion Power Solutions
- Intel Power Devices
- Intel Enpirion Power Solutions for Stratix 10 FPGAs and SoCs
- Power Intel Stratix 10 FPGAs and SoCs Solutions Brief
- Intel Enpirion Power Solutions Selector Guide
- Understanding and Meeting FPGA Power Requirements

Power Distribution Network or Power Delivery Network Tool

The graphical Power Distribution Network or Power Delivery Network (PDN) design tool is an Excel-based, graphical instrument that aids in optimizing the board-level PDN with all Intel FPGAs in regards to distributing power and return currents from voltage regulating modules (VRMs) to the FPGA power supplies, and to ensure optimal performance of the FPGA and transceiver signal integrity. The PDN extracts information from the EPE and can be used to determine a desirable number of bulk and decoupling capacitors for optimal performance and cost.

Relevant links

- Power Distribution Network or Power Delivery Network (PDN) Tool
- PDN User Guide
- Device Specific PDN User Guide

Designer Kit

For each Intel Enpirion device, there is a designer kit accessible from the product webpage. These kits include all the schematics, symbols, layout, and models for designing with Intel Enpirion Power Solutions.

Intel Stratix 10 DX FPGA Data Sheet

The data sheets for the Intel Stratix 10 DX FPGAs and SoCs include all the essential descriptions of the electrical and switching characteristics, as well as the configuration specifications and timing.

Relevant links

- Intel Stratix 10 DX FPGAs
- Intel Stratix 10 Device Datasheet
FPGA Design Resources and Development Kit

Intel provides design, support, and resource documents for Intel Stratix 10 DX FPGAs or SoCs provided free on the Intel Stratix 10 DX page. You can also refer to the following links, which include the FPGA Pin Connection Guidelines (PCG) and other device design guidelines.

Relevant links
- Intel Stratix 10 Support Documentation & Tools
- Intel Stratix 10 Device Design Guidelines
- Intel Stratix 10 Device Family Pin Connection Guidelines
- Intel Schematic Symbol Library
- AN 766: Intel Stratix 10 Devices, High Speed Signal Interface Layout Design Guideline
- Intel Stratix 10 Power Management User Guide
- Intel Stratix 10 DX FPGA Development Kit
- Intel Stratix 10 DX FPGA Development Kit User Guide

Building the Power Tree

This section explains the use of the EPE and the Intel Empirion Power Solutions selector guide for estimating the power requirements of an Intel Stratix 10 DX FPGA or SoC and selecting appropriate Intel Empirion Power Solutions to power the FPGA. The results of this effort help you to successfully build a Power Tree, which is the system of power solutions that provides all of the necessary voltage inputs necessary for the FPGA to operate.

Using the Early Power Estimator

The first step in building a power tree is to use the EPE to determine the power requirements of a specific Intel Stratix 10 DX FPGA or SoC. The register transfer level (RTL) code from the Intel Quartus Prime software Power Analyzer can be exported as a CSV file, which is used as an input into the EPE. If the RTL code is not available during the early design stages, the necessary information can be input to the EPE manually. After all the necessary inputs to the EPE are filled, the results are a thermal analysis report and a complete report that provides the current requirements for each power supply input. This information is used to build the power budget and to determine roughly which Intel Empirion Power devices would best fit each power supply input given the current requirement.

![Figure 1. Intel Stratix 10 DX FPGA Development Kit](image)

![Figure 2. Intel Stratix 10 DX FPGA Power Tree Example](image)

![Figure 3. The Input Section of the EPE](image)
The EPE also provides valuable estimates that can significantly reduce the time it takes to sort through the various power supply options and to build a power tree. After the power requirements are determined, an evaluation of the Intel Enpirion Power Solutions selector guide can provide the necessary components to fill the power tree. The following document helps you to select specific Intel Enpirion power devices for Intel Stratix 10 FPGAs or SoCs—Intel Enpirion Power Solutions for Intel Stratix 10 FPGAs and SoCs.

There are other decisions that need to be made that also impact power device selection.

The following list the power device selection considerations:

- Does my design need an intermediate bus using a bus converter (such as EM2120 or EC2650)?
  - EC2650 would be selected as an intermediate bus for 12 V when the current is under 20 A, and the EM21xx solutions when the current is between 20 and 80 A.

- Does my design need a 2, 3, or 4 phase Multi-Phase Controller (such as the ED8401QI)?
  - Phases may be added based on the design’s current requirements. Each power state is rated at 70 A, so a number of phases must be used to meet desired power requirements. For example, a 200+ A design would require a 4-phase configuration.

- Does my design require a high-current module for the core (such as EM2280), or a discrete multi-phase solution (ED8401 and ET6160)? A multi-phase solution is required for power core rails approximately above 60 A.

- Do I have noise-sensitive inputs that require reduced power supply ripple (such as EN29A0)?

The following white paper describes how to address these considerations—Understanding and Meeting FPGA Power Requirements White Paper.

### Using the PDN Tool to Optimize Decoupling Capacitor Design

The PDN design tool is a Microsoft Excel spreadsheet that is used to calculate the impedance profile of a power distribution network design for Intel FPGAs based on user inputs. With basic user inputs (some of which come from the EPE), such as the power supply, board stackup, transient current information, and ripple specifications, the PDN tool yields an impedance profile and an optimized number of capacitors to meet a given impedance target. Intel Enpirion Power Solutions can reduce the number of bypass capacitors needed. It is important to note that the results of the PDN tool are preliminary estimates, and using a post-layout EDA simulation tool can produce a more accurate impedance profile. With the number of decoupling capacitors determined, you can proceed with schematic capture and simulation.
Schematic Capture
The Intel Schematic Symbol Library can be found in the following link—Intel Schematic Symbol Library. The symbols of the selected Intel Enpirion power devices, as well as the Intel Stratix 10 DX FPGA can be placed in a PCB schematic design software, such as OrCAD, by selecting the symbol that goes with the appropriate device number from the power tree. When all of the symbols have been selected and placed in the Schematic Editor, the correct interconnection of all of the device pins can then be completed.

Layout
Physical layout can be performed after the schematic editing process is complete. With each interconnect correctly established in the schematic editor, the physical layout tool can then be used to ensure that each connection made during layout matches that within the schematic editor.

The physical layout process consists of the following steps:
1. Bring all devices into the physical layout tool along with PCB constraints.
2. Place the devices to optimize the layout considering space, thermal properties, physical access to pins, crosstalk/noise, and trace parasitics.
3. Connect all devices according to the schematic considering that trace resistance, inductance, and capacitance are intrinsically tied to the physical geometry of the trace and that capacitive and inductive coupling occur based on the placement of traces in proximity to each other.
4. Check the completed layout using layout-versus-schematic (LVS) test to ensure all interconnections were properly made.

After the layout is completed, software simulations to confirm behavior can be performed. If these simulations are successful, a physical board can be fabricated. Even though simulations may have indicated a successful design, physical verification of the design is still necessary to include factors that are otherwise difficult or impossible to include in simulation. In some cases, a designer may want to consult with their local Intel Power technical support representative as a final step.

The following lists the physical layout considerations and tips for Intel Enpirion Power Solutions:

- Input and output filter capacitors should be placed on the same side of the PCB, and as close to the Intel Enpirion device package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the Intel Enpirion device should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.
- The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.
- The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and uninterrupted below the converter and the input/output capacitors.
- The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33 mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26 mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.
- Multiple small vias (the same size as the thermal vias discussed in the previous recommendation) should be used to connect the ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops.
- AVIN is the power supply for the small-signal control circuits. It should be connected to the input voltage at a quiet point. This connection may be made at the input capacitor.
- The layer 1 metal under the device must not be more than recommended. Refer to the Intel Enpirion device datasheet section regarding Exposed Metal on Bottom of Package.
- As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.
- The VOUT sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node.
- Keep RA, CA, RB, and R1 close to the VFB pin. The VFB pin is a sensitive, high-impedance node. Keep the trace to this pin as short as possible. Whenever possible, connect RB directly to the AGND pin instead of going through the GND plane.
Power On with VRTT

The Voltage Regulator Test Tool (VRTT) is a piece of validation hardware designed by Intel for the purpose of characterizing power supply robustness. The VRTT can test the static and dynamic current of multiple voltage rails on several FPGAs simultaneously. For instance, a VRTT can be used to test the static and dynamic current of an Intel Enpirion EM2260P01QI PowerSoC used to power the core of an Intel Stratix 10 DX FPGA Development Kit.

The test setup just requires a VRTT, male-to-male header, interposer and the system-under-test (SUT)/development kit, and a PC. The results of the test are result figures and plots that show the performance of the system in terms of multi-phase response, ripple, transient electrical behavior, power efficiency, and more. The VRTT products, including the necessary interposer board can be found on the Processor VRTT web page.

Typical Results and Plots

The results of testing FPGA power delivery solution performance must yield adequate DC accuracy, ripple noise, and transient response. The following is a discussion of testing these key parameters and test results examples from an Intel Stratix device family.

DC Accuracy

The DC Accuracy specified in the Intel Stratix 10 FPGA Pin Configuration Guidelines and General Data Book includes power supply ripple noise in addition to the accuracy of the voltage regulator and any variation of the resistors used to set the output voltage. Therefore, a typical DVM is not adequate to verify the DC accuracy. Rather, the minimum and maximum voltage detected over time should be used to calculate the absolute DC accuracy on each rail.

Figure 5. DC Accuracy of the VCC Core with No Load

Figure 6. DC Accuracy of the VCC Core with 55A Full Load

Ripple Noise

A known measurement technique with a resolution of at least 2mV is suggested for measuring ripple noise. If an adequate scope probe cannot be found, a coaxial cable with a SMA or SMB connector may be used instead. One end of the coaxial cable can be cut off with the leads soldered to one of the high-frequency capacitors directly underneath the FPGA. The oscilloscope should be configured to AC coupled, 1:1, and no bandwidth limitation.

Figure 7. Ripple Noise of the VCC Core No Load
Summary

This white paper introduces the Intel Stratix 10 DX FPGA or SoC and presents a step-by-step guide of how to design a power delivery solution for this family of FPGAs. The guide includes a description of all the necessary documents and software, and explains how to build a power tree using EPE and parametric power device part selection. Furthermore, a description of the schematic editing and physical layout procedures is provided, along with a discussion of the VRTT for validating a design. A description of the results of a VRTT is also presented.

For more information about Intel and the Smart Grid, visit www.intel.com/power.

Figure 8. Ripple Noise of VCC Core 55A Full Load

Transient Response

The same setup as ripple noise can be used to measure the transient response. A summary of the transient response specifications can be found in the PDN Power Distribution Network tool.

Figure 9. Transient Response of VCC Core at 28 Step Load
References
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2. Intel FPGAs Accelerate Intel Xeon® Scalable Processors in Servers and High-End Embedded Systems
3. Expand Server Memory Capacity and Improve Server Performance with Intel Stratix 10 FPGAs and Intel Optane™ DC Persistent Memory
4. Intel Stratix 10 Device Datasheet
5. Intel Stratix 10 Support Documentation & Tools
6. Intel Stratix 10 Device Design Guidelines
7. Intel Stratix 10 Device Family Pin Connection Guidelines
8. Intel Stratix 10 DX FPGA Development Kit
9. Intel Stratix 10 DX FPGA Development Kit User Guide
10. Intel Quartus Prime Software Suite
13. Early Power Estimators and Power Analyzer
14. Download Page for Early Power Estimator for Intel Stratix 10 Devices
15. Early Power Estimator for Intel Stratix 10 FPGAs User Guide
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24. ED8401QI: Multi-Phase Digital Controller with PMBus
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29. AN 766: Intel Stratix 10 Devices, High Speed Signal Interface Layout Design Guideline
30. Intel Voltage Regulator Test Tool
31. VRTT Demo
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