PLC Architecture in the Industry 4.0 World: Challenges, Trends, and Solutions

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Introduction

Programmable logic controllers (PLCs) are an integral part of factory automation and industrial process control. PLCs control a variety of analog and digital sensors and actuators, and communicate over simple to complex interfaces in varying protocols. In addition to control functions, PLCs perform signal processing and data conversion.

This white paper examines the challenges and motivations of evolving PLC architectures and discusses current trends. For example, the Industrial Internet of Things (IIoT) expects future PLC architectures to deliver scalable solutions that are secure, high performance, low power, small footprint, and are ready for Industry 4.0—with built-in secure communications to enterprise IT systems aiding IT-powered manufacturing.

PLC Evolution

Since their introduction, PLCs have evolved from simple input-output controllers to complete processor-based systems that execute complex control algorithms. PLCs have undergone significant form-factor changes: from industrial PCs and Programmable Automation Controllers (PAC) in PC-like form-factors to compact enclosures and mini-PLCs. The scope of PLC functionality has also evolved. In addition to discrete control functions, PLCs have integrated functionality such as Human Machine Interface (HMI), motion-control, real-time industrial Ethernet, and data communication gateways.

The demand for additional features, precision, and connectivity on the factory floor has driven this increasing integration. It has been sustained by PLC component cost reductions and the availability of higher performance processing engines. In general, the evolution of PLC functionality has followed the industrial automation demand curves of features, performance, and lower power. Following that trajectory, the demands of Industry 4.0 and IoT, to a large measure, will drive future PLC architectures.

Historical Role of Motion-PLC in Driving PLC Architecture

To appreciate the effect of market drivers on PLC architecture, it is useful to examine how motion-PLCs drove performance requirements, and therefore, architecture. Over the last 10 to 15 years, a quiet revolution took place in factory automation: the number of controlled axes per machine increased significantly. Figure 1 conceptually depicts this increase in the context of the CPU load.

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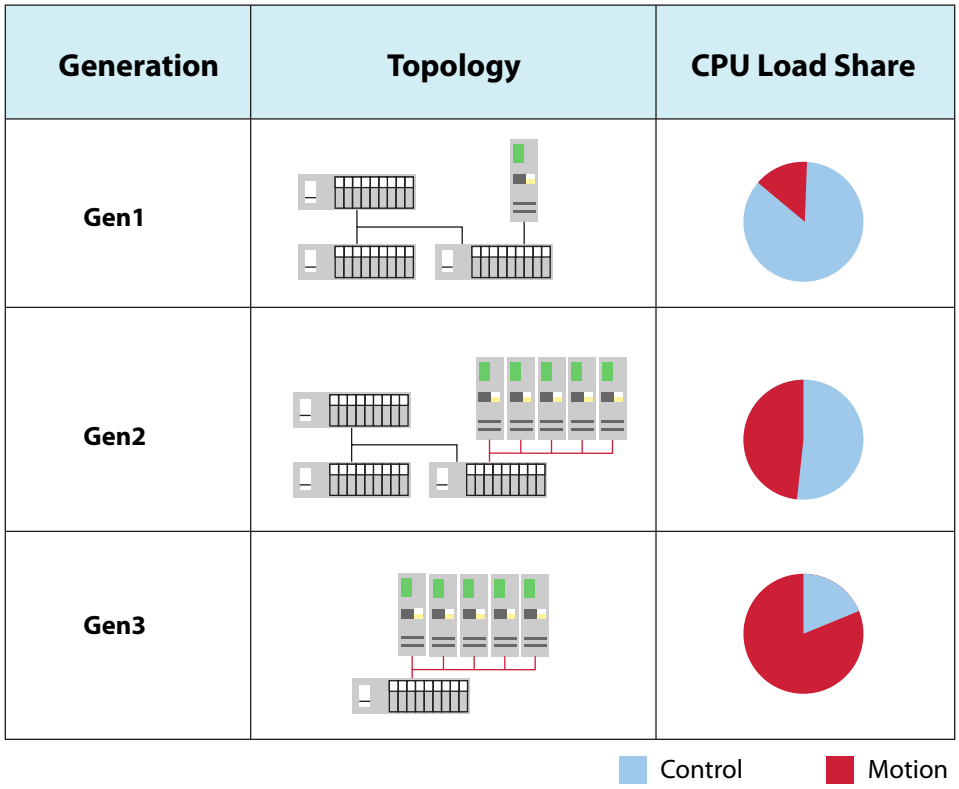
Figure 1. Control and Motion CPU Load Share



Source: Bosch. Rexroth Group

With centralized control, in which the main controller controls all feedback loops, all axes (and other discrete I/O) share the processing power. This architecture limits performance and flexibility. An increased number of axes required faster update cycles and led to the deployment of faster, more expensive, power hungry processors.

Distributing motion-control functionality to distributed axes drives, thereby removing the burden from the main controller, mitigated these limitations. However, this model suffered from the high cost of multiple processors and produced an overall larger system footprint with increased power consumption.

Power and Space Constraints Drive Move to Compact, Modular PLCs

As energy costs became a significant concern and factory space became increasingly expensive, manufacturers moved away from large-footprint, multi-processor architectures and back to centralized control. While this move solved the space constraints and associated costs, newer technological approaches were required to address the performance bottlenecks of single processors that had led to a distributed architecture in the first place.

Hybrid PLC Architecture: Processor and FPGA

Manufacturers attempted to address the performance issues with a novel approach: combining processors and FPGAs. The processor performed standard control functions (comprising primarily of gateway and discrete I/O control, but also HMI functionality), while the FPGA performed the rest, specifically, motion control. Table 1 shows some historical real-world examples.

Table 1. Hybrid Processor and FPGA Example Architectures in Real-World PLCs

Product	Architecture (Processor and FPGA)
PLC 1	NEC ASSP (MIPS) and FPGA
PLC 2	Renesas (V850) and FPGA
PLC 3	ST Spear and FPGA
PLC 4	Intel x86 and FPGA
PLC 5	TI Sitara and FPGA

Source: Altera Database

Problems with the Hybrid Processor and FPGA Approach

The hybrid processor and FPGA architecture solved the performance problem. However, it still suffered from the increased power consumption of the faster processors. Additionally, it came at a high cost from high-performance processors and the additional FPGA cost.

The typical 5-year lifetime of processors also introduced additional product lifecycle headaches. Typical industrial equipment life cycles (7 to 10 years) are incompatible with 5-year processor lifetimes. This incompatibility led to obsolescence difficulties that contributed to delays in new algorithm development. Engineering teams scrambled to redesign existing equipment when a processor was at its end of life.

The hybrid approach also led to limited protection of manufacturers' software investments. There was no guarantee that a replacement processor would come from the same manufacturer. Therefore, roadmap scalability became a significant problem. Approximately 80% of manufacturers encountered developmental delays and only ~30% of projects achieved their original forecast volumes due to delayed time to market[1].

Major PLC manufacturers experience the following issues[2]:

- Design cycles are getting longer
- Time to market is becoming more critical
- Competition has increased; competitors adapt to market requirements quickly
- For safety-PLCs, functional safety certification is challenging and takes a long time
- Equipment needs to support secure communication to the enterprise domain with deterministic I/O information

[1]Source: Altera analysis tracking thousands of designs

[2]Source: Altera Customer Advisory Board interviews of a variety of PLC manufacturers

- Increased cost pressures
- Demand for scalable, high-performance applications with lower power
- Convergence of software and hardware teams' development approaches remains a challenge
  - Impacts productivity
  - Impacts time-to-market goals

These issues align with those observed in the hybrid approach:

- Software development continues to drive product differentiation. However, new algorithms take a long time to implement
- Higher performance or more processor cores are needed, which translates to higher BOM cost and increased power consumption
- In a hybrid model, FPGA acceleration is difficult due to processor-FPGA functional integration issues
- A particular implementation may not provide a path to longer term, higher value solutions, forcing a redesign to a different processor
- Obsolescence adds unavoidable iterations and interruptions
- Ultimately impacts profitability

The Industry 4.0 Paradigm and Its Impact on PLC Architecture

The current manufacturing automation environment of Industry 4.0 demands high-performance PLCs enabled with secure enterprise connectivity and HMI. Today, multiple international Industry 4.0 initiatives rely on cyber-physical systems to implement the promise of smart manufacturing, leveraging connected systems for Machine-to-Machine (M2M) and enterprise interaction.

Making PLCs ready for Industry 4.0 is fraught with new challenges, requiring grounds-up PLC redesign. The major challenges confronting PLC designers today include:

- *High-performance control*—Smart-manufacturing environments require PLCs to process instructions, service interrupts, and support integrated HMI at speeds faster than ever before. This need has led to the use of more powerful processors with higher MIPS and multiple cores, resulting in high cost and power consumption penalties.
- *Connectivity*—Deterministic M2M connectivity between disparate machines requires support for multiple Industrial Ethernet protocols (including newly emerging standards-based deterministic Ethernet such as IEEE 802.1 TSN) within a single PLC system. Enterprise connectivity demands application interoperability frameworks such as OPC-UA.
- *Secure communications*—PLCs connected outside the factory network and to the enterprise are vulnerable to cyber-attacks, making security a significant concern.
- *Cross-platform interoperability*—Choosing the wrong processor or ASSP can be an expensive error. Functional interoperability between diverse systems requires standardized operating systems running on non-proprietary processor cores.

- *Future proofing*—With an ever-evolving connectivity and interoperability environment, changes in market requirements are more frequent, leading to software and hardware changes.

Furthermore, pre-Industry 4.0 challenges remain, including scalability, functional safety, lower power consumption, smaller footprint, and software investment protection.

SoC FPGAs: A Smarter Approach to PLC Architecture

System-on-Chip (SoC) FPGAs, which combine a processor and FPGA fabric on a single chip, present a unique alternative for overcoming today's PLC design challenges:

- *High-performance control*—SoC FPGAs can off-load the PLC's processor by implementing high-performance algorithms and HMI in the hardware fabric. Unlike sequential processors, FPGAs are massively parallel and can greatly accelerate algorithm execution. With embedded digital signal processing (DSP) blocks and on-chip memory, FPGAs offer faster hardware acceleration at lower cost and power consumption than conventional processors.
- *Connectivity*—FPGAs can implement multiple Industrial Ethernet protocols simultaneously on a single device by instantiating ready-made intellectual property (IP) cores. Designers can enable protocols by downloading the relevant protocol stacks, which execute in the built-in SoC FPGA Hard Processor System (HPS). The HPS can also run an OPC server, enabling enterprise communications over OPC-UA. Designers can integrate emerging standards, such as IEEE 802.1 TSN, by reprogramming the FPGA hardware. The high-performance FPGA fabric can easily meet the stringent IEEE 802.1 TSN timing requirements.
- *Secure communications*—Open SSL encryption, implemented in the FPGA fabric, provides up to 4X acceleration over processor-based implementations. This encryption enables faster, more secure enterprise communication channels.
- *Cross-platform interoperability*—With an integrated processor, SoC FPGAs offer a scalable roadmap using an industry-standard processor.
- *Future proofing*—Designers can reprogram the FPGA fabric to incorporate hardware changes, avoiding major redesign of entire systems.

Worldwide SoC Adoption Trends in PLC Architecture

Table 2 summarizes PLC manufacturers using SoCs in PLC architecture in 2013. This summary includes conversions from hybrid architecture to SoC and new designs based on SoCs.

Table 2. Worldwide SoC Adoption in PLC Architecture – 2013

Region	Application	Number of Platforms	End Product/Manufacturer Profiles
Asia-Pacific	PLC, I/O, and other factory automation	30	Local factory automation equipment manufacturers
Europe	PLC, I/O, and other factory automation	34	Factory automation and process control equipment manufacturers with international operations
Japan	PLC, I/O, and other factory automation	49	Factory automation and process control equipment manufacturers with international operations
North America	PLC, I/O, and other factory automation	41	Equipment manufacturers in defense and aerospace, factory automation/process control with international operations
Worldwide	PLC, I/O, and other factory automation (all regions)	154	38.3% of all new designs that used an FPGA (402 total designs)

Source: Altera Market Analysis (Includes Known Sales by Comparable Competition)

Out of 402 total designs, 154 were new SoC designs or designs converted from hybrid to SoC. This number is approximately the total number of PLC designs that were re-architected in 2013, and represents 38.3% of all new designs that used an FPGA. Data in 2014 and 2015 continue this trend with an increase in the percentage of SoC adoptions in new or re-architected designs.

Benefits of Using SoCs in PLC Architecture

Manufacturers who use SoCs in PLC architectures derive the following benefits[1]:

- High performance
  - 4,600 DMIPs for less than 1.8 W
  - Up to 1,600 GMACs and 300 GFLOPS based on >125 Gbps processor to FPGA inter-connect and cache coherent hardware accelerators
- Lower power—Up to 30% less power vs. a two-chip discrete solution
- Reduced BOM and PCB space and layer cost—Up to a 55% form factor reduction
- Scalability and investment protection—Scalable SoC processor roadmap grows with application needs and protects software development investment
- Flexibility—SoC FPGAs can accommodate software and hardware changes
- Improved time to market

[1] Numbers based on Altera SoC device features, processors, and package designs.

In competitive bid situations, manufacturers who have moved to a flexible SoC-based architecture can outbid those who have not. Additionally, an SoC architecture provides advantages in absolute price, total cost of ownership, scalability, and protection of customer investment. Cost and power efficient SoCs can be rapidly adapted and scaled according to growing and evolving customer needs driven by Industry 4.0 and IIoT. Altera also offers devices, tools, methodology, boards, and reference designs qualified for IEC61508 SIL3 functional safety.

Accelerating Adoption of a SoC FPGA Platform Ready for Industry 4.0

When working with an SoC FPGA vendor, like Altera, that has a demonstrated commitment to the industrial market, manufacturers receive the additional time-to-market benefits of ready-made solutions and reference designs. These building blocks serve as blueprints for modern PLC architectures.

Altera teamed with 3S Smart Software Solutions (developers of CODESYS), EXOR International (a leader in HMI development), and Barco Silex (a security and encryption IP leader) to create a single-chip PLC design using the ARM®-based Cyclone® V SoC. This design implements control, EtherCAT, HMI, and secure enterprise communication over OPC-UA in a micro system on module (microSoM) that is less than half the size of a credit card. As of November 2015, Altera has also demonstrated a Smart Factory design comprising three of these PLCs connected over an IEEE 802.1 TSN backbone and working with complete determinism, featuring 802.1 TSN IP from TTTech, a pioneer in ensuring reliable networks.

The typical 15-year life-cycle of Altera SoCs, which is much longer than that of discrete processors, combined with scalable processing platforms, provides protection against obsolescence and preserves software investment.

With its ready-made microSoM, PLC evaluation design, available IEEE 802.1 TSN and TUV-certified functional safety offerings, the Altera® Cyclone V SoC is the ideal platform to develop PLCs ready for Industry 4.0 with fast time to production.

Document Revision History

Table 3 shows the revision history for this document.

Table 3. Document Revision History

Date	Version	Changes
December 2015	1.0	Initial release.