

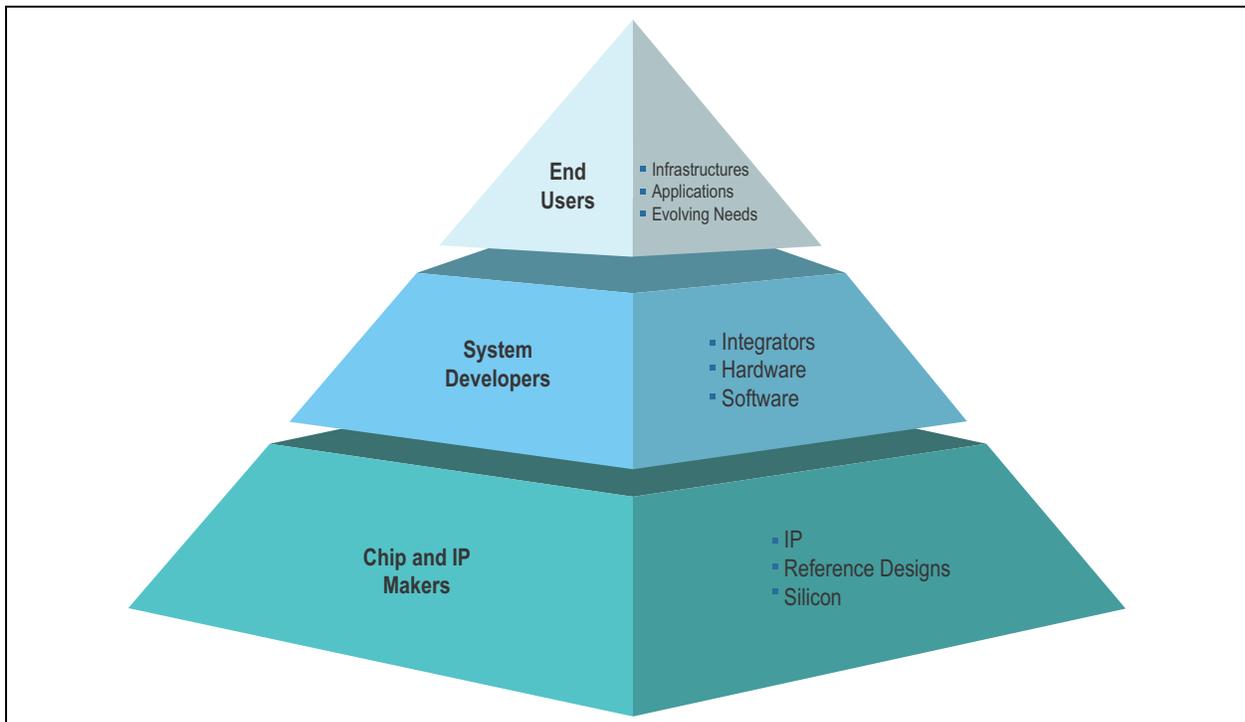
Intellectual property (IP) is a key component in system designs for many different market verticals. The IP in these system designs are either designed in-house or by a third party. Today's challenging economics with internal design teams make the question of building or buying IP more important and can add risk.

In this paper, we present and demonstrate an innovative model for IP scalability, integration, and delivery. We examine the need to simplify the entire process of acquiring, evaluating, testing, and integrating IP into a design. This innovative model helps system developers mitigate the risk of using third-party IP and meet their shortened time-to-market windows.

Introduction

The demand to go faster with fewer resources is at the heart of businesses - big or small. Driving this demand is the need for scalable and intelligent systems to replace outdated infrastructures incapable of handling the recent explosion of data for applications such as cloud computing, big data, and social media.

Figure 1 displays the challenges that have to be addressed at each level of the supply chain to meet the explosion of data.

Figure 1. Supply Chain Integration Challenges

The big picture is both challenging and compelling. For system developers, the first question should be —what are our true in-house IP competencies and what IP competencies can be leveraged from third-party sources?

There are numerous factors to take into account when deciding whether to build or buy IP. You can think of the scenarios as a puzzle. These pieces of a puzzle when apart mean nothing, but when put together, become a picture. That picture is the solution. The pieces need to be created with a focus on solving the problem. These pieces refer to the blends of IP that, when stitched together, form the solution. These IP pieces are built to include certain feature sets, performance specifications, and also to adhere to existing protocol standards so they can be connected to other IP pieces. After the IP parameters and specifications are identified, system developers have to consider the following questions:

- Does this IP already exist in-house or is it available from a third party?
- How long does it take for a team to build it?
- Does the in-house team have the expertise and funds to build it?
- How robust and mature is the IP from a third party?

Keeping these questions in mind, how can we change our strategy to meet the end customers' performance requirements, short timeframes, and price pressures?

Basically, the development model has to change. System developers cannot keep following the old model of developing every IP in-house. Altera provides a differentiated IP model to enable system developers to continue providing their solutions without losing any ground in performance, schedules, and costs.

The following sections will describe how Altera and its partners address system developers' concerns by providing the necessary designs, evaluation tools, process flow, and techniques to increase IP performance and productivity.

IP Delivery—Simplified IP Logistics Process Flow

The first consideration is the availability and accessibility of the IP.

Altera provides a simplified IP logistics process flow called OpenCore Plus to enable the fast acquisition, evaluation, and licensing of various IP for system integration. This process not only allows the simulation and compilation of the IP, but enables the testing and validation of the prototype design on actual hardware.

Figure 2 shows the process flow and explains how a customer navigates through simple steps to immediately integrate an IP into a design.

Figure 2. OpenCore Plus Feature Process Flow



Altera IP Solutions

Altera® FPGAs, coupled with Altera and partner IP, provide the right combination to handle various application demands. The IP is delivered in a variety of packaging – whether hardened in silicon, provided as a soft IP, or as a reference design. This unique blend of IP provides you the flexibility to solve your design challenges.

IP Scalability and Integration

Although the need to maximize bandwidth and feature performance is essential on systems, so is the need to easily integrate subsystems. This is where performance and productivity are both needed to enable unique solutions. Altera's position as a vertically integrated company that develops silicon, IP, and reference designs enabled the creation of an innovative IP model that can easily provide higher levels of scalability and integration. To do this, Altera uses a multi-staged silicon and IP strategy to determine the right blends of soft and hard IP. There are three major stages that feed into the strategic architecture model:

1. A field stage, which provides market trends and ongoing feedback.
2. A silicon and IP innovation stage.

3. A development and validation stage, which aligns all design teams across the planning, integration, and verification stages.

These three stages enable Altera to determine the right combinations of soft and hard IP to provide the scale and integration required for the IP portfolio.

Furthermore, Altera is committed to its IP partner to provide the required support and as much inside detail as possible to enable them to emulate the same vertical integration model. This benefits both sides to be more effective and competitive in selling solutions.

Vertical integration serves as a great competitive strength, but this is not the only aspect that can be leveraged. To further differentiate, Altera has continued to reduce silicon geometries and has implemented an IP model that encompasses innovative design techniques. The innovative design techniques included on Altera's soft IP are as follows:

Table 1 lists the design attributes to deliver higher IP scalability and integration.

Table 1. IP Design Attributes

Scalability	Integration
<ul style="list-style-type: none"> ■ Reduced IP logic utilization ■ FIFO control algorithm 	<ul style="list-style-type: none"> ■ 15% IP core timing margin ■ Consistent clocking across design domains

These design advantages, coupled with the benefit of silicon geometry reductions, provide the following benefits:

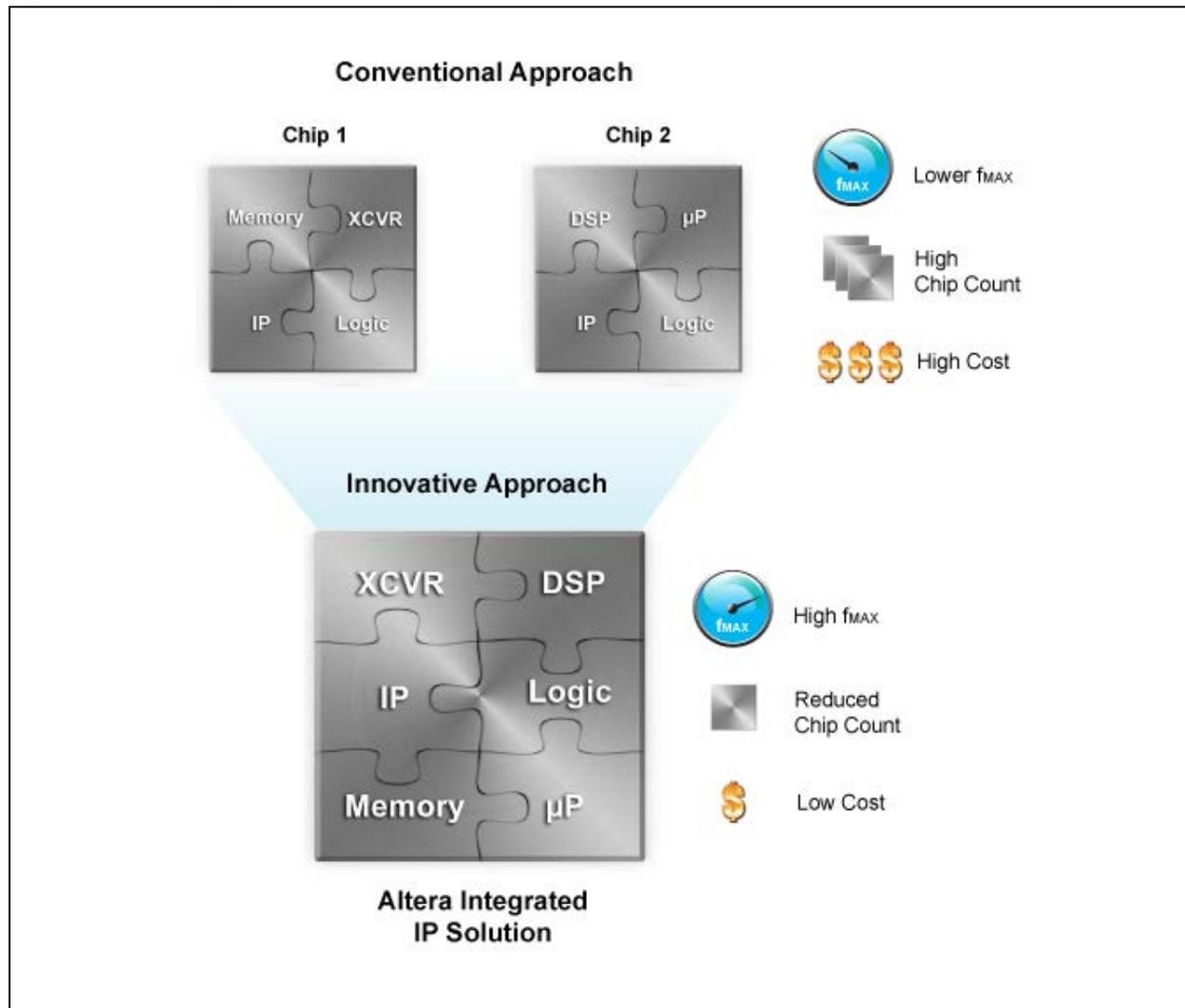
- Simplified and faster timing closure and device fit
- Higher design f_{MAX} to scale system performance
- Efficient data processing for various workloads
- Higher user logic and IP subsystem integration at a reduced cost
- Rapid time-to-market deployments
- Increased management and customer satisfaction at all levels

In addition, the innovative Altera IP model includes the right enhancements to account for various software knowledge levels - whether a novice, intermediate, or expert. Streamlining the IP design blocks and leveraging the hard IP on Altera's FPGA silicon has greatly enhanced the IP subsystem scalability and integration for system designs.

One attribute cannot be successful without the other. Altera has tightly coupled the benefits of scalability and integration to help you maximize bandwidth, increase performance, and achieve faster multiple IP integration on a single device.

Figure 3 shows how Altera's proven IP model enhances integration and scalability for system development. A comparison of the key benefits is also displayed.

Figure 3. Higher Integration Enablement



By breaking down the IP further into soft and hard IP, and adding reference designs into the mix, users can see the individual benefits of each, as project needs and decisions vary with regards to how much IP is needed. Here are some of the scenarios a design team may run into:

- Scenario 1: Includes only soft logic in the IP, which provides a great amount of flexibility, but a larger resource count; whereas including only hard logic in the IP provides less flexibility, but at a much lower resource count.
- Scenario 2: Includes a unique combination of soft IP and hard IP to form a design function. This particular scenario reaps the benefits of both sides, which is the ability to provide a good amount of flexibility at a reduced resource count.
- Scenario 3: Includes reference designs, which may leverage a combination of soft and hard IP, but provides a higher level of abstraction of an application-specific function. Note that there are various levels of abstractions that can be recognized in a specific reference design.

Figure 4 shows the productivity and performance attributes for each type of design scenario.

Figure 4. IP Scenario Benefits

All Soft or All Hard IP	Combined Integration of Soft and Hard IP	Reference Designs
<ul style="list-style-type: none"> ■ Soft IP designed with 15% timing margin provides faster design timing closure ■ Soft IP enables high configurability, which allows the efficient optimization of features and datapaths ■ Hard IP minimizes logic resources, power, and timing concerns 	<ul style="list-style-type: none"> ■ Combined performance strengths optimizes the solution ■ 15% timing margin and logic resource savings ■ Simplified integration with high configurability 	<ul style="list-style-type: none"> ■ Enhanced time to market ■ Reduced engineering resources; specific expertise not required for design integration ■ Simple modifications for performance tuning

Performance and productivity gains are at the forefront of every decision that Altera and its partners make. The ability to scale performance and productivity going forward are paramount to achieve the end solutions for existing and next-generation applications. Altera and its partners continue to enable users to scale IP usage and fit more IP on a single device to meet tough application specifications at a lower cost.

Vertical Market Coverage Provides IP Quality and Robustness

The Altera and partner IP portfolio provides solutions that cover ten vertical markets. These solutions consist of a wide variety of IP that includes both soft IP and hard IP to provide the utmost flexibility, performance, and integration.

By covering multiple verticals, Altera and partners provide robust IP to ensure the highest quality. Altera IP cores are capable of supporting numerous applications for different markets. During the development phase of the IP, Altera takes into account the IP performance scalability, flexibility, and dynamic qualities needed to be successful across various applications and markets. In addition, by being part of numerous internal evaluation tests, Altera IP are thoroughly tested before it ships, thereby reducing the time needed for simulation and hardware debug.

With over 400 IP cores and reference designs, Altera and its partners are helping to pave the way for the next stratum of portfolio performance and productivity. Figure 5 identifies some of the key markets to which the IP portfolio caters to.

 For a complete listing of verticals and Altera IP, refer to the [All Intellectual Property](#) page on the Altera website.

Figure 5. Key Markets Serviced by Altera IP



Altera continues to expand its core capabilities and joins forces with highly specialized IP partners to enable the features required by the emerging applications across these markets.

What's Next?

The future of IP performance and integration are rapidly changing as end user needs are expanding and system design houses are required to keep up. These trends will continue to require an innovative IP model. Altera and partners are responding by providing that IP model and the building blocks to enable more intelligent functionality, reduce every nanosecond of data travel time, and squeeze every Gbps and IOPS out of your system, to provide you the differentiation you need to support these more intelligent, higher bandwidth, and performance-hungry applications.

An evolving paradigm calls for the introduction of smarter, simpler, higher performance, and rapidly integrate-able IP subsystems. Altera and partners are developing the right IP solutions for the many new generations of systems to come.

Conclusion

In this paper, we discussed the building or buying IP scenario faced by system development teams. As shown throughout the paper, the need to buy IP is becoming the more economic option. Altera's IP model solves these economic challenges and delivers the unbound IP scalability, integration, and delivery that system design houses require to make greater, competitive impact.

References

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- Phillip Swart, IP Marketing Manager, Software and IP, Altera Corporation

Document Revision History

Table 2 lists the revision history for this document.

Table 2. Document Revision History

Date	Version	Changes
September 2013	1.0	Initial release.