

Lowest system power can be achieved by utilizing low-power FPGAs, which can be more power efficient than processors, ASSPs, and ASICs. When evaluating low-power FPGAs, key considerations include the power efficiency of the process technology, architectures and features, system interconnects, and EDA software. Altera® Cyclone® V FPGAs excel at all of the above metrics, and do so at the lowest system cost.

## Introduction

As new systems are developed, designers turn to the newest semiconductor technology to provide the performance necessary to satisfy increasing market demands. Over the years, semiconductors have achieved higher performance levels, but they have done so at the expense of increased system power consumption.

Traditional approaches to achieving next-generation performance levels are no longer feasible, due to factors including diminishing performance returns per unit power, maximum clock frequency limits, absolute thermal maximums, constraints on system-cooling capacity, and higher costs associated with power systems (operating expenses for cooling and capital expenses for larger facilities needed when thermals limit system density).

 For more information about the importance of low-power system design, read the *Meeting the Low Power Imperative at 28 nm* white paper.

Today, system designers must utilize data-level parallelism to address increased system performance requirements within a constrained or shrinking system power budget. CPUs have adjusted from scaling the core clock frequency of single-thread/single-core processors, to scaling the number of threads and cores. General-purpose graphics processing units (GPGPUs) and scale out big data architectures offer improvements in performance-to-power ratio over single CPUs, but the ultimate expression of data-level parallelism can be found in ASICs and FPGAs. At 28 nm, FPGAs offer substantial benefits unmatched by ASICs, and only FPGAs are fully configurable.

## Process Technology

While improvements in semiconductor process technology, by themselves, are no longer a panacea of lower cost, lower power, and higher performance, devices using the latest process technology do provide important benefits to system designers. For example, smaller process geometries allow for lower capacitance and shorter interconnects, which decrease dynamic power. An examination of approximately 100 customer designs shows 30% of total power is attributable to signal routing, so this is very significant in the chip's overall power budget.

Cyclone V FPGAs are built on TSMC's 28-nm ultra-low power process technology (28LP), using proven polysilicon gate and silicon oxynitride gate dielectric (Poly/SiON). 28LP is the same low-power process technology used to achieve ultra-low-power operation for mobile handsets. Cyclone V FPGAs use variable channel lengths and multi-threshold voltage transistors to minimize leakage. Standard and low-threshold transistors are used only when required to achieve performance. In concert with a reduced core voltage, these innovations allow Cyclone V FPGAs to achieve up to a 40% total power decrease from the previous generation.

## Architecture and Features

Altera's key architectural features include hard intellectual property (IP), partial reconfiguration, logic density granularity, embedded memory granularity, PLLs, and the ARM® Cortex™-A9 MPCore™ Processor System.

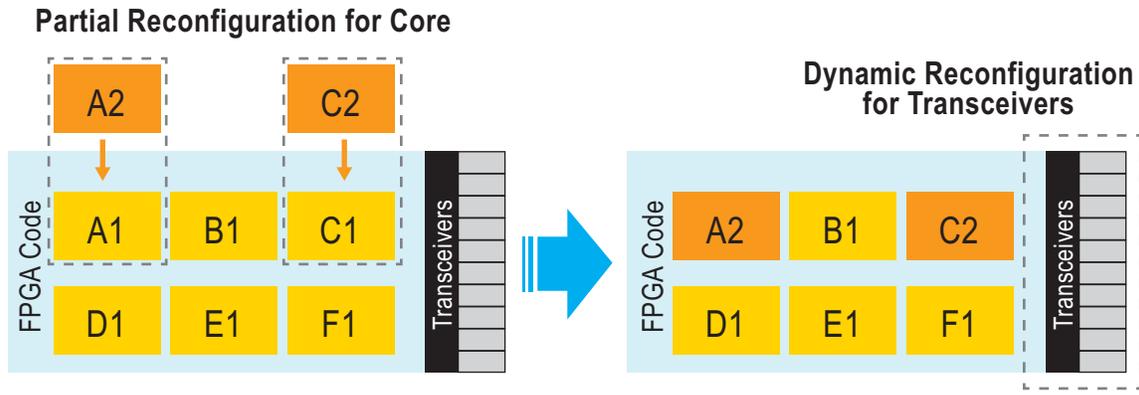
### Hard IP

FPGAs provide wide flexibility by allowing system designers to implement virtually any function. Nonetheless, there are a number of common functions required by a diverse set of applications across different markets. For example, over half of FPGA designs today contain an external memory interface to take advantage of plentiful cost-efficient DRAM. By hardening the IP required to implement this common function, Cyclone V FPGAs are able to achieve not only lower development cost and higher performance, but also greater power efficiency, due to smaller block size and associated reductions in capacitance and elimination of programmable interconnect fabric.

## Partial Reconfiguration

Partial reconfiguration allows one logic function block to replace another logic function block during system operation, as shown in [Figure 1](#).

**Figure 1. Partial Reconfiguration During System Operation**



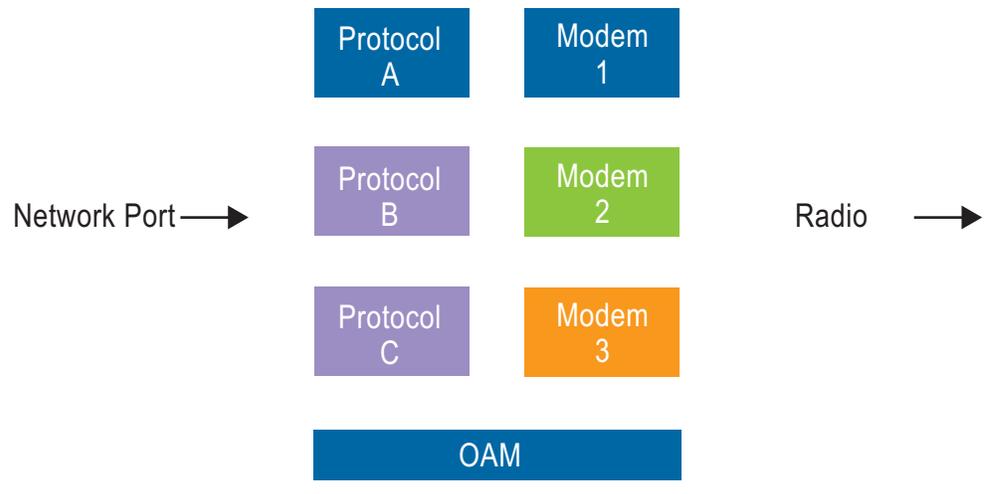
FPGAs have always offered an advantage over fixed function devices like ASICs and ASSPs, due to the efficiency of hardware programmability. As listed out in [Table 1](#), partial reconfiguration extends this efficiency and power advantage further by allowing the reuse of blocks that change during system operation. As a result, systems do not need to support every piece of desired functionality all the time, thus enabling the designer to use a smaller device with lower static power.

**Table 1. Device Technologies and their Required Logic**

Technology	Required Logic
ASSP	Superset of all functionality for <b>all systems</b> of <b>all customers</b> .
ASIC	All functionality required by <b>all systems</b> of <b>one customer</b> .
FPGA	Only the functionality needed in <b>one particular system</b> .
FPGA with Partial Reconfiguration	Only the functionality needed for <b>one particular system</b> at <b>one particular time</b> .

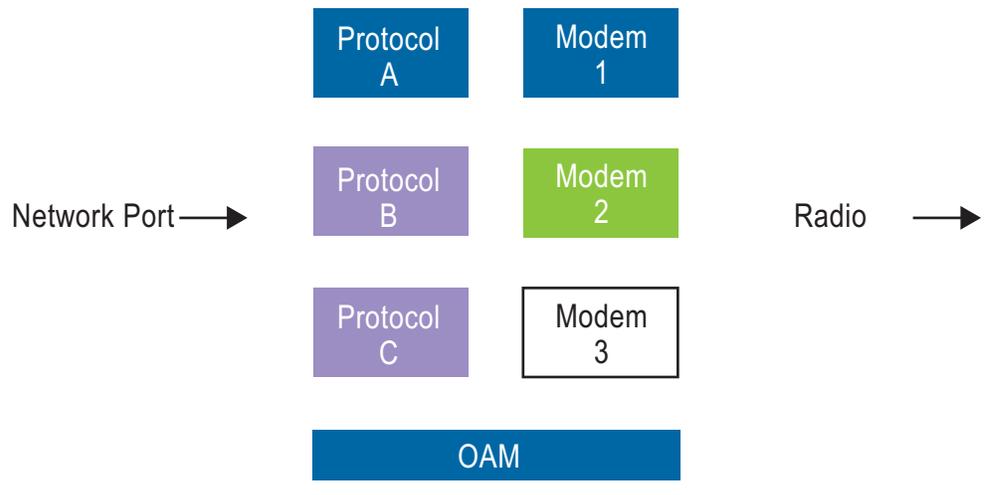
ASSPs include logic to support all functionality for all customers, as shown in [Figure 2](#).

**Figure 2. ASSP Implementation**



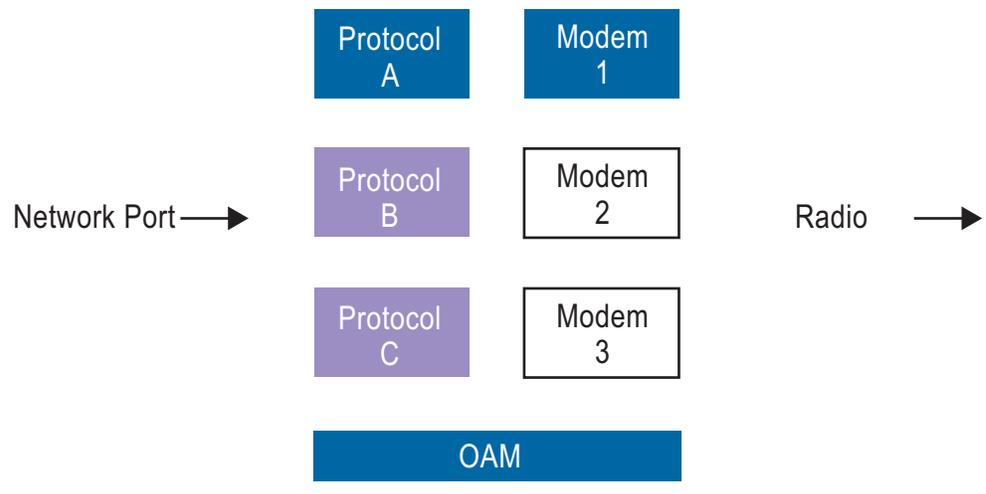
ASICs only need to support functionality used by one customer, and can drop modem 3, as shown in [Figure 3](#).

**Figure 3. ASIC Implementation**



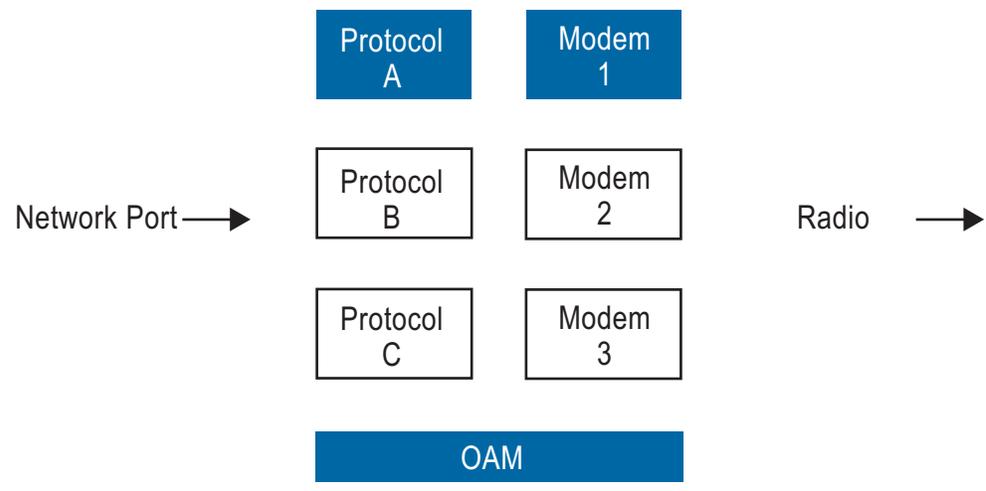
FPGAs only need to support functionality used in one design for one customer, and can drop modem 2, as shown in [Figure 4](#).

**Figure 4. FPGA Implementation**



FPGAs using partial reconfiguration need only contain logic for the active protocol. Since protocols A, B, and C are mutually exclusive at any given point in time, an FPGA with partial reconfiguration can exclude the logic needed for protocol A and protocol B, when the network port is using protocol A, as shown in [Figure 5](#).

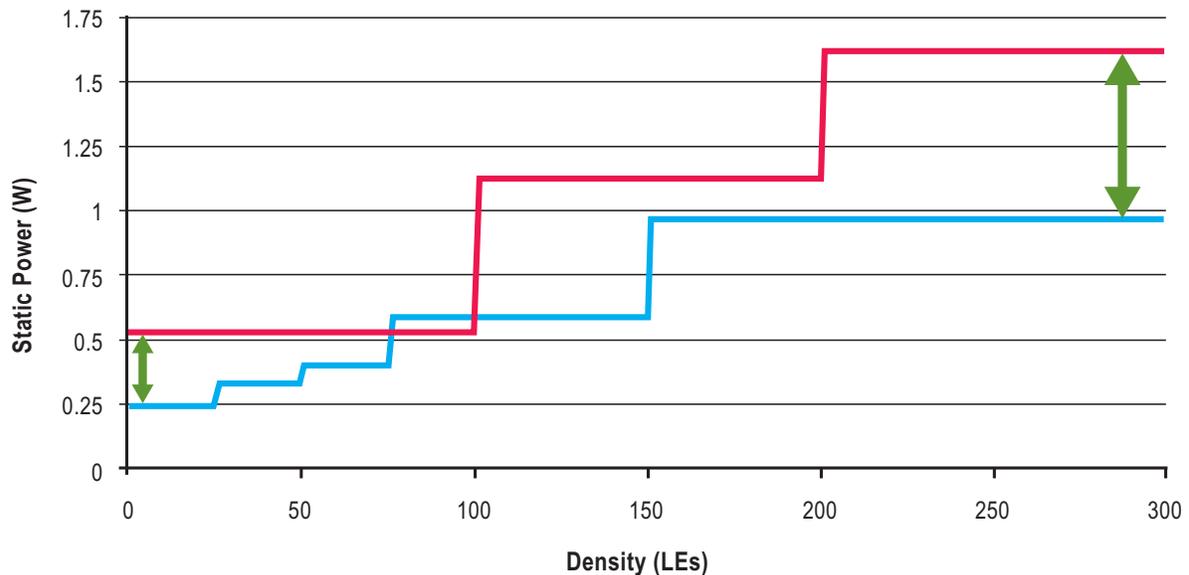
**Figure 5. FPGA Implementation Using Partial Reconfiguration**



## Logic Density Granularity

In FPGAs, static power scales with device density. Therefore, the lowest power FPGA should closely match the system requirements. If a larger FPGA needs to be used, because the minimum density offered is too high, a static power penalty is imposed. Cyclone V FPGAs offer a rich granularity of density offerings to ensure systems have the lowest static power, and hence the lowest total system power. Figure 6 illustrates how Cyclone V FPGAs have the lowest static power for almost every amount of logic. In competing 28-nm FPGA families, the lack of a full range of low-density offerings imposes a significant power penalty.

**Figure 6. Static Power Advantage of Higher Logic Granularity<sup>(1)</sup>**



**Note to Figure 6:**

(1) Conditions: 85°C junction temperature, maximum process, commercial grade.

## Embedded Memory Granularity

Small memories are ideal for wide and shallow memory arrays, which require a number of ports per bit of memory. In addition to embedded M10K SRAM with 10 Kb of storage, Cyclone V FPGAs include 640-bit memory logic array blocks (MLABs). Small embedded MLABs can improve power consumption of shallow FIFO buffers by offering increased utilization compared to larger embedded SRAM blocks. For example, a 32-bit-wide, 10-word-deep FIFO buffer requiring 320 bits of memory would have utilization of only 3% using a standard 10K embedded SRAM block, but could be implemented with only a single smaller 640-bit MLAB with 50% utilization. Cyclone V FPGAs implement these smaller MLABs throughout the FPGA fabric for convenient localized access, which also reduces power associated with routing to a distant SRAM.

## Phase-Locked Loops

A fractional phase-locked loop (fPLL) is a highly flexible PLL, which helps to reduce system cost by eliminating external voltage-controlled crystal oscillators (VCXOs). In addition, fPLLs are highly power efficient due to use of binary-value delta-sigma modulation (DSM). Cyclone V FPGAs include up to eight fPLLs, providing system designers with plentiful resources to achieve lowest system cost and power.

## ARM Cortex-A9 MPCore Processor System

On-die integration of external components can reduce system power due to lower I/O power requirements. Cyclone V SoC FPGAs integrate an ARM Cortex-A9 MPCore processor system, with a host-class application processor and complete peripheral set, directly onto the Cyclone V FPGA die. This integration can save up to 30% system power, compared to a two-chip solution.

Cyclone V SoC FPGAs were designed with power management in mind. An independent FPGA power plane allows for low-power operation. Additionally, the hard processor system (HPS) supports power management from software. Software-controlled options include:

- PLL and clock divider control
- Clock domain gating
- Processor sleep modes
- Low-power memory controller modes

## System Interconnect

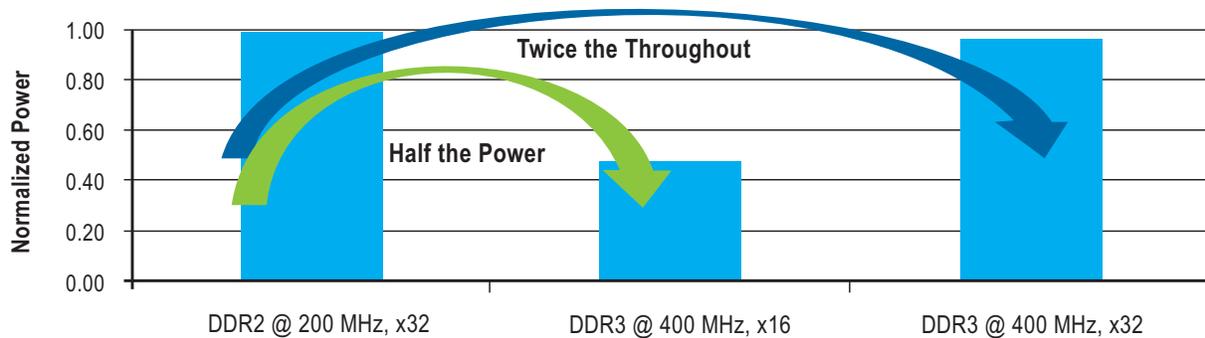
As total power shrinks, a larger component of power is I/O related. By taking advantage of new I/O capabilities, this power component can be reduced.

## DDR3 SDRAM

Cyclone V FPGAs support DDR3 SDRAM external memory at up to 400 MHz. With the faster throughput per pin, designers can achieve a given memory bandwidth with a narrower interface. In addition, DDR3 SDRAM components support lower voltages than previous-generation DDR2 SDRAM components, further reducing power.

Figure 7 shows how reduced memory interface data bus width and reduced voltage combine to lower total system power.

**Figure 7. SDRAM Data Bus I/O Power**



Additionally, Cyclone V FPGAs include a multiport front-end hard IP, which allows designers to easily optimize sharing of a single DDR3 memory interface. Sharing a common memory interface reduces the number of I/O pins and external components that consume power. Compared to ASSPs, which can support only a single instance of a given function, FPGAs can support multiple instances of the function, without wasting numerous devices.

## LPDDR2 SDRAM

Compared to traditional non-power-aware memory interfaces, such as DDR2 or DDR3 SDRAM, LPDDR2 SDRAM achieves power saving, through a combination of low voltage (1.2 V) and advanced power management features. LPDDR2 SDRAM manages array refresh with power-aware capabilities including:

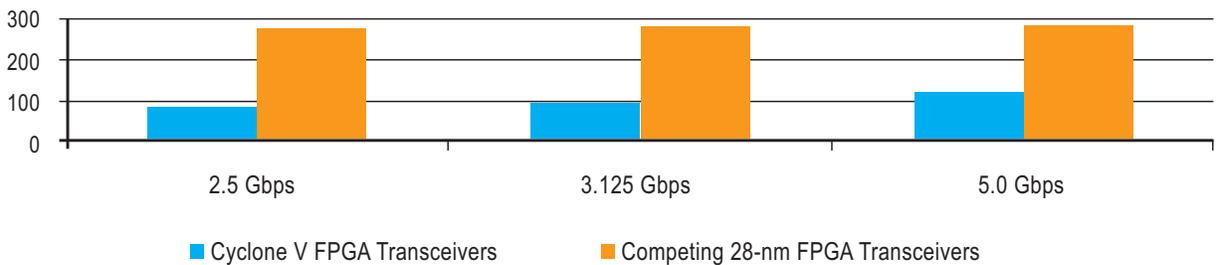
- Temperature-aware refresh—Reduces refresh rates at low temperatures
- Partial array self-refresh—Allows powering down unused portions of the memory array
- Deep power-down—Saves power when preserving memory array, and contents are not required

Cyclone V FPGAs include support for low-power LPDDR2 SDRAM interfaces, so that system designers can take advantage of these system power savings.

## Transceivers

High-speed transceivers offer a way to exchange data at high bandwidths, with dramatically fewer on-PCB resources. Using high-speed transceivers, Altera's Cyclone V FPGAs offer the lowest power per bandwidth available on FPGAs today, as shown in [Figure 8](#).

**Figure 8. Transceiver Power (mW) per Channel <sup>(1)</sup>**



**Note to Figure 8:**

(1) Conditions: T<sub>J</sub>=85°C maximum process, commercial grade.

## Power-Aware Productivity Software

Power-aware EDA design software provides additional tools for achieving the lowest system power. The following are some of the tools provided by Altera's Quartus® II design suite:

- Memory transformation—Switches read/write enable signals to read/write clock enable signals for lower power
- Power-aware memory balancing—Minimizes the number of SRAMs simultaneously active by restructuring address decode logic when aggregating multiple physical SRAMs into a larger logical memory
- Soft power-down—Automatically implements low-power mode for unused FPGA resources, includes M10K SRAMs, variable-precision digital signal processing (DSP) blocks, PCI Express® (PCIe®) hard IP blocks, hard memory controllers, and fPLLs
- Design Space Explorer (DSE)—Automatically sweeps all possible design implementation options to find the lowest power implementation

 For more information about the power-aware design tools available in the Quartus II design suite, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

## Conclusion

Lowest system power can be achieved by using low-power FPGAs built on 28LP process technology, with power efficient architectures and features, system interconnects, and EDA productivity software. Cyclone V FPGAs were designed with all of the above characteristics, thereby offering an excellent route to lower system power at the lowest system cost.

## Further Information

- White Paper: *Meeting the Low Power Imperative at 28 nm*  
[www.altera.com/literature/wp/wp-01158-low-power-28nm.pdf](http://www.altera.com/literature/wp/wp-01158-low-power-28nm.pdf)
- Delta-sigma modulation  
[http://en.wikipedia.org/wiki/Delta-sigma\\_modulation](http://en.wikipedia.org/wiki/Delta-sigma_modulation)
- *Power Optimization* chapter of the *Quartus II Handbook*  
[www.altera.com/literature/hb/qts/qts\\_qii52016.pdf](http://www.altera.com/literature/hb/qts/qts_qii52016.pdf)

## Acknowledgements

- Michael Smullen, Product Marketing Manager, Low-Cost Products, Altera Corporation

## Document Revision History

Table 2 lists the revision history for this document.

**Table 2. Document Revision History**

Date	Version	Changes
March 2012	1.0	Initial release.