First Demonstration of Chip-to-Module Electrical Channel Interoperability over OIF CEI-28G-VSR Compliant Links

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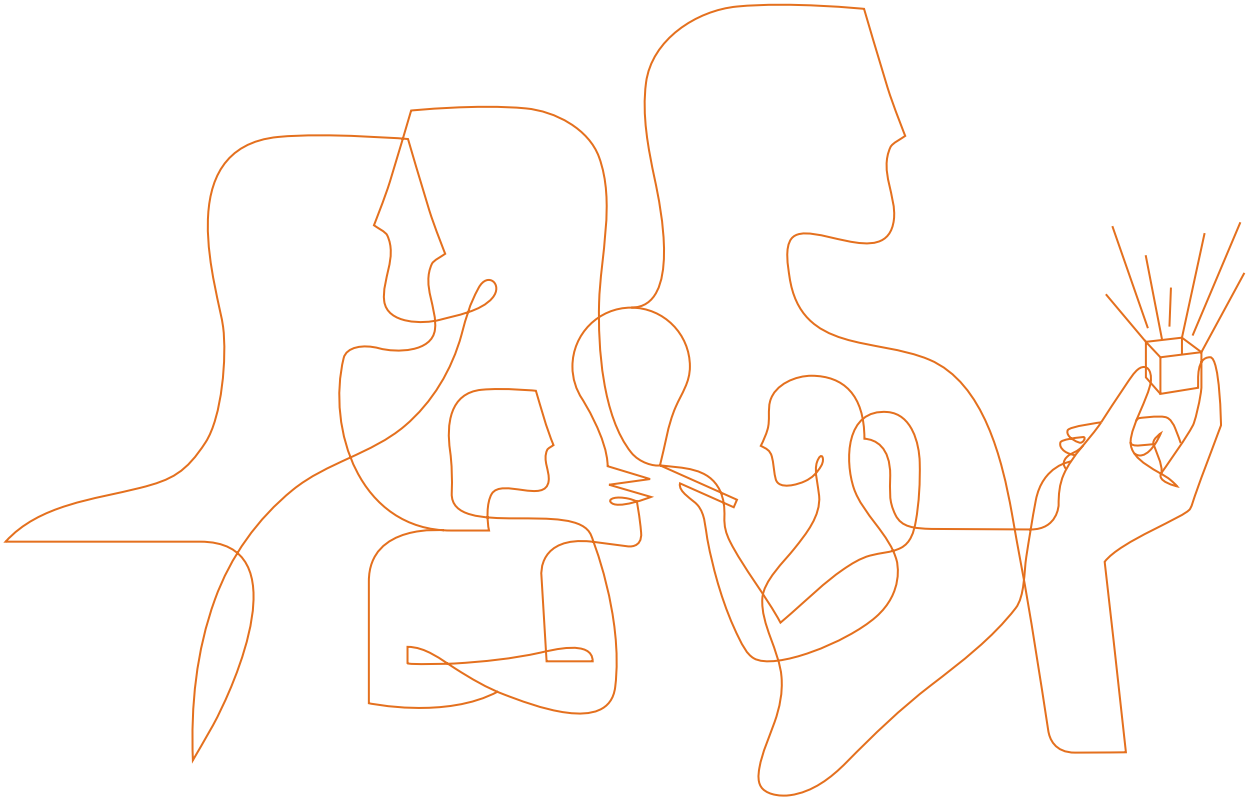

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Abstract:

We propose and demonstrate CEI-28G-VSR 4x25G "chip-to-module" multi-vendor interoperability including jitter performance which is able to maintain overall system interoperability for an IEEE 100GBASE-LR4/ER4 application.

Introduction

Presently, most commercially available optical modules for high capacity applications support system-side electrical interfaces operating at data rates between 10Gb/s and 14Gb/s. Several optical standards are now under development that will more than double this operating range, to data rates between 25Gb/s and 32Gb/s. For example, working groups of several standards bodies are now defining the OIF CEI-28G-VSR, 32G Fibre Channel, and IEEE 4x25G chip-to-module interfaces.

Another factor driving the increase in system-side data rates is the need for higher faceplate densities. The consequent trend to smaller optical module form factors and lower power dissipation mandate a narrower system-side bus operating at a higher rate [1]. For example, the IEEE 100GBASE-LR4 CFP module form factor uses the CAUI system interface operating at 10.3Gb/s per lane. This MSA will shortly be followed by a smaller, lower-power form factor MSA dubbed CFP2 that uses the narrower 4x25G "CAUI-4" system bus. CAUI-4 lanes operate at 2.5 times the 10G CAUI rate, allowing the 10:4 IEEE PMA "gearbox" function to migrate outside the module and on to the line card.

A new challenge arises for these next-generation optical modules. While the module must support an adequate reach to the host IC, the higher 25G line rate implies greater jitter accumulation in the electrical link due to physical losses and reflections among the elements of the PMD function. The module must somehow accommodate or reduce this additional jitter without impacting the overall jitter and bit error rate (BER) performance requirements of the optical line interface.

A Clock and Data Recovery (CDR), or retimer, function within the optical module will reset the transmit and receive link jitter budgets, reducing the amount of equalization needed in the module to close the electrical link. This approach takes advantage of the equalization functions already present in the host IC's serial transceivers to do the heavy lifting. In this way, equalization power is burned on the system side, reducing the power burden on the module. Further, resetting the link jitter budgets inside the module ensures that optical link jitter and BER requirements are met. The module's electrical and optical link jitter budgets are now separated: signal impairments within 25G host-to-module electrical channel do not impact the overall jitter and bit error rate (BER) performance of the optical system.

Overview of OIF CEI-28G-VSR "chip-to-module" electrical channel requirements

The industry-sponsored OIF consortium is presently defining an Implementation Agreement (IA) termed CEI-28G-VSR specifically to address electrical channel requirements of the higher-rate 19.6Gb/s to 28.05Gb/s chip-to-module applications [2], [3].

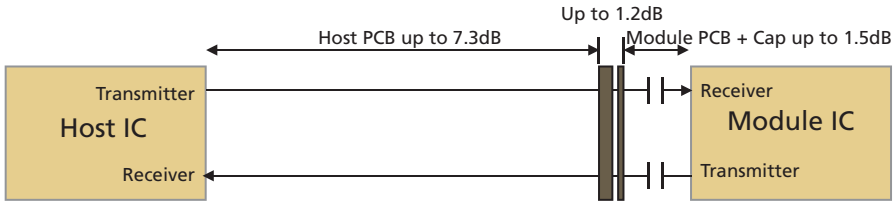

Figure A: OIF CEI-28G-VSR chip-to-module electrical channel

The 28-VSR IA electrical channel is required to perform at a BER < 1E-15 over a bus consisting of four or more electrical channels having up to 10dB–11dB of insertion loss (IL) at the maximum Nyquist rate of 14.0GHz. Other RF channel characteristics such as return loss (RL), insertion loss deviation (ILD) and crosstalk need to be within acceptable limits in order to qualify as being equalizable by the 28G IA.

Other key system transceiver parameters include the maximum allowable transmitter amplitude and jitter generation at the bus transmitters, and the required receiver jitter tolerance at the bus receivers, with prescribed amounts of equalization. The present generation of 10Gb/s chip-to-module interfaces includes IEEE Annex 83 CAUI, which only mandates transmitter-side equalization consisting of up to 6dB of de-emphasis. For the new higher-rate channels a different equalization strategy is planned, allowing both transmitter equalization (e.g. linear FIR), receiver equalization (e.g. CTLE), or a combination of both, to meet the far-end receiver's signalling and jitter requirements.

Simulations and prototype measurements of the new 28Gb/s VSR electrical channel exhibit well-behaved electrical characteristics that help to reduce overall link equalization requirements. At the moment, realistic VSR IA electrical channels can be sufficiently equalized by providing up to 6dB–7dB of CTLE-based equalization within the receiver. (Some transmitter pre-cursor de-emphasis has been shown to help but only with longer channels.) The present overall loss budget of 10dB from the host ASIC to the module retimer chip allows for approximately 3 to 6 inches of trace length, depending upon the host PCB material. A reach of 6 inches is possible with a very low-loss dielectric material such as Megtron-6, while lower performance material such as FR4-08 can achieve a 3-inch reach.

One of the important initial drivers for a higher-speed electrical interface was the migration of the present CFP pluggable module form factor to a smaller, lower power version to improve faceplate density and system thermal requirements.

In the transmit direction, a CTLE as described above can be implemented within the module for negligible additional power consumption if a CDR is used to recover the electrical signal. The CDR is able to effectively reset the transmit jitter budget and allow for a very clean eye with minimal jitter to be launched onto the optical fiber.

Low-jitter CDRs also aid in reducing optical module power by reducing the amount of electrical channel equalization required in the receive direction. A low-jitter retimer facing the optical line receiver PMD block serves the purpose of resetting the received incoming jitter from the laser and optical fiber as well as the additive jitter from the photodiode-TIA. This enables robust signal detection within the module, while providing the host IC receiver with sufficient SNR to recover the signal with minimal overall equalizer power consumption.

Results and discussion of OIF CEI-28G-VSR physical layer optical module interoperability testing

The first ever chip-to-module interoperability testing using commercially available silicon was carried out on a prototype system (see Figure B below).

The host IC was an Altera 28nm CMOS Stratix V FPGA and the module ICs consisted of Gennum CDRs operating at 25.8Gb/s. The CEI-28G-VSR channel was comprised of:

- a short PCB trace on the Altera Stratix V Signal Integrity board
- a VSR host trace board, manufactured in several trace lengths
- a new 25G-QSFP+ connector designed to operate at data rates greater than 25Gb/s, mounted on the VSR host trace board
- a short 1-inch PCB trace with AC coupling capacitors mounted on a small board representing an optical module PCB

The smaller QSFP+ form factor was chosen for the module PCB in order to demonstrate the relevance of CDRs not only in next-gen 100G CFP2 module applications such as 100GBASE-LR4/ER4, but also to demonstrate their applicability in lower power optical module applications employing VCSEL based lasers for use in short-reach 4x 25-28Gb/s multi-mode systems.

The overall channel loss between the FPGA transceiver IC and module retimer IC is 16dB (note that this loss exceeds the 10dB channel budget as defined in the 28G-VSR specification), and the length of the VSR host trace PCB is 7 inches. All measurements are based upon a PRBS31 data stream. Equalization of the channels requires 6dB CTLE peaking in the receiver and 2-3dB of transmitter de-emphasis. The crosstalk within the system is well behaved: transmit jitter does not degrade appreciably as the number of active channels is increased from one to four transmit and receive data paths.

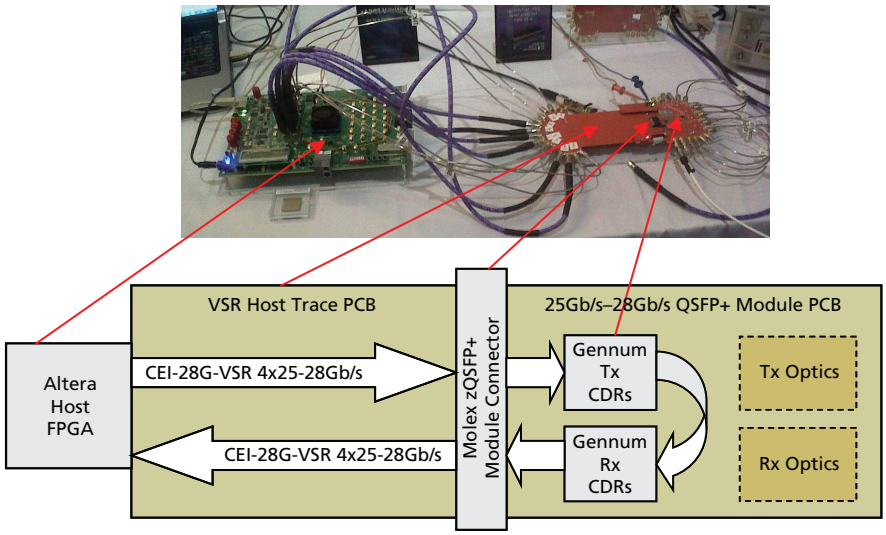

Figure B: CEI-28G-VSR Interoperability Block Diagram and Setup

Figure C shows a scope screen capture of the data eye at the output of the transmit CDR after having equalized the 7-inch VSR channel. The jitter is well controlled and sufficiently low to drive module TOSAs in new applications such as 100GBASE-LR4 CFP2 modules. The random jitter (RJ) of the FPGA transmitter and module transmitting CDR link is measured to be << 300 fs rms. The BER of the link is measured as less than 1e-15.

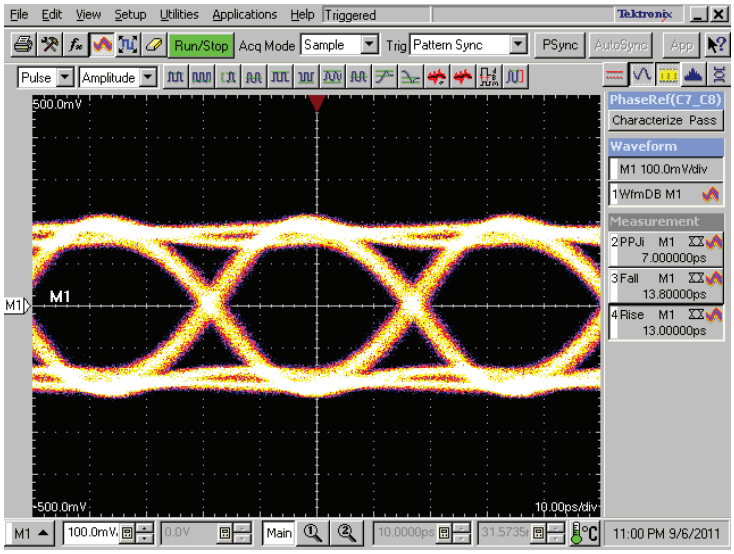

Figure C: Measured 28.0Gb/s eye diagram at output of Tx CDR

Conclusions

High performance data links for next-generation optical modules such as 25G-QSFP+ or CFP2 are now technologically feasible and can yield the required system BER targets (i.e. 1e-15). Systems transceivers with very low jitter generation (i.e, << 300fs rms) are able to reduce their equalization requirements or, as shown in this paper, to extend electrical link distances beyond those afforded by the loss budget specified in the present 28G-VSR IA. Additionally, the ability of the CDR to reset the jitter budget within the module is the key to separating the optical and electrical link budgets. Retimer-based modules will allow 100G optical link budgets to be extended beyond those of 100GBASE-LR4/ER4 applications.

References

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