Achieving Lowest System Cost with Midrange 28-nm FPGAs

WP-01175-1.0 White Paper

As electronic products increase in complexity and capability, the cost to develop and support them also increases from a design and debug perspective, a manufacturing perspective, and an operation and maintenance perspective. This white paper discusses some of the ways in which Altera® Arria® V FPGAs are designed to reduce costs from all of these perspectives.

Introduction

As electronic products increase in complexity and capability, the cost to develop and support them also increases. Longer development time, increased need for design expertise, all costly debug infrastructure all increase the cost of system development. Furthermore, increased complexity adds increased cost in supply chain management and manufacturing, not to mention the increase in operating costs once the system is deployed. To truly save costs, one must evaluate all of these areas early in the design cycle. Altera has focused on this larger cost arena to develop the 28-nm portfolio of FPGAs, specifically in the development of Arria V FPGAs. This white paper discusses some of the ways in which Arria V FPGAs are designed to reduce costs from all of these perspectives.

Reducing Design and Debug Costs

Arria V devices provide several ways for designers to reduce their design and debug costs, including hard IP, intelligent pin placement, proprietary tools and resources, and Altera's unique Virtual Target.

Hard IP

Arria V devices include a large amount of circuitry dedicated to performing the most common functions in FPGA designs. Arria V devices offer the highest number of these "hard" intellectual property (IP) blocks of any midrange FPGA family, and they serve to significantly simplify the overall design process. One of the most time-consuming parts of FPGA design is achieving timing closure, and the hard IP blocks in Arria V devices ease this task by operating consistently and reliably at the specified maximums—particularly the memory controllers, multiport front end, and memory PHY. These specifications can cause timing closure challenges in FPGAs that do not feature hard IP blocks. Figure 1 shows a block diagram of the hard IP blocks in an Arria V FPGA.

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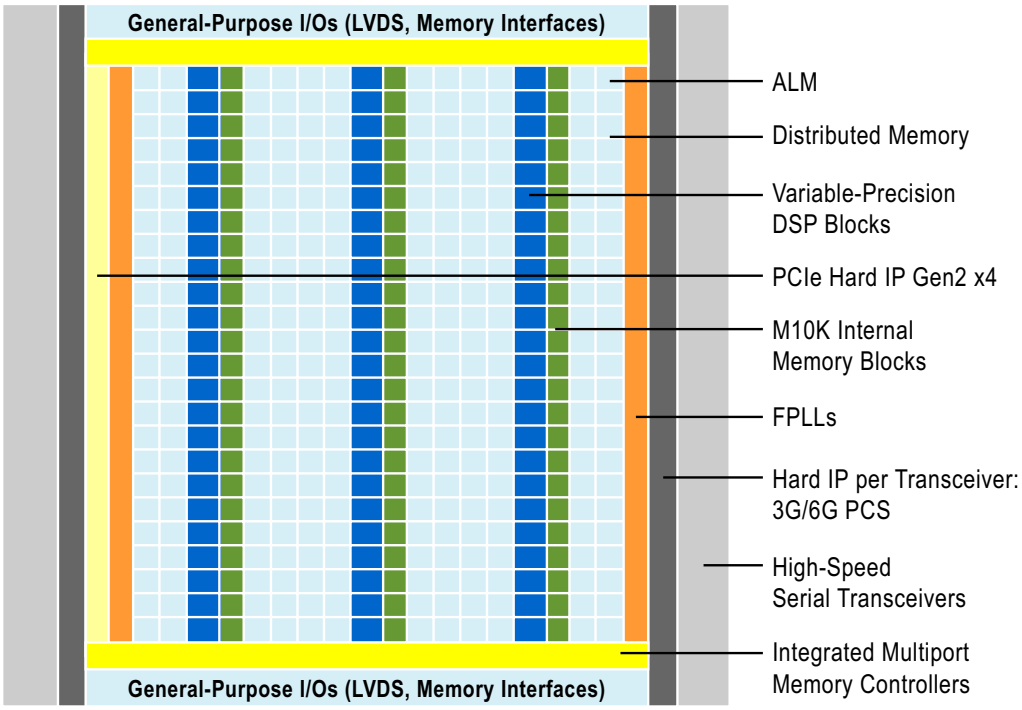
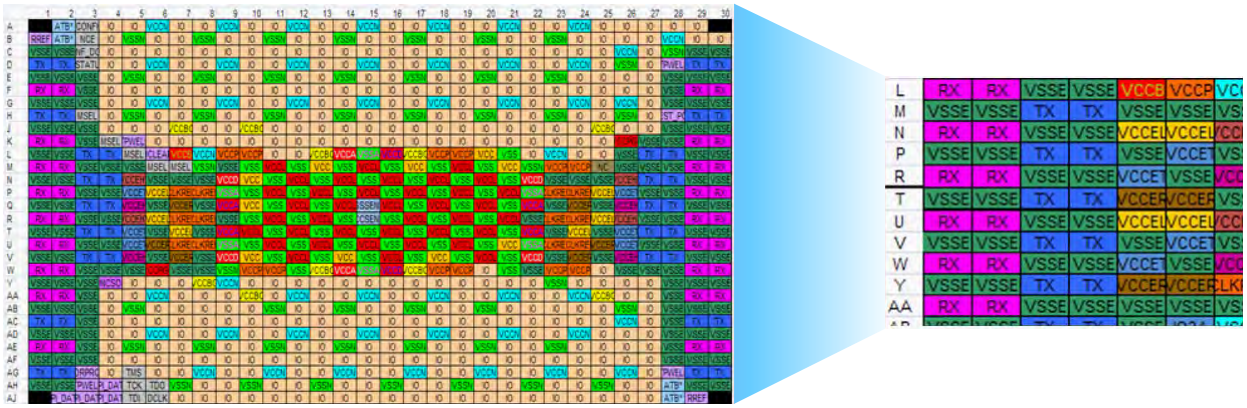
Figure 1. Block diagram of Arria V FPGA



Intelligent Pin Placement

Another way that Arria V devices reduce development time is with their intelligent pin placement, which is designed to ease board layout and maximize signal integrity, and thereby minimize PCB design and debug effort. Figure 2 shows a representative pin layout of an Arria V FPGA on the left side, and expanded detail of the transceiver pin layout on the right side.

Figure 2. Pin Layout of a Representative Arria V FPGA Package



The power and ground pins are placed in a regular, repeating checkerboard pattern, which eases PCB layout. As shown on the right side of Figure 2, the transceiver pin placement is regular and repeating along the outside edges of the device, with a minimal number of TX-pair columns, which also eases layout and reduces PCB layers. The RX pins are placed on the outside of the device, which maximizes their signal

integrity by ensuring that they receive as little interference as possible from possible aggressor signals routed to the device. Finally, the memory interface pins are shielded and placed away from the transceiver pins to minimize the possibility of crosstalk. In these ways, Arria V pin placement reduces PCB layout effort and cost, and minimizes development time.

Tools and Resources

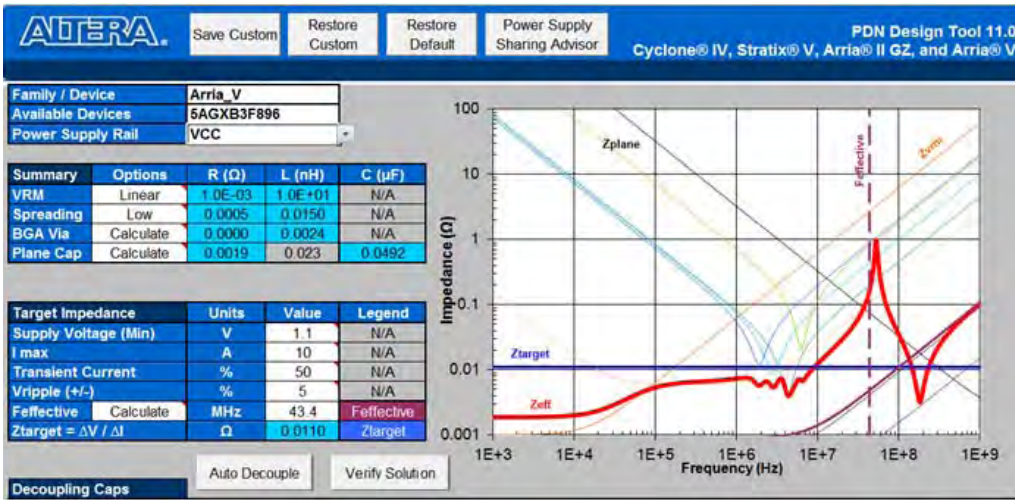
Another way in which Arria V devices minimize design and debug effort is with their comprehensive support tools and resources for designing power distribution networks (PDNs). Unlike other off-the-shelf semiconductors, FPGAs have different switching supply current requirements, depending on their application. As a result, the PDN must be designed to meet the needs of the specific application to supply clean power that avoids violating device specifications and other negative impacts like ground bounce.

To aid in PDN development, Altera offers PDN tools and a Board Design Resource Center. The purpose of the Altera PDN tools is to help the design of a robust PDN for the device in the targeted device family by determining an optimum number, type, and value of decoupling capacitors needed for selected device/power rails to meet the desired impedance targets. This spreadsheet tool is useful for exploring the various what-if scenarios during the early design phase, without extensive and time-consuming pre-layout analysis.

For more information, refer to the Board Design Resource Center on Altera's website.

Altera offers a PDN tool that features each density-package combination of the Arria V FPGA family, ensuring that the exact values for each specific device are included in the calculations to determine the exact PDN characteristics desired by the user. The PDN tool allows the user to select a variety of device characteristics from drop-down menus, and to select the number and values of the capacitors for each power rail. The tool calculates the composite impedance of the PDN along with the impedance characteristics of the voltage regulator module VRM, the decoupling capacitors and their mounting inductance, the PCB, and the FPGA with on-package and on-chip capacitors. By determining the optimal set of decoupling capacitors for a given design in a fast, accurate, and interactive way without requiring a SPICE simulation, the PDN tool eases the board layout process and potentially saves board space, while enabling the user to easily evaluate cost and performance trade-offs. Figure 3 shows a screenshot of an Altera PDN tool.

Figure 3. Screenshot from Altera's PDN Tool

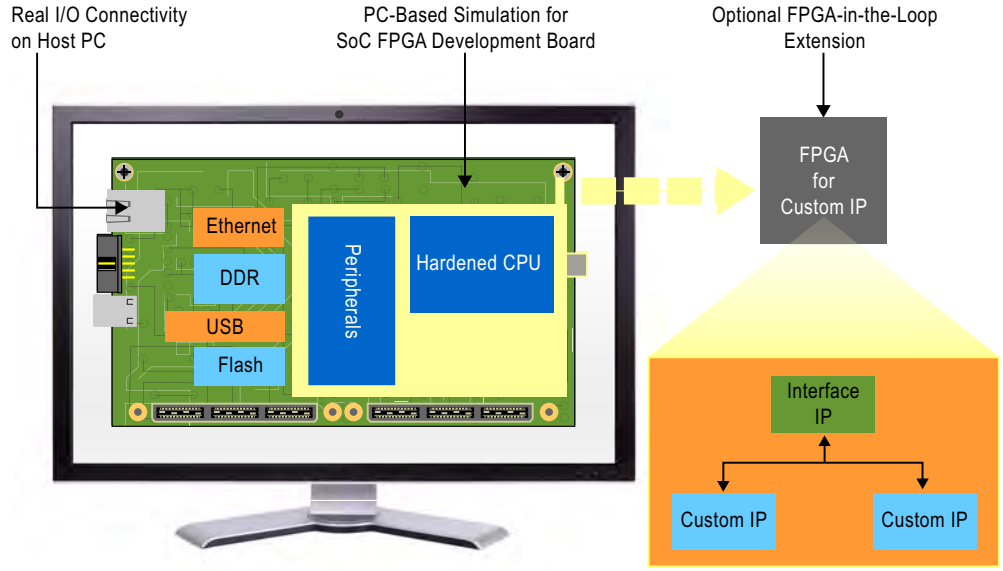


Virtual Target

Users of Arria V system-on-chip (SoC) devices benefit from a development option unique in the FPGA industry. Software developers can use the SoC FPGA Virtual Target, a PC-based functional simulation of an Altera SoC FPGA development board. The Virtual Target is a binary- and register-compatible functional equivalent of an SoC FPGA development board, that enables embedded software engineers to develop using familiar tools and maximize legacy code reuse, then move their application to the SoC FPGA with minimal effort.

The Virtual Target offers ecosystem tools compatibility and additional debugging capabilities unique to a simulation environment. As a simulation model, the Virtual Target offers more visibility into the system under debug, allows users greater control of the application execution (especially in a multicore system), and performs many debugging tasks that are hard or impossible on hardware. These features and capabilities enable significant productivity gains during embedded software development, which is often the longest and most resource-intensive part of embedded systems projects. Figure 4 shows the Virtual Target with the optional FPGA-in-the-loop extension that allows embedded developers to test their software with Altera FPGA hardware such as custom peripherals and hardware accelerators.l

Figure 4. Altera Virtual Target for SoC FPGAs



Lower Manufacturing Costs

Arria V devices reduce manufacturing costs in a number of ways, including hard IP, fractional phase-locked loops (FPLLs), voltage rails, core fabric, and new packaging, all of which mainly stem from the highest level of integration offered in a midrange FPGA.

Hard IP

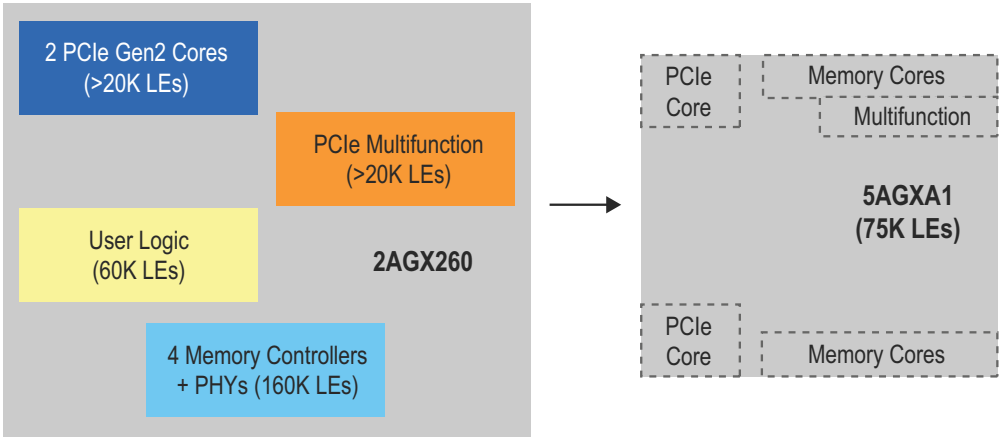
Arria V FPGAs include the most hard IP in a midrange FPGA. The hard IP in Arria V FPGAs was selected to ease the implementation of the most commonly used functions in midrange FPGA applications, maximizing the usefulness of the silicon area they occupy. Using hard IP for these functions reduces their cost of implementation and their power consumption. Table 1 lists the hard IP functions in Arria V devices, and shows the amount of device resources that are saved via a hard implementation versus implementation in FPGA fabric resources.

Table 1. Hard IP Functions in Arria V FPGAs

Hard IP Block	FPGA Resources Saved per Block
32-bit DDR3/DDR2 memory controller with ECC, command/data reordering, and multiport front end	>40K LEs and 45 M10K blocks
PCIe Gen1 and Gen2	>10K LEs
PCIe Multifunction	>20K LEs
ARM® Cortex™-A9 MPCore™ processor and peripherals	>40K LEs

Figure 5 shows an example FPGA design that uses four memory controllers, two PCI Express (PCIe) blocks with multifunctions, and 60K LEs of user logic. The left side of Figure 5 shows that an Arria II device with 260K LEs of user logic capacity (the EP2AGX260) is needed to accommodate all of these functions if they were implemented in the FPGA fabric in "soft" logic. The right side of Figure 5 shows the same design implemented in an Arria V FPGA (5AGXA1) with lower user logic capacity (75K LEs), demonstrating how the hard IP-based architecture of Arria V can reduce overall implementation cost.

Figure 5. Hard IP Blocks Reduce FPGA User Logic Requirements and Lower Implementation Costs



Note: Hard IP block sizes not to scale

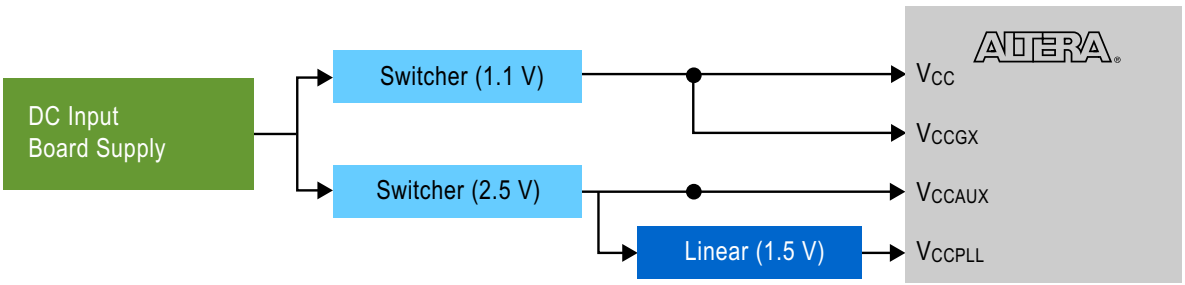
FPLLs

FPLLs enable Arria V devices to synthesize a wide range of frequencies with high precision. FPLLs accomplish this by leveraging 32-bit M and N values in their feedback path, as well as a δ-σ modulator. With this capability, FPLLs can potentially replace voltage-controlled oscillators (VCXOs) on the board, reducing both board costs and board space.

Voltage Rails

As shown in Figure 6, Arria V devices require the fewest number of voltage rails of any midrange FPGA, as few as three in the simplest configuration. Additional voltage rails are required to support I/O standards that are different voltages from than the ones shown in the diagram, as is standard with other FPGAs. These minimal voltage rail requirements can reduce voltage regulator requirements, as well as simplify board design and reduce board layers.

Figure 6. Arria V FPGAs Require the Fewest Number Power Rails of Any Midrange FPGA



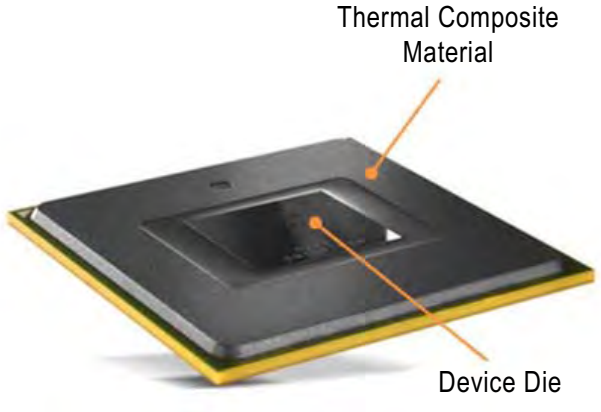
Core Fabric

Arria V FPGAs utilize an innovative core fabric to efficiently implement both logic and digital signal processing (DSP) functions. The basic building block of the Arria V is the adaptive logic module (ALM). In this generation of Altera devices, the ALM has two more registers than to the prior generation, increasing the register-to-logic ratio and providing a better fit for the register-rich designs that are common to higher density FPGAs. In addition, Arria V FPGAs feature a new embedded memory block, the M10K. This memory block is smaller than embedded memory blocks in competing architectures, resulting in higher granularity, more memory ports, and fewer wasted blocks overall. Finally, Arria V FPGAs have variable-precision DSP blocks that can implement multipliers of varying precision. This capability enables Arria V FPGAs to deliver the precision multiplier required by the customer's application, rather than imposing a single predetermined precision upon all users.

New Packaging

Another way in which Arria V devices reduce manufacturing costs is with their innovative new packaging. Arria V devices are the first FPGAs to be offered in thermal composite flip chip ball-grid array (BGA) packaging. Thermal composite packages, shown in Figure 7, provide several cost-saving features compared to the lidless flip chip packages used with other midrange FPGAs.

Figure 7. Thermal-Composite Flip Chip Packaging



First, thermal composite packages are designed to use the same familiar handling and heat-sink procedures as metal-lidded packages. The thermal composite material provides a large surface area for ease of adhesion and greater thermal dissipation than lidless packages. A designer can mount heat sinks easily to the top of thermal composite packages in the same way as with metal-lidded packages, without costly handling procedures and PCB attachments. Finally, thermal composite packages are also lower profile than lidded packages, enabling their use in more space-constrained environments.

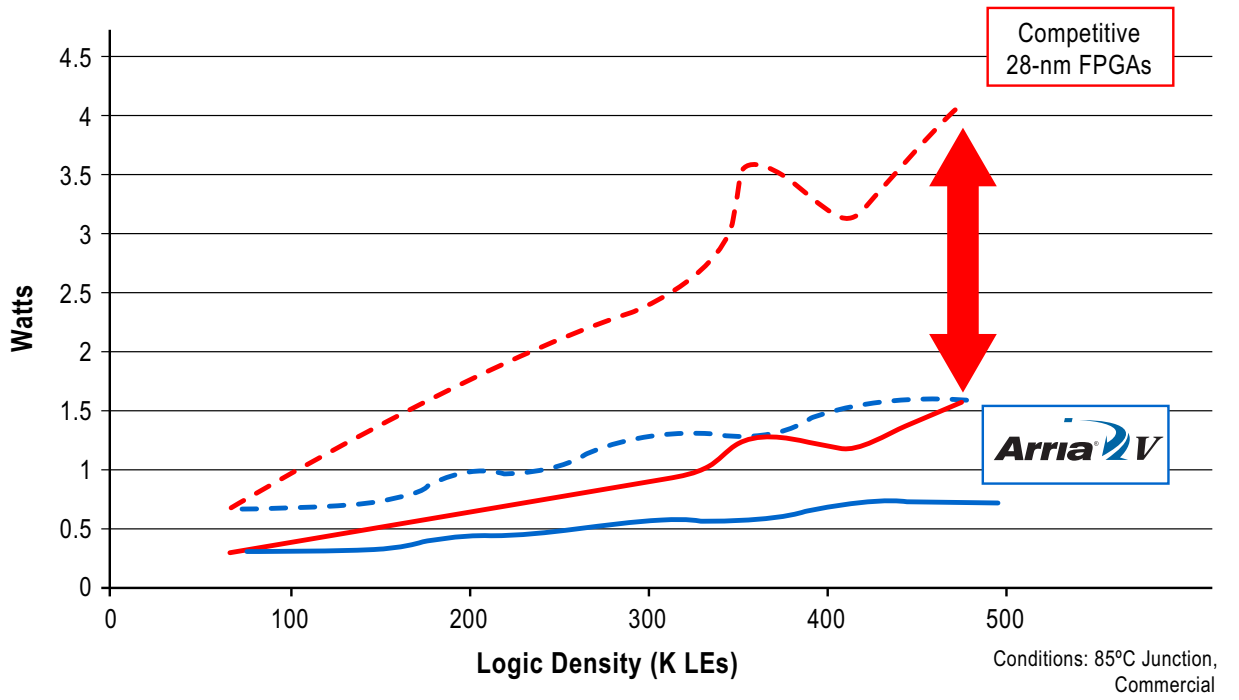
Keep Operation and Maintenance Costs to a Minimum

Arria V FPGAs keep operation and maintenance costs to a minimum via two main aspects: low power consumption and in-field reconfiguration.

Low Power Consumption

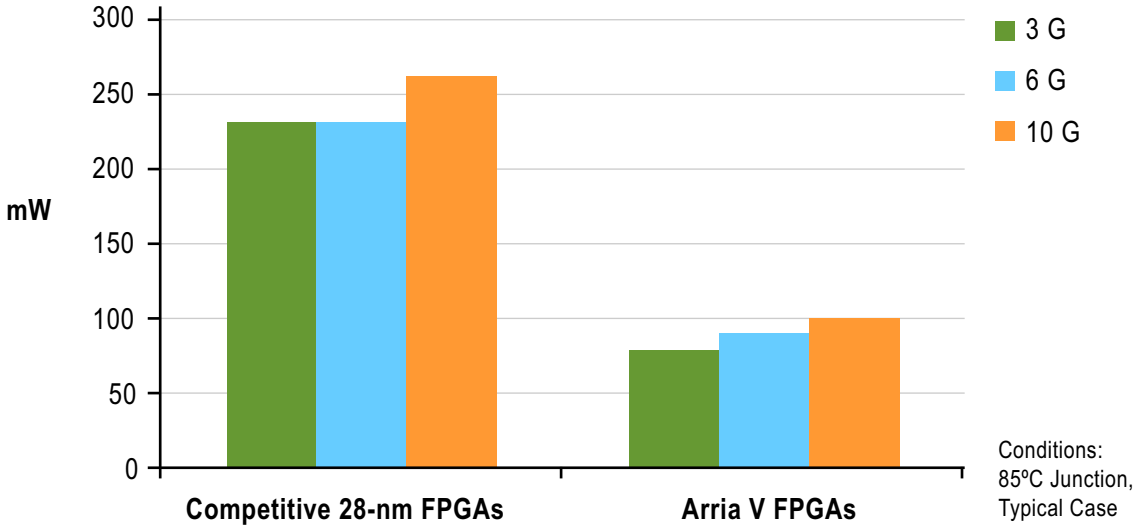
Arria V FPGAs are the lowest power-consuming midrange FPGAs, with the lowest static power and transceiver power. Power consumption is increasingly a key decision criterion for today's electronic products and systems, and low power consumption is an attractive way to keep operational costs to a minimum. Figure 8 shows the static power consumption of Arria V FPGAs (blue lines) compared to the power consumption of competing 28-nm midrange FPGAs (red lines). The solid lines show the typical static power consumption of commercial-temperature devices under typical conditions at 85°C, while the dotted lines show the worst-case static power consumption of commercial-temperature devices at 85°C. As the graph shows, Arria V devices consume significantly lower static power, up to 60% less power than competing devices.

Figure 8. Static Power Consumption of Arria V FPGAs Compared to Other 28-nm Midrange FPGAs



Arria V devices also consume the lowest amount of transceiver power of any midrange FPGA. Altera's extensive transceiver design expertise is unmatched in the industry, and this unique advantage is reflected in the low dynamic power consumption of its transceivers. For example, at 6 Gbps, Arria V transceivers consume less than 100 mW of power, significantly lower than transceivers in competing 28-nm midrange FPGAs, as shown in Figure 9. For designs that utilize the up to 36 transceivers available in Arria V devices, the power savings is over 5 W.

Figure 9. Power-Per-Channel of Arria V FPGAs Compared to Other 28-nm Midrange FPGAs



Arria V SoC FPGAs offer software-controlled power-down modes, enabling them to operate while the FPGA fabric is powered down. Other modes enable the processor to run in single-core (versus dual-core) operation, or at slower clock speeds. With these and other low-power features in place, Arria V devices consume the least amount of power for midrange applications, as demonstrated by recently published power benchmarks.

In-Field Reconfiguration

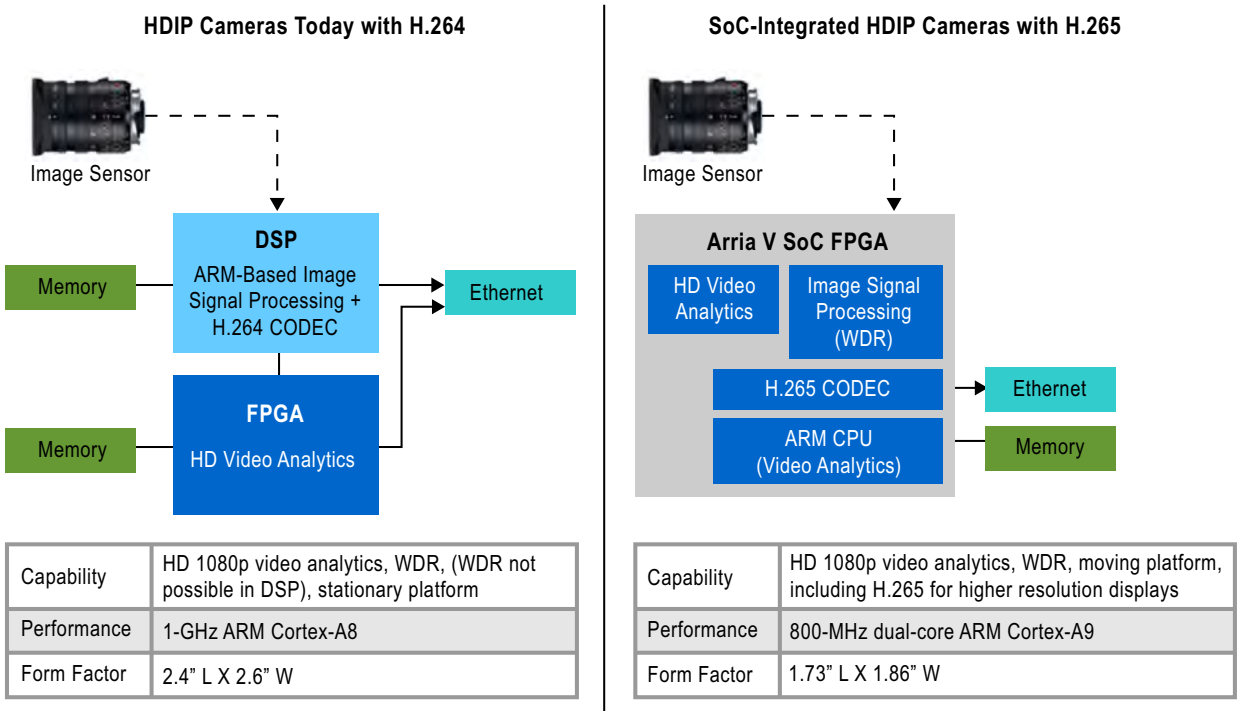
Another way in which Arria V devices lower maintenance costs is with remote upgrade capability. With this capability, product developers can upgrade their products in the field without resorting to costly "forklift" upgrades, and without requiring maintenance personnel to perform the upgrades locally or manually. Entirely new functionality can be delivered in the field using this feature, which enables product developers to use a platform-based approach to offer multiple products of various capabilities based on a single hardware platform. Altera FPGAs provide a unique feature to facilitate this process: Configuration via Protocol (CvP), which enables configuration of the FPGA over an industry-standard protocol. The first CvP protocol to be supported is PCIe. Using CvP, developers can take control of the FPGA configuration process using a host processor connected to the PCIe bus, and source the configuration information anywhere in their system. In this way, the memory costs of storing the FPGA configuration file can be also reduced, since they can be combined with the host processor's stored instructions and data.

Integration Example

The application example of an high-definition (HD) IP camera with H.265 encoding illustrates how an application can take advantage of some of the Arria V FPGA's features to achieve the highest level of system integration and corresponding integration cost benefits. The block diagram on the left side of Figure 10 shows a current implementation of an HD IP camera using a digital signal processor to perform image and signal processing, as well as the H.264 video encoding. This

design also includes an FPGA to perform custom HD video analytics. The right side of Figure 10 shows an implementation based on an Arria SoC FPGA, which combines the image and signal processing, an H.265 video coder/decoder (CODEC), wide dynamic range (WDR) processing, and custom HD video analytics into a single device.

Figure 10. HD IP Camera Developmental Evolution



Capability	HD 1080p video analytics, WDR, (WDR not possible in DSP), stationary platform
Performance	1-GHz ARM Cortex-A8
Form Factor	2.4" L X 2.6" W

Capability	HD 1080p video analytics, WDR, moving platform, including H.265 for higher resolution displays
Performance	800-MHz dual-core ARM Cortex-A9
Form Factor	1.73" L X 1.86" W

Table 2 shows a breakdown of the FPGA device resources utilized by this design in the top rows, and for comparison shows the device resources available in an Arria V 5ASXB3 SoC FPGA in the last row.

Table 2. FPGA Design Resources Used in the Example

Design Module	Logic Resource Requirement (LEs)	Memory Resource Requirement (M10K)	DSP Resource Requirement (18x18 multipliers)
HD Video Analytics	74K	295	38
Wide Dynamic Range Signal Processing	95K	335	180
H.265 CODEC(1)	40K	250	200
Total	**209K**	**880**	**481**
Devices Resources in Arria V 5ASXB3	**350K**	**1,729**	**1,618**

(1) Estimated

This level of integration is only possible using an Arria V SoC FPGA, resulting in a smaller form factor, lower power consumption, and fewer support components—all of which contribute to lower overall product cost, as well as lower cost of operation. In addition, all of the image processing or video analytic algorithms can be updated dynamically and remotely while the product is deployed in the field, resulting in lower maintenance costs and longer product lifetimes.

Conclusion

This paper discusses just some of the ways in which Arria V FPGAs are uniquely qualified to reduce overall product development costs from several different perspectives, including design and debug, manufacturing, and operation/maintenance. Altera has invested in lowering the total system cost for designs by integrating features that decrease the need for support components such as oscillators, capacitors and power regulators. Design costs are reduced due to higher integration and increased hard IP with the memory controllers, PCIe blocks, and embedded processors. Finally, by offering a drastic 40% reduction in total power consumption, Arria V FPGAs save significant operating costs, making the devices a cost-effective solution not only at the time of design, but for the lifetime of the product.

Further Resources

- Board Design Resource Center, including the PDN Design Tool: www.altera.com/technology/signal/board-design-guidelines/sgl-bdg-index.html
- Arria V Family Pin Connection Guidelines: www.altera.com/literature/dp/arria-v/PCG-01013.pdf
- Using Virtual Target with the ARM Cortex-A9 MPCore Processor: www.altera.com/devices/processor/arm/cortex-a9/virtual-target/proc-a9-virtual-target.html
- Arria V Device Handbook: www.altera.com/literature/hb/arria-v/arriav_handbook.pdf
- Arria V Early Power Estimator: www.altera.com/support/devices/estimator/arria-ii-gx-estimator/aiigx-power-estimator.html
- Arria V Power Benchmarks: www.alterawiki.com/wiki/Arria_V_Power
- Video: "Arria V FPGA Sneak Peek: Transceiver Operation at 6.375 Gbps and 10.3125 Gbps": www.altera.com/b/arria-v-fpga.html
- Webcast: "Achieving 1066-MHz DDR3 Performance With Advanced Silicon and Memory IP": www.altera.com/education/webcasts/all/wc-2010-1066mhz-ddr3-silicon-memory-ip.html
- White Paper: *Using External Memory Interfaces to Achieve Efficient High-Speed Memory Solutions*: www.altera.com/literature/wp/wp-01169-high-speed-memory.pdf

Acknowledgements

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Document Revision History

Table 3 shows the revision history for this document.

Table 3. Document Revision History

Date	Version	Changes
November 2011	1.0	Initial release.