Optimize Power and Cost with Altera's Diversified 28-nm Device Portfolio

This white paper describes the power and cost advantages of Altera's diversified 28-nm FPGA portfolio that is tailored for a wide range of applications. This portfolio includes the Stratix® V, Cyclone® V, Arria® V, and HardCopy® V devices.

Introduction

Altera's 28-nm devices provide a diversified product portfolio tailored to support a broad spectrum of applications, ranging from low cost and power, to high-end applications. This diversification extends beyond simple size and density options, offering developers devices with the right combination of price, performance, functionality, and power consumption required by their designs. FPGAs are the technology of choice for many development teams, and Altera continually evolves FPGA technology to reduce cost and power, while increasing performance. Altera's versatile FPGAs are supplanting ASIC and ASSP approaches as a major component in system designs, and as a multi-function adjunct to the system CPU.

Today's system application designers face increasing requirements for higher integration and performance, along with lower power and cost. Simply designing FPGAs to the next incremental progression may satisfy mid-range application needs, but would compromise performance at the high end and cost at the low end. To meet the needs of the widest application range, the FPGA must take greater incremental leaps. To meet the widest application requirements, Altera's 28-nm portfolio leverages significant advancements in the following areas:

- Process Technology
- Transceiver Design
- Product Architecture
- System IP

Leaping Beyond Incremental Progression

Altera has taken an evolutionary leap by creating a diversified portfolio of product options at the 28-nm process node. The 28-nm process brings inherent improvements to Altera's FPGA performance.

Greater circuit density reduces the cost for each functionality, while smaller transistors reduce power. But unlike competitors "one type fits all" process technology, Altera offers two distinct 28-nm process options. Altera's 28-nm high-performance (HP) process optimizes for performance, while the low-power (LP) process minimizes power for a given functionality or application.

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September 2012   Altera Corporation

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Altera's 28-nm HP process is for designs requiring the fastest possible logic speeds. High-K metal gates produce logic blocks and DSP functions that are as much as 35% faster than other process options. High-performance transistors use a strained-silicon structure in which a cap covers the channel that induces mechanical strain in the silicon lattice, as shown in Figure 1. This architectural feature increases carrier mobility and thus switching speed, without increasing leakage current. This results in delivery of 28-Gbps transceivers that operate at 200-mW total power, the highest performance at the lowest power available.

Figure 1. Transistor Cap Reduces Current Leakage and Power
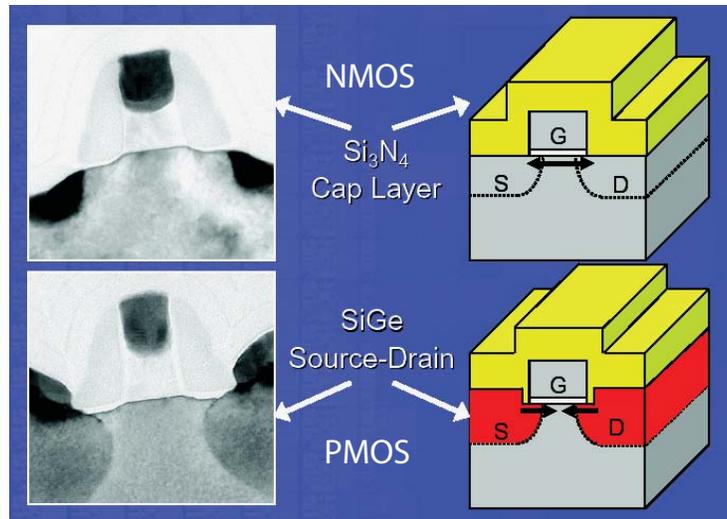
Conversely, the LP process targets applications that require minimal device power consumption. The LP process provides minimum leakage and reduced dynamic current through the use of longer gate channels and other techniques. The LP process also uses more conventional metallization than the HP process to further minimize cost and power. As a result, the LP process achieves 50% lower power than the previous process node.

Tailored Transceivers Provide Performance Options

Altera's versatile approach also provides performance options to tailor the serial transceivers. If an application such as I/O expansion requires only 5-Gbps transceivers, the design does not require the power and cost of larger transistors required for operation at 28 Gbps. Rather, the design requires a transceiver that simply meets performance requirements at the lowest power and cost.

Altera's 28-nm portfolio introduces a modular transceiver that enables designers to match device performance with the application. This transceiver design uses the same base architecture to produce multiple variants targeting from 3-, 6-, 10-, 14.1-, and 28-Gbps operation. Further, the transceivers allow dynamic selection from among several speed settings within their ranges, drawing less power with reduced speed. This selectability provides a method to reduce average system power consumption by operating transceivers at minimal speed when idle, ramping to higher speed only as needed for time-critical data transfers.

These transceivers support a wide variety of protocols, including 3G SDI, 1-, 10-, and 100-Gigabit Ethernet, Fibre Channel, Infiniband®, Interlaken®, PCI Express® (PCIe®), SATA, Serial RapidIO®, and SONET.

For more details about Altera's 28-nm transceiver technology, refer to the *Extending Transceiver Leadership at 28nm* white paper.

Versatile Architecture Reduces Cost and Power

Altera incorporates a number of architectural enhancements into its 28-nm devices to increase versatility and reduce power. These enhancements include support for smart power options, dynamic reconfiguration, variable-precision DSP, and support for various memory protocols and I/O standards.

Take Control of Power

Smart power features can reduce average device power consumption by controlling FPGA operation in specific blocks. To completely eliminate power consumption in inactive logic blocks, designers can use multiple power planes to 'turn off' individual logic blocks when not needed. When circuits must remain powered even when idle, the available block-oriented clock gating can help reduce dynamic power consumption. The power controller can use the gating to slow or stop the clock to specific blocks when their function does not need high performance or can be suspended.

For more information, refer to *Reducing Power Consumption and Increasing Bandwidth on 28-nm FPGAs*.

Minimize Downtime with Dynamic and Partial Reconfiguration

The partial and dynamic reconfiguration capability in Altera's 28-nm FPGAs increases versatility while reducing cost. Unlike previous FPGAs which must be fully configured before running, Altera's 28-nm devices allow in-circuit reconfiguration of some FPGA blocks, while others continue operating normally. Such reconfiguration permits an FPGA's functionality to change in response to system needs without stopping system operation. Rather than requiring a large FPGA to store all functions and then switch among them, designers can target a smaller FPGA and load functions as needed.

For more information, refer to *Increasing Design Functionality with Partial and Dynamic Reconfiguration in 28-nm FPGAs*.

Leverage Variable-Precision DSP

Altera's innovative DSP design allows designers to independently configure the precision of each DSP block in a device—ranging from 9x9 to 27x27 bits—to implement required higher packing or precision. For example, simple video processing may require only 9-bit precision, while a high-end color system may require 24 bits. In the case of 9-bit video, a single block can fracture to support three, 9-bit multipliers, tripling the DSP block efficiency. A single variable-precision block can efficiently address this full range, thus allowing designers to adapt FPGA resources to their algorithms rather than adapting the algorithm to fixed resources.

Variable-precision DSP also supports bit growth of FIR filters and FFTs in the design, by allowing successive stages to increase precision as needed, thereby maximizing resource utilization. Altera's DSP blocks provide the industry's only 64-bit cascade bus and adder for combining individual blocks to achieve even higher precision.

For more information about Altera's variable-precision DSP, refer to the *Accelerating DSP Designs with the Total 28-nm DSP Portfolio* white paper.

Altera's 28-nm portfolio supports three different types of on-chip memory for various applications. For example, the M20K memory block is optimized for high-performance operation and high bit density required by 100G and packet processing applications that require large memories with high, raw bandwidth. The M10K block has a lower bit density but offers more ports per silicon area, making it suitable for DSP-intensive applications such as motor control, studio equipment, and 3D TV that would not fully utilize an M20K block. Most applications also require small buffers which would waste 90% of the M10K block's capacity. For efficient and low-cost handling of shallow buffers and delay elements, Altera offers the 640-bit MLAB block.

Interface with Application-Specific I/O

Altera's high-performance I/O blocks for memory interfaces and LVDS signaling are ideal for high-end wireless, radar, and 100G systems. However, this high performance I/O is unnecessary for mid-range applications, such as remote radio units and broadcast equipment. Instead, designers can use Altera's various I/O architectures tailored for distinct application classes. The high-end I/O supports 1066-MHz DDR3 DIMM memory and 1.4-Gbps LVDS, for applications such as 100GbE switches. The mid-range I/O block handles 533-MHz DDR3 memory and 1.25 Gbps. The low-cost I/O block is well suited for 400-MHz DDR3 and offers 3.3V-I/O with 16-mA drive for industrial applications.

Hard IP Increases Efficiency

Hard IP implementations first appeared in Altera's 40-nm devices as PHY layer elements that eliminate the need for external devices in high-performance serial I/O. In Altera 28-nm devices, Embedded HardCopy blocks provide a measure of ASIC cost, performance, and power characteristics without compromising design flexibility, as shown in Figure 2.

Figure 2. Customizable Embedded HardCopy Block
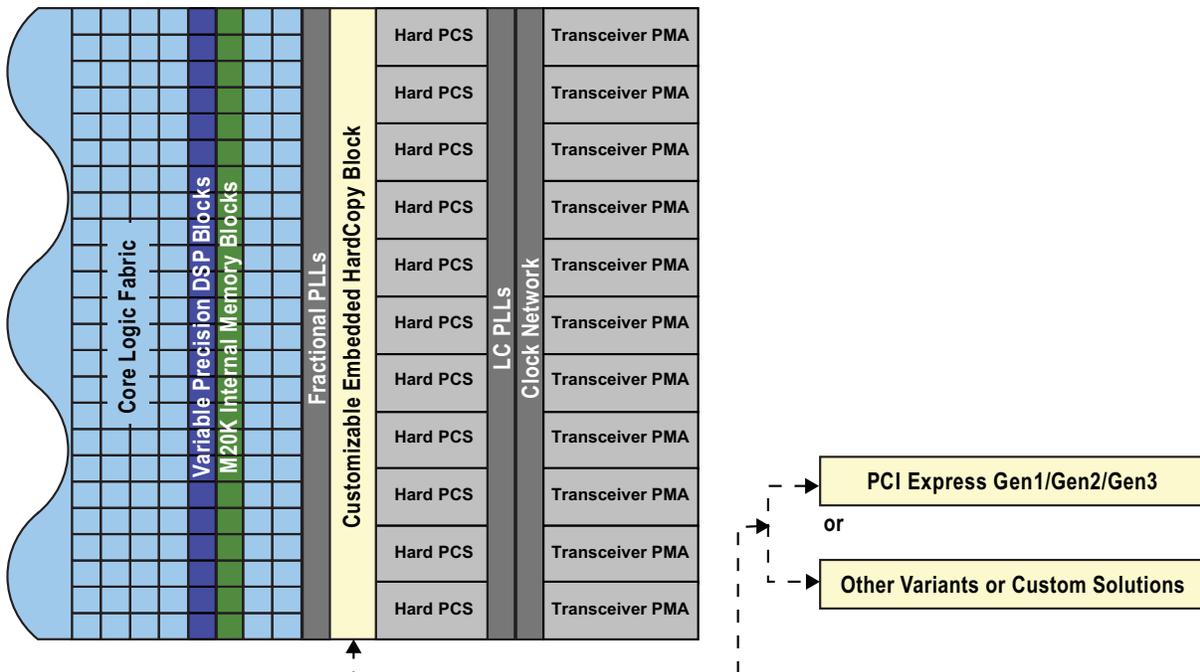
Incorporating HardCopy blocks in the FPGA frees the device's programmable resources for custom circuits while reducing cost. For example, a PCIe protocol stack requires 150 K logic elements as a soft implementation, but requires as little as one-third the die area in HardCopy blocks. The hard IP also improves performance. Compared to soft implementations in the device's LEs, hard IP for the same functionality uses up to 65% less power while offering up to 50% higher performance.

The HardCopy blocks include support for common functions—such as memory controllers, PCIe stacks, and Ethernet interfaces—to address the broadest range of application requirements. Furthermore, these blocks support a degree of configurability. For example, designers can configure a PCIe HardCopy block for Gen1 or Gen2, and an Ethernet block for 40G or 100G operation, as required.

Altera can also use Embedded HardCopy blocks to rapidly implement emerging, application-targeted device variants. The ability to expand support in current-generation devices reduces the need for device migration, thus reducing designer's time-to-market.

Chose Application-Tailored Solutions

To provide the most versatility, Altera's 28-nm portfolio includes devices with various combinations of process, architecture, transceiver, and system IP features. Within each family are variations for different transceiver speed grades and hard IP block resources that allow designers to target devices that closely match their application requirements. The following sections describe these combinations of features.

Cyclone V Lowest Cost and Power

Many applications have only modest performance requirements but face severe cost, power (typically less than 5 W), and space constraints. For example, handheld projectors must draw the lowest possible power to maximize battery life. Motor controllers, displays, and software-defined radios have both power and space constraints. Each application also has other specific requirements. For example, devices such as a WDR surveillance cameras require low data-rate transceivers to send signals off-unit, while night vision goggles require internal video processing and buffering.

Altera's Cyclone V family—the lowest cost and power option available in Altera's 28-nm portfolio—targets such applications. Cyclone V devices are built on the LP process and save cost by using wire bond packaging. The Cyclone V family includes the following variants:

■ Cyclone V GX FPGAs—These devices offer 3-Gbps transceivers, a hard IP PCIe Gen1 x4 interface, M10K and MLAB memory blocks, and variable-precision DSP. A hard IP external memory controller supports low-cost, low-power memories such as mobile DDR, LPDDR2, and 400-MHz DDR3.

■ Cyclone V GT FPGAs—These devices offer the same features as Cyclone V GX, with the addition of 5-Gbps transceivers and two PCIe Gen2 x1 hard IP blocks.

■ Cyclone V E FPGAs—These devices do not include hard IP blocks, but are composed solely of LEs for maximum design flexibility.

Arria V Balanced Performance, Power, and Cost

For mid-range applications, the ability to balance performance, power, and cost is critical. Devices such as remote radio units, broadcast video cameras, 10G/40G line cards, and video switchers need higher performance than those targeting low-cost devices, with 10-Gbps transceiver requirements common. Nevertheless, such devices must remain as inexpensive as possible, while using less than 10 W of power. Common functions for this application space include video processing and buffering, FIR filters, and higher-performance external memory.

Altera's Arria V family offers the balanced performance, power, and cost required by mid-range applications. Arria V devices use the LP process technology to minimize power. These devices include M10K/MLAB memory blocks, while offering faster transceivers to handle more demanding performance requirements. Arria V devices also use flip-chip packaging to maximize off-chip signaling speeds. The Arria V family offers the following variants:

- Arria V GX FPGAs—These devices include 6.5536-Gbps transceivers, a hard IP PCIe Gen 2x4 interface with multi-function support, variable-precision DSPs optimized for FIR filter applications, and a hard IP memory controller that supports DDR3 SDRAM at 533 MHz.

- Arria V GT FPGAs—These devices offer 10-Gbps transceivers for applications requiring slightly more speed. Logic capacities range from 75,000 to 500,000 LEs.

Stratix V Highest Performance and Bandwidth

Once considered outside the reach of FPGAs, high-performance applications such as 40/100GbE switches, military radar, and advanced LTE base stations are among the most demanding. These systems require transceivers that operate at the highest possible performance for backplane and chip-to-chip communications and dense, high-speed external and internal memory. These applications often call for high-precision DSP, along with logic in excess of 350-MHz clock speed. While power may not be the primary concern in these applications, reduced power carries significant benefits in terms of lower system cooling costs and greater system reliability.

Altera's Stratix V devices meet the demands of these high-end applications—offering the highest performance at the lowest power in their class. Stratix V devices use the HP process technology to offer transceiver speeds up to 28 Gbps, requiring only 200 mW. A soft memory controller configurable for a wide range of memory types (including DDR3, RLDRAM II, and QDRII+) up to 72-bits wide handles speeds up to 1066 MHz.

Available in logic capacities up to 952 K LEs, the Stratix V family offers the following variants:

- Stratix V GX FPGAs—These devices incorporate 14.1-Gbps transceivers that support serial backplane and optical communications and include hard IP PCIe Gen 3 x8 and 40/100G Ethernet IP options.

- Stratix V GT FPGAs—These devices are similar to Stratix V GX FPGAs, but also offer 28.05-Gbps transceivers for highest performance applications. The GT series includes 14.1-Gbps transceivers, but also incorporates variable-precision DSP blocks for up to 54x54 operation.

- Stratix V E FPGAs—These devices offer only LEs to provide the highest capacity of configurable logic available. All Stratix V devices include M20K memory blocks for the highest performance and density.

Quick HardCopy Path to ASICs

In addition to the three FPGA families, Altera offers the 28-nm HardCopy V ASIC family that provides a low-risk, low-power, and low-cost path for taking FPGA designs to volume production. The resulting ASIC uses the same process technology and has the same hard IP blocks as the FPGA, including transceivers, thus reducing performance differences in migration. The HardCopy ASIC is package- and pin-compatible with the original Stratix V design, and offers the same signal integrity. The use of HardCopy V ASICs enables developers to deliver products significantly earlier than other ASIC methodologies.

Conclusion

Altera's versatile 28-nm device portfolio precisely matches designer's requirements, while minimizing cost and power. In addition, Altera offers an integrated set of design tools that help empower all device features. Altera's Quartus® II design software includes system integration and power analysis tools to help achieve the right balance of performance and cost. Altera offers a variety of IP cores for quick and easy implementation of standard functions. Designers can use the Quartus II software to rapidly migrate to a HardCopy V ASIC implementation.

Altera's 28-nm device portfolio represents a significant leap forward, making FPGAs the ideal solution in an ever-widening application range. By embracing process, architectural, and IP diversity, Altera provides an integrated set of FPGA options that accurately match the various cost, performance, and power requirements. This offering provides an unprecedented array of application developers with a rapid, low-risk approach to designing and producing next-generation products.

Further Information

- White paper: *Accelerating DSP Designs with the Total 28-nm DSP Portfolio*
  www.altera.com/literature/wp/wp-01136-stxv-dsp-portfolio.pdf

- White paper: *Extending Transceiver Leadership at 28 nm*
  www.altera.com/literature/wp/wp-01130-stxv-transceiver.pdf

- White paper: *Increasing Design Functionality with Partial and Dynamic Reconfiguration in 28-nm FPGAs*
  www.altera.com/literature/wp/wp-01137-stxv-dynamic-partial-reconfig.pdf

- White paper: *Reducing Power Consumption and Increasing Bandwidth on 28-nm FPGAs*
  www.altera.com/literature/wp/wp-01148-stxv-power-consumption.pdf

Acknowledgements

- Juwayriyah Hussain, Sr. Product Marketing Engineer, Altera Corporation

- James Adams, Corporate Marketing, Altera Corporation

- Umar Mughal, Product Marketing Manager, Altera Corporation

Document Revision History

Table 1 lists the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
September 2012	1.2	■ Updated Arria V FPGA transceiver speed to 6.5536 Gbps and Stratix V GT FPGA transceiver speed to 28.05 Gbps. ■ Updated Stratix V FPGA logic capacity to 952 K.
June 2012	1.1	Minor text edits.
May 2011	1.0	Initial release.