

This document describes the advantages of modern switching voltage regulators in a power distribution network (PDN) design to achieve the best FPGA transceiver performance. This white paper provides guidance on voltage regulator selection for low-noise applications, and a test case that demonstrates the transceiver performance for different types of voltage regulators and voltage rail configurations.

## Introduction

PDN designs targeting transceiver (SERDES) FPGAs require clean voltage sources with strict voltage rail requirements. Although Low Drop Out (LDO) linear voltage regulators are typically used in low-power applications, this method often requires careful isolation of voltage rails. Board designers must consider the trade-offs between voltage rail isolation and voltage rail sharing in these applications. Too much isolation increases the voltage regulator count, while too much sharing may affect performance. If the PDN is inadequately regulated, the performance of the transceiver could be at risk. Therefore, the correct selection of voltage regulators and voltage rail configuration is important to achieve the best transceiver performance.

Innovations in switching voltage regulators now provide significant advantages over linear regulators in many PDN designs. In addition, advances in FPGA transceiver technology eliminate the need for some external regulators by placing them inside the FPGA. This document provides guidance on the following aspects of voltage regulator selection and implementation:

- [Linear vs. Switching Voltage Regulators](#)
- [FPGA Voltage Rail Isolation Guidelines](#)
- [Recommended Single Package Solutions](#)
- [PDN Performance Examples](#)

## Linear vs. Switching Voltage Regulators

Traditionally, board designers use a linear regulator for low current, low noise, with limited board space, and use a switching regulator for high power and efficiency. While this guideline may still apply in some cases, advancement in switching regulator design now enables replacement of linear regulators in many applications. This section describes the differences between linear and switching regulators, provides examples of each type, and introduces the advancements in switching regulators.

Linear regulators provide low output noise, are easy to implement, require few support components, have faster response to load variations, and are lower cost than switching regulators. However, as power requirements increase, a linear regulator cannot provide an efficient high-current output. Typical switching regulators provide efficient, high-current output, but often require multiple support components and incur a noise penalty. Recent advances in switching regulator design now allow the switching regulator to occupy the space once held by linear regulators. The next section provides more detail about the options available with this new technology.

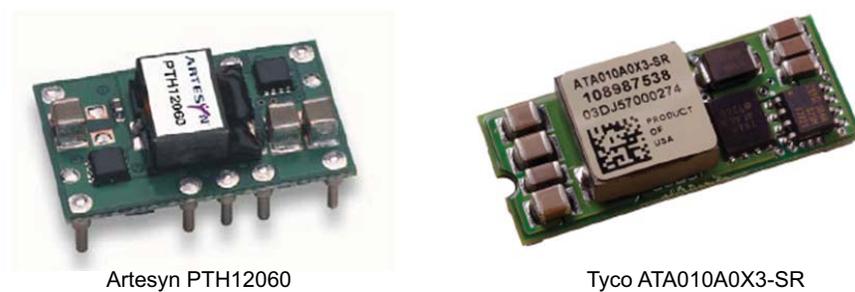
## Advances in Switching Regulator Design

There have been several important transformations in switching regulators in the past ten years. These transformations began with DC/DC-converter IC, external power FETs, and Inductors with many external support components. The next transition consisted of a mini switching circuit on a mini circuit board with a standard interface to a PCB. In further advancements, a DC/DC converter is integrated with the MOSFETS in a single package (monolithic switcher), with the inductor remaining outside the package. The most recent advancement consists of a single package solution. The next section provides more details about these advancements.

### Mini Circuit on Mini PCB Solutions

The mini circuit on a mini PCB has two standards associated with DC/DC converter modules; the Point of Load Alliance (POLA) and the Distributed-Power Open Standards Alliance (DOSA). Each standard defines a pin-out interface, a standard package size, and standard electrical specifications and controls. Examples of these technologies are the Artesyn™ Technologies PTH12060 DC/DC Converter (POLA standard), and Tyco Electronics ATA010A0X3-SR Power Module (DOSA standard). Each require minimal external support components and have a footprint area of ~1.1X0.7 inches. These modules help reduced the overall footprint and optimized the parasitics associated with the switching regulator circuit, as illustrated in [Figure 1](#).

**Figure 1. Power Modules, POLA, and DOSA Standards**



## Single Package Solutions

Some vendors now offer a switching regulator that integrates all of the power supply components in a single package, such as the Linear Technology  $\mu$ Module™ family, the Intersil Power Module family, and the National Semiconductor Simple Switcher Power Module family, as illustrated in [Figure 2](#).

**Figure 2. Single Package Solutions**



For example Linear Technology's  $\mu$ Module takes all components associated with the switching regulator circuit and encapsulates them on a substrate. The major blocks such as the DC/DC converter, MOSFETs, and Inductor reside on their own substrate and are interconnected. This technology further reduces the footprint and improves the optimization compared to the POLA and DOSA Modules. [Table 1](#) compares the footprint area of each package.

**Table 1. Package Footprint Comparison**

Vendor	Package Footprint
Linear Technology	6.25mm x 6.25mm up to a 15mm x 15mm package
Intersil	15mm x 15mm package
National Semiconductor	6.5mm x 6.4mm up to 13.77mm x 10.16mm package

## FPGA Voltage Rail Isolation Guidelines

Typical FPGA devices consist of many voltage rails, and even more voltage rails are required to power the noise sensitive SERDES transceivers. For example, [Table 2](#) shows the recommended voltage rail isolation for an Altera Stratix IV GX FPGA device with transceivers. Despite the high number of voltage rails in this FPGA, some of the rails may share the same regulator, depending on the design. However, certain voltage rails may require isolation because of noise and performance concerns. Designers must closely follow the manufacturer's recommendations for power requirements. There are noise sensitive circuits that may require a low noise power source. Failure to provide a clean power source in a critical area may affect the performance in terms of jitter generation and PLL functionality.

**Table 2. Example Voltage Rail Isolation in Stratix IV GX FPGA**

FPGA Voltages			
Voltage Value	Voltage Name	Description	Share/Isolate
0.9V	VCC VCCD_PLL	FPGA core power PLL digital power	Share Share / Isolate
1.2V–3.0V	VCCIO	I/O supply voltage, banks 1-8	Share

**Table 2. Example Voltage Rail Isolation in Stratix IV GX FPGA**

<b>FPGA Voltages</b>			
<b>Voltage Value</b>	<b>Voltage Name</b>	<b>Description</b>	<b>Share/Isolate</b>
¾ VCCIO	VREF	Input reference voltage banks 1-8	Share
1.5V	VCCPT	Programmable power technology	Share / Isolate
1.8V/2.5V/3.0V	VCCPGM	Configuration pin power	Share
2.5V	VCCCLKIN VCCA_PLL VCCAUX VCCABAT	Differential clock input power PLL analog power Auxiliary power Battery backup	VCCCLKIN - Share VCCA_PLL - Isolate, Bead VCCAUX - Share / Isolate VCCBAT - Isolate to battery
2.5V/3.0V	VCCPD	I/O pre-driver power	Share
<b>Transceiver Voltages</b>			
0.9V	VCCHIP	XCVR hard IP digital power	Share
1.1V	VCCR VCCT VCCL_GXB	XCVR receiver analog power XCVR transmitter analog pwr XCVR clock power	Share/Isolate
1.4V/1.5V	VCCH_GXB	XCVR TX output buffer power	Share/Isolate
2.5V/3.0V	VCCA	XCVR high voltage power	Share/Isolate

## Ferrite Bead Filtering

You can use ferrite bead filtering as an additional form of isolation to help overcome some of the challenges of designing an efficient PDN with multiple voltage rails targeting a high-speed FPGA. Isolation of sensitive power sources for key areas may require multiple regulators. However, through the use of ferrite beads, multiple voltage rails can share the same regulator while remaining isolated from other voltage planes. A Low-Q Ferrite Bead has high impedance over a broad high frequency band, making it a very good low pass noise filter. Designers must avoid common side effects of a ferrite bead, such as voltage ringing and anti-resonance.

 For a more in depth explanation on designing with ferrite beads, refer to [AN 583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs](#).

## Decoupling Analysis

The decoupling design is a critical component of a PDN. A conventional approach to decoupling does not meet the requirements of high-speed FPGA PDNs. You can use Altera's PDN tool to perform extensive analysis and implement a precise decoupling design. The PDN tool analyzes each voltage plane to construct a decoupling design based on the following factors:

- Spreading inductance
- Capacitor mounting via inductance
- BGA via inductances
- Plane capacitance
- Regulator type

Including all components of the voltage rail in the analysis enables the designer to accurately decouple the voltage plane.

 For more information on Altera's PDN tool, refer to the [Power Distribution Network Design Tool](#) website.

## Recommended Single Package Solutions

Linear Technology, National Semiconductor, and Intersil offer single package solutions that integrate components such as DC/DC controllers, inductors, and power MOSFETs into the package. Vendors typically provide evaluation boards for testing various regulator types. Altera recommends using such a board to evaluate the performance of your desired power supply before making a selection.

### Linear Technology

Linear Technology's  $\mu$ Module power supplies are a solution for high-speed transceiver PDN designs. These integrated switching power supplies can provide an efficient, high current solution while ensuring a low output voltage ripple as well as low switching noise normally associated with traditional switching regulators. Current mode architecture allows the addition of extra capacitance at the output to achieve a low ripple without affecting the stability of the power supply. Encapsulating the power supply components in a single package allows the parasitic capacitances and inductance to be tightly controlled therefore reducing EMI and switching noise from the power supply. The list below highlight reasons why these power supplies are ideal for high speed transceivers:

- Small form factor
- Tight load/line regulation
- Very low output ripple
- $13\times C/W$  to  $15\times C/W$  thermal resistance
- Multi-output devices
- Tested/characterized as single IC
- No power cycle failure
- Variety of I/O levels
- Variety of output current levels
- As easy to design as an LDO

 For more information on Linear Technology's  $\mu$ Module family, visit the  [\$\mu\$ Model Regulators](#) website.

## National Semiconductor

National Semiconductor's SIMPLE SWITCHER Power Modules are a power supply solution for high-speed transceiver and other noise-sensitive signal path ICs. These modules utilize a single, exposed bottom package technology for thermal performance and reliability. These modules integrate a shielded inductor and key signal path control circuitry, while reducing parasitic capacitance and trace inductance. The modules deliver the efficiency of a synchronous switching regulator with the simplicity of a linear regulator. By completely containing the switching elements inside the package, these devices offer low EMI performance. National Semiconductors Power Modules also offer pin-to-pin compatibility across current options within each family, meaning only one design and layout is needed to support up to six different power supplies.

 For more information on National Semiconductor's Simple Switcher family, visit the [SIMPLE SWITCHER Voltage Converter Family](#) website.

## Intersil

Intersil's ISL8200M is a high-power, current-sharing DC/DC power module suitable for datacom, telecom, and FPGA applications. Patented current sharing in multi-phase operation reduces ripple currents and complexity. Parallel configurations of this regulator can offer up to 60 amps of current capability. The ISL8200M's thermally enhanced, compact QFN package operates at full load and over-temperature, without requiring forced air cooling.

 For more information on Intersil's Power Module family, visit the [Power Modules](#) website.

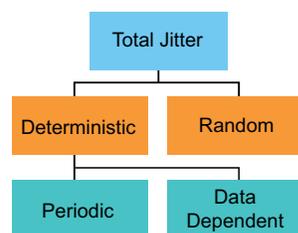
## PDN Performance Examples

This section provides an explanation of the impact of PDN noise on jitter components, followed by a test case that demonstrates the affects a PDN can have on the performance of the transceiver in an Altera Stratix IV GX device, using different PDN configurations.

### Affected and Unaffected Jitter Components

PDN noise has a significant impact on jitter components. [Figure 3](#) illustrates the different components of jitter explained in [Table 3](#).

**Figure 3. Jitter Tree**



To determine affected jitter components in a PDN design, define each jitter component by its cause. For example, when Periodic Jitter (PJ) has a sinusoidal property, it is usually related to interference from a data pattern, or fluctuations of a power source. Inadequacies in the PDN can affect PJ. For example, an underrated regulator can be a source of fluctuations on a voltage rail. A poor decoupling design can cause a voltage rail to sag. Table 3 details the impact of PDN noise on jitter components.

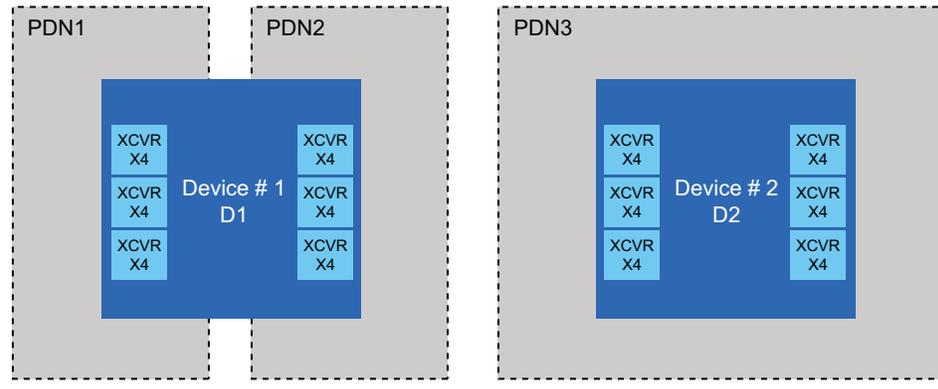
**Table 3. Impact of Noise on Jitter Components**

Jitter Component	Description	Impact
Total Jitter (TJ)	Peak to peak value of the summation of DJ and RJ	N/A
Deterministic Jitter (DJ)	Clock timing or data signal jitter that is predictable and reproducible. It's also bounded and has a non-Gaussian probability distribution	Related to device imperfections, Electro-Magnetic Interference (EMI), crosstalk, and grounding problems. The grounding problems may be connected to a component or group of components that make up the PDN. EMI and crosstalk are not likely related to the PDN design.
Random Jitter (RJ)	Unpredictable electronic timing noise. It's unbounded and follows a Gaussian distribution	Unpredictable and can be caused by timing noise, thermal noise, white noise, or even shot noise. When there are variations in a current source, the difference in those levels of current are sources of noise. Some devices that rely on a stable current source may be susceptible to this noise. It is evident the PDN design can have an impact on the RJ component. The test case described in the next section relies on a RJ(rms) measurement to quantify the performance of the transceivers.
Periodic Jitter (PJ)	A periodic shift in phase of a signal; falls under the Deterministic Jitter category	Falls under the DJ category.
Data Dependent Jitter (DDJ)	Timing jitter that's correlated to a sequence of bits in a data stream; falls under the Deterministic Jitter category. It's also classified as a form of ISI.	Causes are component and system bandwidth limitations. This jitter component consists of both ISI and DCD. The ISI is the most common form of DDJ and arises from limitations in the bandwidth of transmission lines or a device driver or buffer. Frequency dependent loss is another major source of ISI as well.

## Transceiver Performance Experiments

The following experiments use a dual Stratix IV GX (EP4SGX230KF40C2) test board to measure the performance of transceivers in different PDN configurations. The transceivers are situated on each side of the device, as shown in [Figure 4](#).

**Figure 4. Altera Power Share Board Diagram**



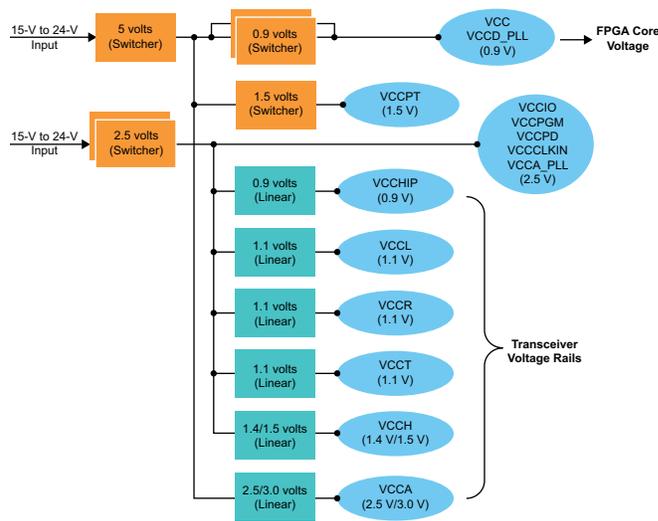
Device #1 has each side design with its own unique PDN. Device #2 has a unique PDN design for both sides. This setup creates three unique PDN designs that share or isolate transceiver power rails. The three configurations are referred to as “PDN1,” “PDN2,” and “PDN3.” Within each configuration, various power sharing, isolation, and regulator types are specified for experimentation and comparison purposes.

The goal of this experiment is to determine the effects of sharing critical transceiver voltage rails and drive them with various regulator types. The test measures RJ(rms) value of a victim transceiver channel (passing a high frequency pattern - 1010), while all other transceiver channels are running PRBS31 data. Data is collected over different configurations and multiple data rates from 4.25Gbps to 8.5Gbps. The RJ(rms) parameter provides the key metric for assessing performance because this parameter has the most impact on performance.

### PDN Configuration 1

In PDN1, all six transceiver voltage rails are isolated and driven by a linear regulator. Each voltage rail has its own voltage plane, as shown in [Figure 5](#).

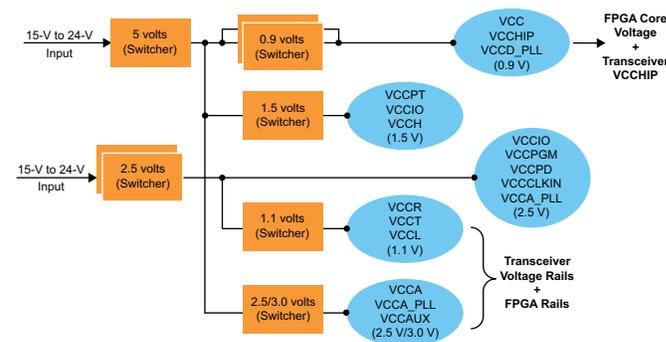
**Figure 5. PDN1 Power Tree**



**PDN Configuration 2**

In PDN2, all like transceiver voltage rails are shared with another like voltage rail. The shared voltage rails have their own voltage plane. All voltage rails are driven by a Linear Technology  $\mu$ Module switching regulator, as shown in Figure 6.

**Figure 6. PDN2 Power Tree**



- VCCHIP (0.9V) shares with VCC (0.9V)
- VCCR (1.1V) shares with VCCT (1.1V) shares with VCCL (1.1V)
- VCCH (1.5V) shares with VCCPT (1.5V)
- VCCA (2.5V) shares with VCCIO (2.5V)

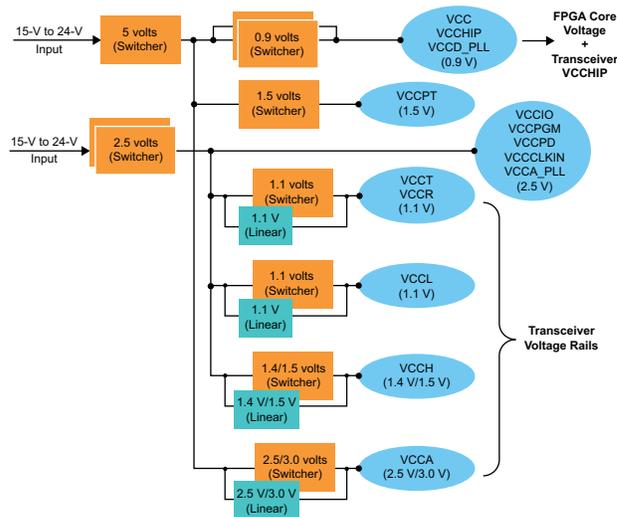
### PDN Configuration 3

In PDN3, two of the transceiver voltage rails are shared and driven with either a linear regulator or Linear Technology's  $\mu$ Module switching regulator.

- VCCHIP (0.9V) shares with VCC (0.9V)
- VCCR (1.1V) shares with VCCT (1.1V)

The remaining transceiver voltage rails are isolated and have their own voltage plane. These voltage rails can be driven with either a linear regulator or by a Linear Technology's  $\mu$ Module switching regulator, as shown in [Figure 7](#).

**Figure 7. PDN3 Power Tree**



### Test Case

The test case consists of 12 transceiver channels passing data. A single channel is designated as the victim, and its TX output is fed to the input of a spectrum analyzer. This victim channel passes a high frequency pattern (1010). The remaining 11 aggressor channels are all externally looped back and pass a PRBS31 data pattern originating in the core of the FPGA device. Each measurement is duplicated multiple times to insure reproducible results.

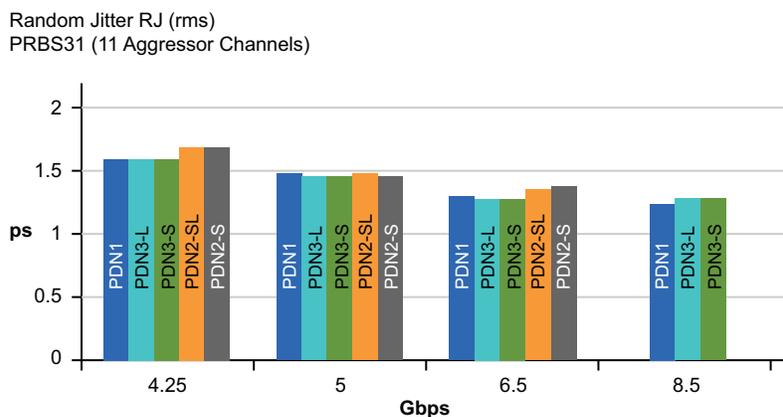
Initial tests begin with data collection from PDN1 to establish a baseline. PDN1 should produce the best results considering all transceiver voltage rails are isolated. Next, other combinations of the remaining configurations are tested and the data collected. All data is measured by an Agilent E4440A Spectrum Analyzer, measuring the Phase Noise or RJ(rms) in pico seconds.

### Test Results

[Figure 8](#) summarizes the data collected over 5 different configurations. PDN1, PDN2, and PDN3 configurations represent the isolation or sharing of voltage planes. PDN2 and PDN3 also have the added ability to choose between a switching regulator and a linear regulator for certain transceiver voltage rails. The configurations of the graphs are identified as the following:

- PDN1 - (XCVR rails = all linear regulators)
- PDN3 - L (XCVR rails = all linear regulators)
- PDN3 - S (XCVR rails = all switching regulators)
- PDN2 - SL (XCVR rails = combination of linear/switching regulators)
- PDN2 - S (XCVR rails = all switching regulators)

**Figure 8. RJ(rms) Data**



PDN2 configuration does not support 8.5Gbps due to design constraints of the board.

As previously explained, the RJ(rms) parameter has the most impact on the total performance. The test case looks at relative measurements with different conditions and focuses on the RJ(rms) value as a means to evaluate that performance. This experiment clearly demonstrates that transceiver performance is not affected as a result of combining voltage rails and changing the regulator type.

## Conclusion

This paper illustrates how designers can use advanced switching regulators to improve performance in low noise applications by balancing jitter margin and regulator count. The data collected from these experiments show little difference in performance between different configurations when implementing Altera's Stratix IV GX devices. This data covers configurations up to 8.5Gbps. Designers can achieve a more simple and effective PDN design by combining voltage rails and using new power module technologies.

## References

- *AN583: Designing Power Isolation Filters with Ferrite Beads for Altera FPGAs.*  
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- Intersil's Power Module Family website  
<http://www.intersil.com/powermodules/>

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