

Since their introduction in the mid-1980s and across all end markets, CPLDs have been design engineers' favorite choice for control path applications. Taking into account today's severe pressure to lower costs and power consumption, this white paper examines how Altera® MAX® V CPLDs provide solutions for the top five control-path applications.

## Introduction

With their mix of low price, low power, and high performance, MAX V CPLDs deliver the market's best value. Featuring the industry's first LUT-based, non-volatile architecture and one of the largest CPLD densities, MAX V devices provide higher performance (up to 247.5 MHz) at up to 50 percent lower total power compared to competitive CPLDs. These features allow the following applications to be best served by CPLDs:

- I/O expansion—Performs I/O decoding, which increases the available I/O capability of another standard device with efficiency and at a low cost.
- Interface bridging—Translates bus protocols and voltages between incompatible devices at the lowest possible cost.
- Power management—Manages the power-up sequencing and monitoring of other devices on the board.
- Configuration and initialization—Controls the configuration or initialization of other devices on the board.
- Analog control—Controls analog standard devices (light, sound, or motion) digitally via a pulse-width modulator (PWM), without needing a digital-to-analog converter (DAC).

## I/O Expansion

Engineers like to reuse their favorite ASSPs across multiple end products. Since each ASSP has a fixed number of I/O pins and associated functions, this can be a problem if the next end product needs more I/Os or different functionality. By using a few general-purpose I/O pins, CPLDs decode and expand the I/O capability of standard products, allowing engineers to reuse their favorite ASSPs while adding new functionality at minimal cost. MAX V CPLDs, with flexible I/O capability and a selection of package options with a high number of I/Os and logic per package area, are an ideal complement to today's I/O pin-constrained ASSPs and microcontrollers. Some CPLD features that ease I/O expansion design challenges include:

- Low cost per I/O pin or I/O density per board area

- Flexible I/O banks and I/O options (i.e., supporting multiple voltages, Schmitt triggers, etc.)
- Reprogrammability to solve design-specific problems and last-minute changes

Table 1 compares the I/Os and logic in MAX V CPLDs with competing products.

**Table 1. I/Os per mm<sup>2</sup> and Logic Density per mm<sup>2</sup> Comparison of Comparable Density CPLDs**

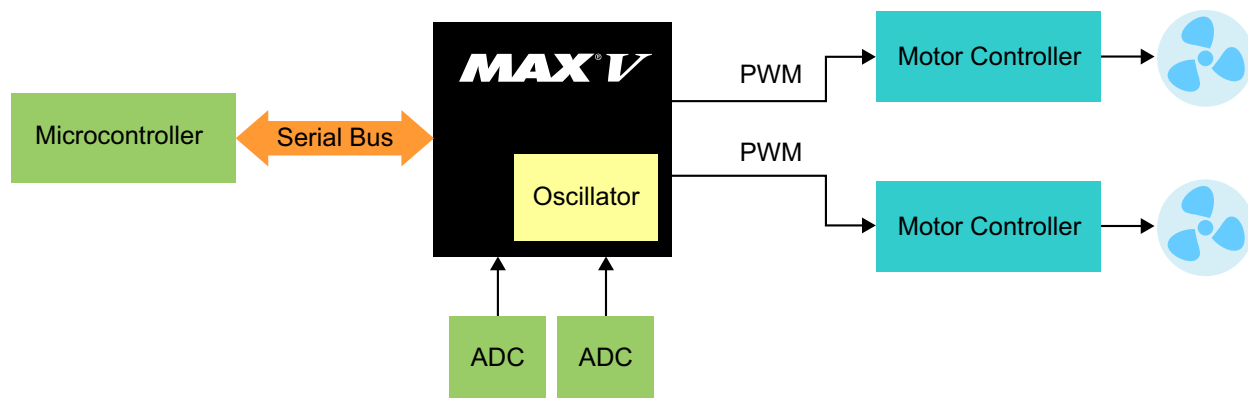
Vendor	CPLD Family	Device	Package/ Body Size (mm)	Available User I/Os	Available User Logic (1)	I/Os per Package Area (mm <sup>2</sup> )	Logic per Package Area (mm <sup>2</sup> )
Altera	MAX V	EP5M40Z	64-MBGA 4.5 x 4.5	30	~32	1.48	1.58
Altera	MAX V	EP5M40Z	64-EQFP 7 x 7	54	~32	1.10	0.65
Xilinx	CoolRunner II	XC2C32	QF32 5 x 5	21	32	0.84	1.28
Xilinx	CoolRunner II	XC2C32	CP56 6 x 6	33	32	0.92	0.89
Lattice	MachXO, MachXO2	No 32- or 64-macrocell devices available				-	-

**Notes:**

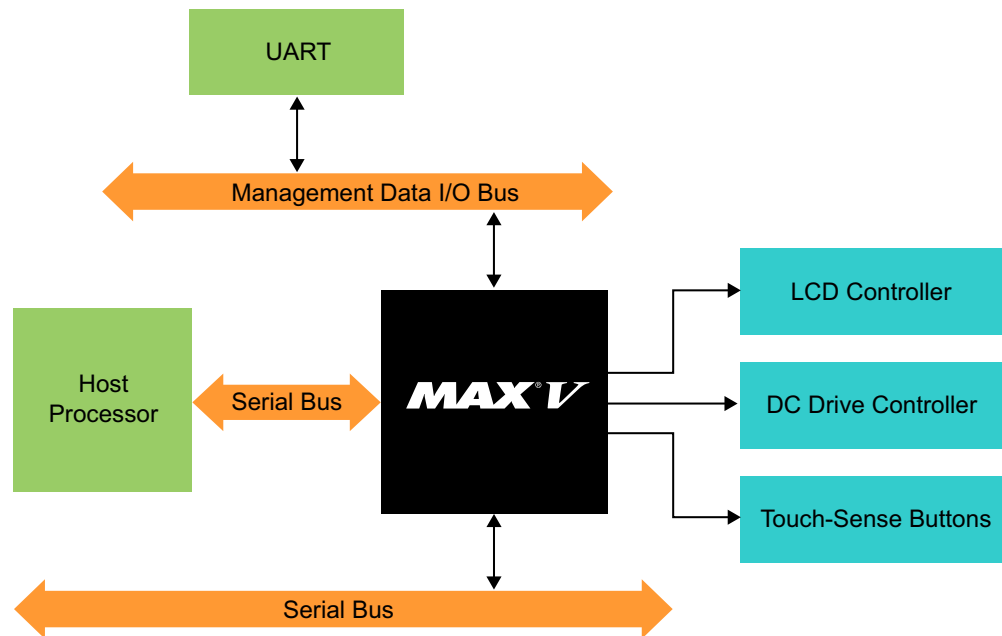
(1) LUT-based CPLDs have been converted to equivalent macrocells, based on benchmark analysis.

Figure 1 shows how a microcontroller with limited I/O capability can control many devices in a system by using only a two-wire serial bus. In this example, the MAX V CPLD interfaces to the serial bus input and then distributes instructions to control multiple devices (in this case, fan motor controllers). The MAX V CPLD's on-board oscillator can be used to periodically monitor for inactivity and shut-down the fans to conserve system power. Data can also be converted from parallel to serial, such as taking information from multiple analog-to-digital converters (ADC) and communicating it to the microcontroller via the serial bus.

**Figure 1. Expanding a Serial Bus Using MAX V CPLDs**



Choosing the best microprocessor within a given processor family depends on many factors, including the number of available general-purpose I/Os. Choosing a lower I/O count microprocessor paired with a low-cost CPLD is often cheaper than a standalone microprocessor with higher I/O count. Figure 2 shows how MAX V CPLDs can control a large number of devices on the board with only a minimal number of inputs from the host processor.

**Figure 2. Minimizing Processor Costs by Distributing Control Signals via MAX V CPLDs**

## Interface Bridging

The number of bus protocols and voltage levels supported by ASSP and microcontroller vendors continues to expand. Simple and in-expensive translation between these interfaces is needed. MAX V CPLDs are designed to support many types of interface bridging applications, including

- Voltage-level shifting—i.e., 3.3 V in, 1.8 V out
- Bus translation applications—Convert proprietary interfaces to industry-standard protocols
- Multipoint bus bridging
- Serial-to-parallel and parallel-to-serial bus conversions
- Encryption—Encrypts and decrypts data

Figure 3 shows how designers can use MAX V CPLDs to implement a low-cost, low-power LCD controller and interface to a LCD display. The boards may be physically separated via a flex cable or as part of a backplane configuration. As new LCD models become available, the LCD controller can be updated to accommodate new technical requirements for different screen sizes or proprietary interfaces. Thus the design engineer has the flexibility for real-time selection amongst LCD vendors based on the LCD's cost, power, and features.

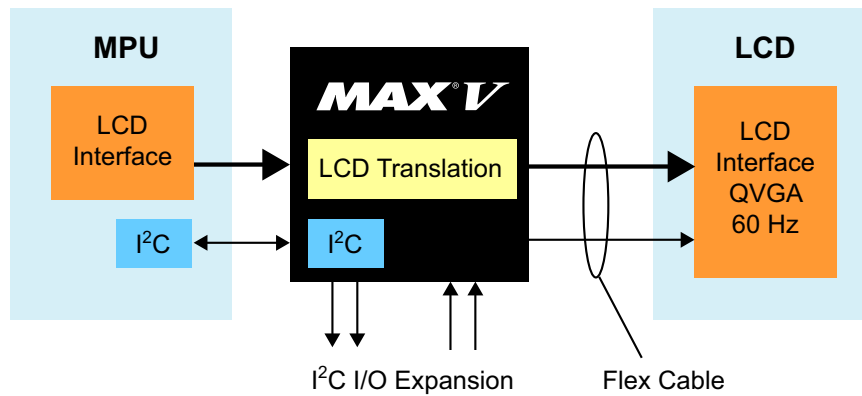
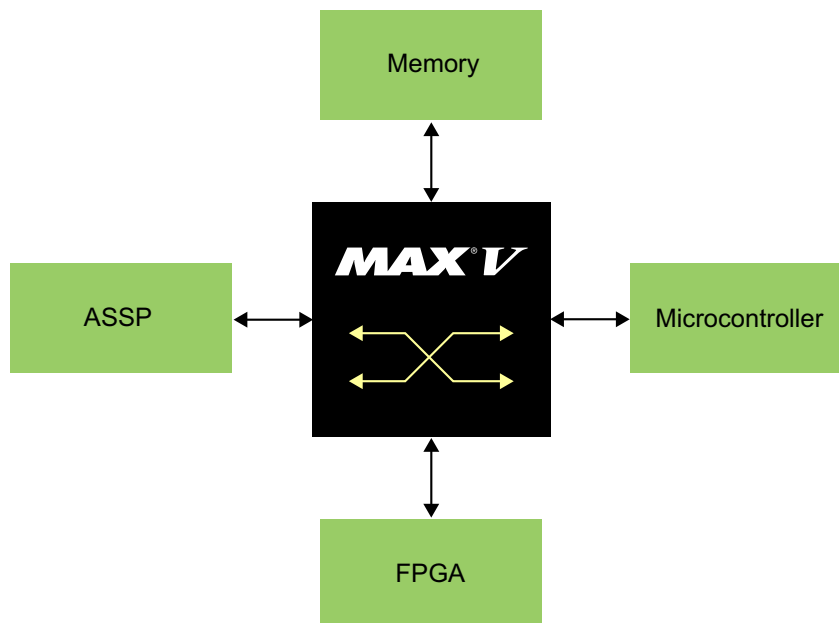
**Figure 3. Implementing a Customizable LCD Controller Interface Using MAX V CPLDs**

Figure 4 depicts how MAX V CPLDs can function as a crosspoint switch to enable multipoint connections. Using programmable logic in this application enables the greatest flexibility to match the requirements of any specific design. In this application, the logic in the MAX V CPLD is divided into three major blocks:

- Switch matrix—Connects any input to any output
- Configuration register—Reconfigures connections during operation
- Address decoder—Decodes the output addresses of the configuration

**Figure 4. Multipoint Connections Using a MAX V CPLD**

Interface bridging requires a large number of I/O pins to support the bus interfacing, but not a lot of logic. MAX V CPLDs offer a high I/O count and a low logic ratio that provides engineers with the lowest possible cost per I/O pin. For applications needing more complex logic functions along with high I/O counts, Altera's Cyclone® series of FPGAs may offer better cost per logic than CPLDs.

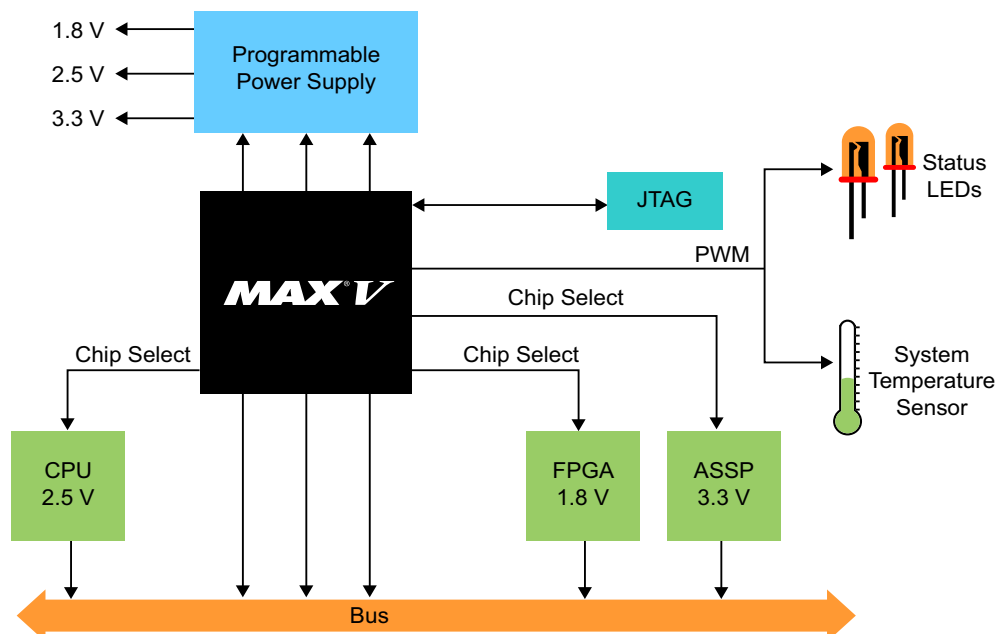
## Power Management

As board density and the number of power planes on a board increase, the complexity of the power management also increases. Various power management tasks include multi-voltage system power-up, system reset, chip-select generation, and real-time monitoring. MAX V CPLDs have the features and density to integrate all these functions, including the following, into a single non-volatile, instant-on device:

- Instant-on—Allows MAX V CPLDs to power up first (in 500  $\mu$ s or less) and then manage the start-up sequences for other devices.
- MultiVolt—Allows a designer to select the most convenient I/O voltage for the power management interface: 3.3-, 2.5-, 1.8-, 1.5- or 1.2-Volt.
- Internal oscillator—Useful for periodic monitoring the status of various power planes, associated power supplies, and downstream devices
- User flash memory (UFM)—Non-volatile storage captures system information for debug and diagnostic.
- Hot socket compliance—Allows CPLDs to be plugged into and out of a live system without damage, an optimal solution for controlling the power management of plug-in boards.
- Analog interface—Allows PWM to interface with various analog standard products, such as temperature, pressure, and voltage sensors.

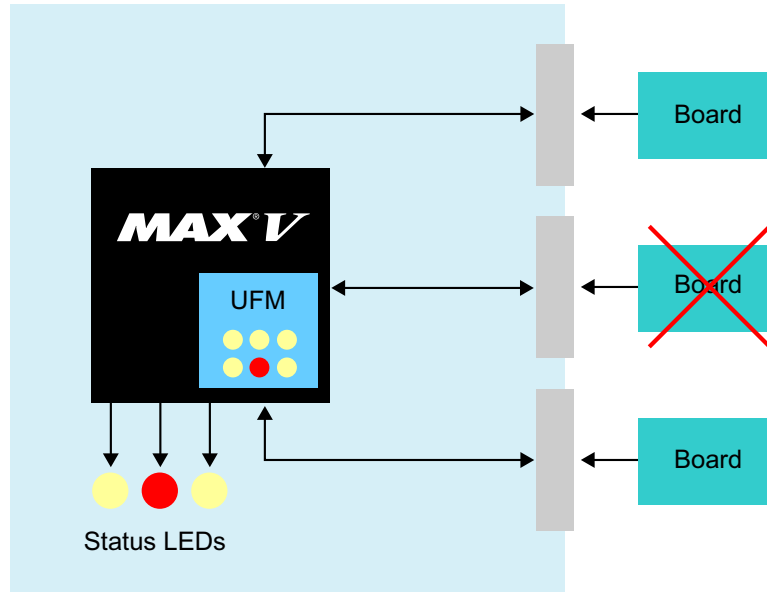
Figure 5 illustrates a typical MAX V CPLD power-management application. Because multiple power rails support different devices, a control logic is needed to manage the complete power-up sequence of each device. To ensure that accidental driving of these signals does not occur during power up, the MAX V CPLD is also used to control critical bus signals until the power up is complete. The JTAG port monitors the power-up sequence, storing errors and information upon power up. The port can also be used to set break points in the power-up sequencing, which is useful during the debug phase.

**Figure 5. Multi-Voltage System Power-Up Management Using a MAX II CPLD**



As shown in Figure 6, the MAX V CPLD can also monitor the addition or removal of boards to the backplane. The high-current CPLD I/O enables LEDs to directly indicate which boards are plugged in, while the user flash memory can log this information for debug/diagnostic purposes.

**Figure 6. Board Swapping Management and Monitoring**



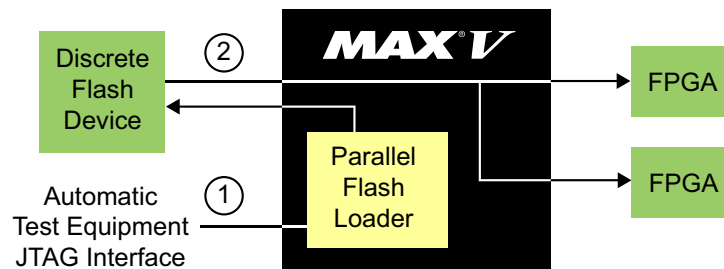
## Configuration and Initialization

CPLDs are commonly used to manage the configuration or initialization of other volatile devices. Examples of components that require configuration or initialization include FPGAs, digital signal processors, ASSPs, ASICs, and discrete flash memories.

MAX V CPLDs' fast instant-on performance powers-up first and then manages the configuration and initialization of the other devices. Real-time ISP allows the MAX V CPLD to function while downloading and storing a second programming bitstream, reducing system downtime. The reprogramming occurs immediately or at the next power-up scheduled by the user.

To simply program the discrete flash memory or FPGA device configuration, Altera provides the Parallel Flash Loader IP. As shown in Figure 7, the initial step of the configuration application demonstrates the flash programming application. This function configures the flash device using JTAG via the CPLD's JTAG pins. Non-JTAG-compliant flash memory devices can also be configured using the Parallel Flash Loader IP.

**Figure 7. FPGA Configuration Management and Flash Controller Using a MAX VCPLD**



The second step of the configuration application uses the newly programmed discrete flash memory to configure one or more FPGAs. This is a cost-effective, flexible solution utilizing any shared, low-cost flash memory device on a system board. As the highest density CPLDs available, MAX V devices support extremely complex configurations, including those having multiple pages within the flash memory to program the FPGA with many different functions.



For further information regarding the Parallel Flash Loader IP, refer to Altera's application note, *Using the MAX II Parallel Flash Loader with the Quartus II Software*.

## Analog Control

The LUT-based logic architecture, high drive-strength I/Os, and internal oscillator of MAX V CPLDs enable a direct connection to various analog standard products via a PWM interface. This can eliminate the need for a DAC and allow for very precise control of analog products, including:

- Lighting—LED blinking or back-light intensity
- Motion—Various types of motors and servos
- Sensors—Pressure, temperature, voltage, etc.
- Sound—Speakers, etc.

Finely tuned digital control of analog products can help to reduce the power consumption of these analog functions.

## Conclusion

The architecture and features offered by the MAX V family allow the top five CPLD applications described in this white paper to be implemented in a single low-cost, low-power CPLD. MAX V devices are therefore ideal for the next design no matter the market segment: wireline, wireless, industrial, consumer, computer/storage, automotive, broadcast, or military. The CPLD market-share leader, Altera has a track record of ramping to high volume quickly and supporting OEMs with devices that have long life cycles.

## Further Information

- MAX V CPLDs: Cool Value:  
[www.altera.com/products/devices/cpld/max-v/mxv-index.jsp](http://www.altera.com/products/devices/cpld/max-v/mxv-index.jsp)
- Literature: MAX V Devices:  
[www.altera.com/literature/lit-max-v.jsp](http://www.altera.com/literature/lit-max-v.jsp)
- *Using the MAX II Parallel Flash Loader with the Quartus® II Software:*  
[www.altera.com/literature/an/an386.pdf](http://www.altera.com/literature/an/an386.pdf)

## Acknowledgements

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## Document Revision History

Table 2 shows the revision history for this document.

**Table 2. Document Revision History**

Date	Version	Changes
February 2011	1.2	Minor text edit.
January 2011	1.1	Minor text edits.
December 2010	1.0	Initial release.