The development and deployment of network-centric operations and warfare (NCOW) to integrate and connect the military's many separate networks relies on high-speed packet transport and optical networking. Altera's 28-nm Stratix® V FPGAs combine the flexibility needed to adapt to changing network standards and support legacy network interfaces and protocols, while offering the ASIC-like performance traditionally required for these applications. This unprecedented combination of technological advances enables advanced network developers to implement and deploy military capabilities in a secure and flexible manner while dramatically reducing non-recurring engineering (NRE) and critical time to mission.

Introduction

With the tremendous success of commercial Internet and wireless technologies, the Department of Defense (DoD) has sought to implement a similarly interconnected infrastructure to enable NCOW information sharing and interoperability functions. The fragmented nature of the existing DoD information technology (IT) infrastructure has measurable impacts on the pace of operations and the duplicative costs of redundant infrastructure.

Much as the current Internet integrates and connects multiple networks and data types, NCOW provides the ability to access, post, process, and protect data from anywhere within the network. This fundamental change in doctrine is designed to support advanced warfighter edge-of-the-network applications and information sharing across organizations.

This white paper identifies key technologies needed to enable the migration to the DoD NCOW mission. As commercial networks merged and migrated, network bridging, evolving standards, and network security provided important lessons in hardware design flexibility. This flexibility has been even more prevalent as technology moves from 10G to 40G and 100G networks. The unique ability of Altera® Stratix V FPGAs to implement these high-speed interfaces, coupled with reconfigurability and security, is a proven technology path for next-generation networking.

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Global Information Grid

To overcome these informational and communication firewalls, a national strategy was developed to build and integrate the DoD enterprise architecture. One output of this strategy is the development of the Global Information Grid (GIG), shown in Figure 1. The GIG is designed to provide information capabilities that enable the access and exchange of information and services within the DoD and extending to mission partners. The DoD describes the GIG as a "globally interconnected, end-to-end set of information capabilities, associated processes, and personnel for collecting, processing, storing, disseminating, and managing information." *(1)*

Figure 1. Basic GIG Architecture
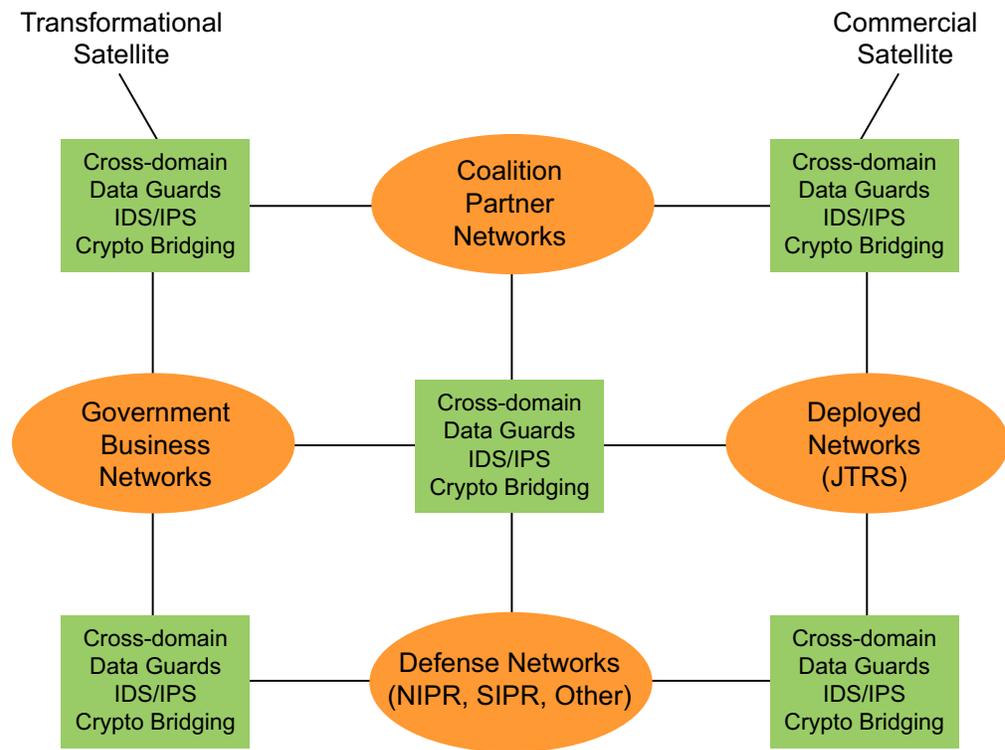
Several key developments are part of the GIG acquisition:

- Transformational satellites (not necessarily TSAT)—Satellite systems capable of increased bandwidth and network routing and/or switching

- Joint Tactical Radio System (JTRS)—A new family of interoperable radio systems supporting mobile users with multiple waveforms and encryption

- Global Information Grid-Bandwidth Expansion (GIG-BE)—A state-of-the-art optical network designed for 40G to 100G and 400G technology transitions, including upgraded routers and switches to increase bandwidth for greater voice, data, and video transmissions

- Network-Centric Enterprise Services (NCES)—A common set of services and applications to manage the network and help users locate and share information including cyber security

- Information Assurance—Tools to protect sensitive information transmitted across the network *(2)*

■ Horizontal Fusion—A portfolio of initiatives focused on developing and demonstrating data applications and tools for information sharing and net-centric operations

Communications Transformation

As illustrated in Figure 2, the rapid growth in commercial network bandwidth is driven by increasing numbers of broadband subscribers via xDSL, FTTx, WiMAX, and the proliferation of 3G/4G mobile wireless devices. The applications driving this bandwidth growth include Internet Protocol television (IPTV), Voice over Internet Protocol (VoIP), and online gaming, as well as a growing number of online users accessing video-on-demand sites. Today, multiple commercial networks, such as wireline carrier networks, cable operators, and mobile operators, coexist, providing broadcast and on-demand content, including ever-increasing amounts of video content. Independent of the source of the content or the delivery mechanism, the network for all these services is IP based with huge bandwidth demands in the core of the transport network.

Figure 2. Commercial Bandwidth Growth Is Driven by Video
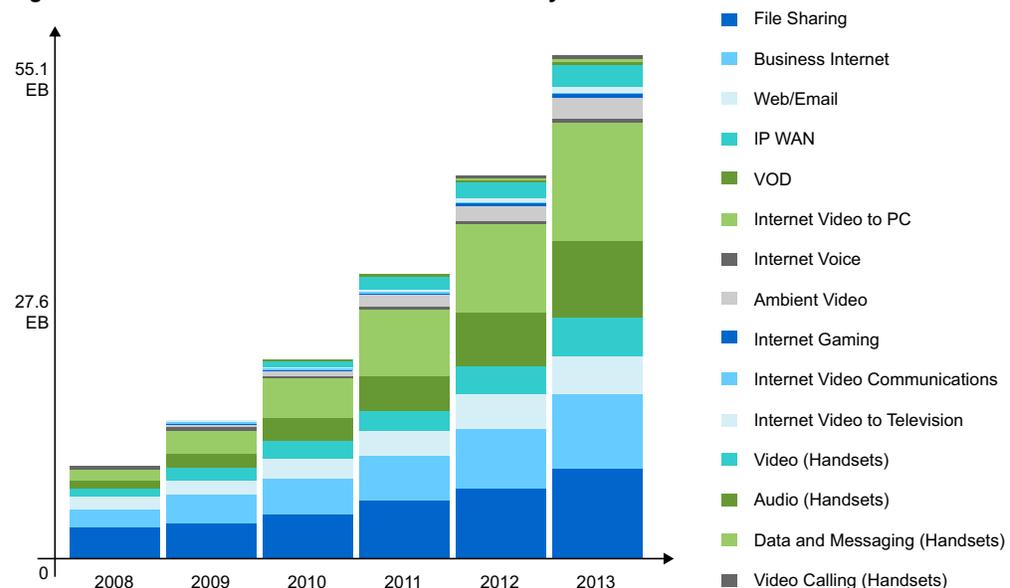
Source: Cisco VNI, June 2009

As with the growth in commercial network bandwidth, military network bandwidth is expected to grow rapidly in the near future. Similarly, applications driving network bandwidth can be expected to include rapid growth in the mobile user communities of JTRS and Mobile Use Objective System (MUOS), as well as the proliferation of high data-rate producers in the Intelligence, Surveillance and Reconnaissance (ISR) areas. As the network's core bandwidth expansion is deployed, the large numbers of networks interfacing and connecting through the GIG will pose interoperability, networking, and security challenges. Advanced technology with the performance and flexibility to enable power- and cost-effective network deployment and operations could be considered the final key to GIG acquisition.

40G-100G Network Technology Needs

As various commercial standards bodies finalize their 100G standards for transport, Ethernet, and optical interfaces, advanced technology adopters need to design flexible 40G and 100G production systems. Next-generation networks can be characterized most simply by the volume, velocity, and variety (V^3) of traffic growth. The key performance parameters (KPPs) of these V^3 networks focus on power efficiency to enable scaling of bandwidth, technology performance and efficiency capable of scalable data processing, and flexibility to adapt to emerging standards and ease network convergence.

The growth in the volume of network bandwidth has a direct impact on power and processing efficiency. Direct scaling of networking bandwidth is unsustainable. Network processing must become more efficient in terms of processing per-watt metrics, such as the watts per Gigabit shown in Figure 3.

Figure 3. Network Interface Efficiency, Chip Level View
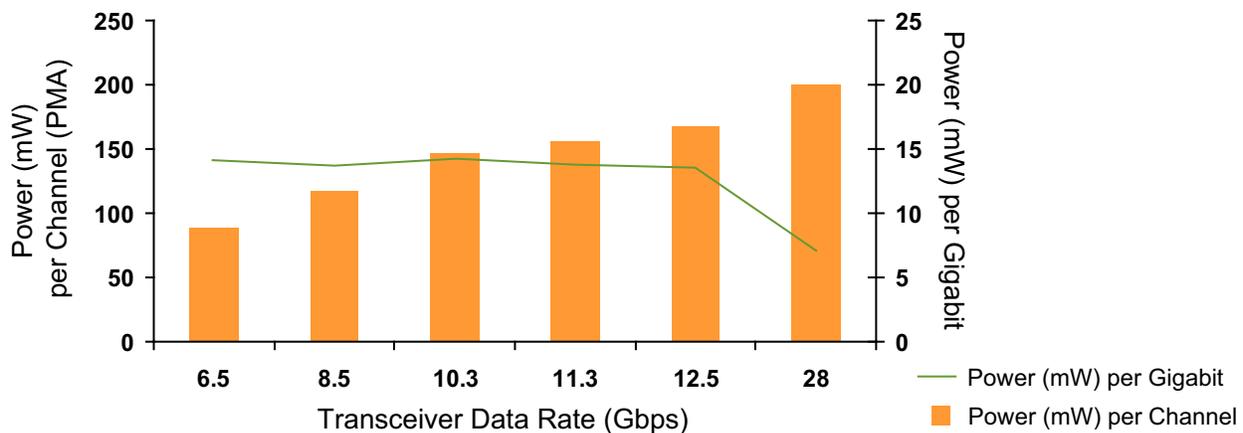
Following Moore's law, operators have traditionally used the next silicon process-node geometry to meet data processing needs by doubling density approximately every 18 to 24 months. However, Gilder's law ("The total bandwidth of communication systems will triple every twelve months.") is also expected to hold for the foreseeable future. Advanced processing solutions such as Altera's Stratix V FPGAs leverage numerous proven processing techniques and architectural innovations including Programmable Power Technology and dynamic on-chip termination to minimize system power while supporting high system bandwidths for 40G, 100G, and 400G applications.

The velocity of next-generation network traffic may be the most difficult KPP to satisfy considering the 28.78125-GHz requirement of the CEI-28G protocol. In this case, executing the divide and conquer approach of Amdahl's law ("The speedup of a function using parallel processing is limited by the time needed for the sequential fraction of the program.") to trivially simple parallelism is neither power efficient nor scalable. Additionally, parallelizing algorithms due to technology performance limitations increases customer design cycles as system complexity is a side effect of massive parallelism. An FPGA solution, such as the Stratix V direct network interface shown in Figure 4, provides native 28.78125-GHz interfaces with the highest performance logic available, thereby reducing the need for massive parallelism and reducing development cost and risks.

Figure 4. Stratix V Direct Network Interface Reduces Power and Allows Adaptation
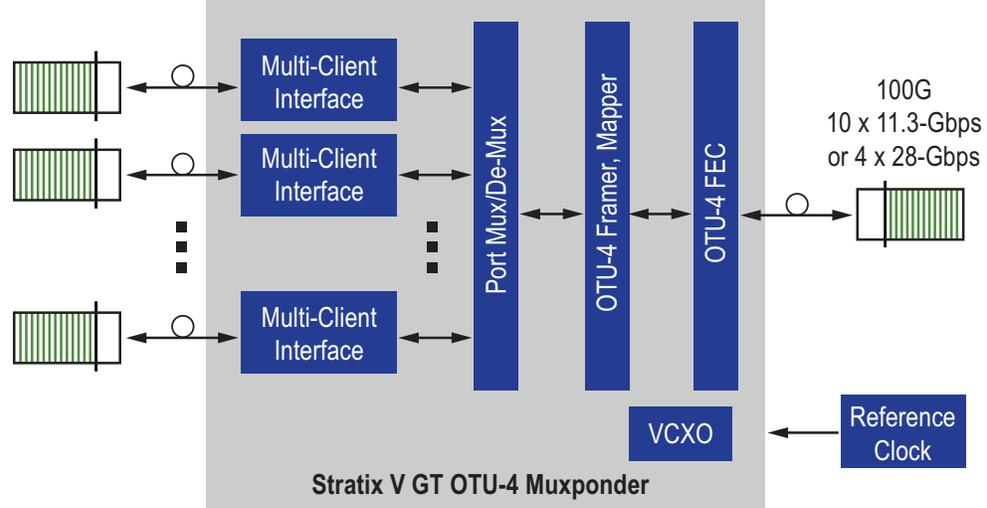
Network protocol variety and standards variations (proprietary implementations) necessitates technology flexibility. Enabling interoperability and convergence has focused commercial service providers on emerging 100G Ethernet standards (Figure 5) for their next-generation line-card options. To be ready to deploy these networks, a reconfigurable solution is needed as standards and interfaces may still be in draft form. Waiting for standard finalization to begin ASIC development is a significant time-to-market limitation for both commercial and military network providers.

Figure 5. Scalable and Reconfigurable Processing Using FPGAs
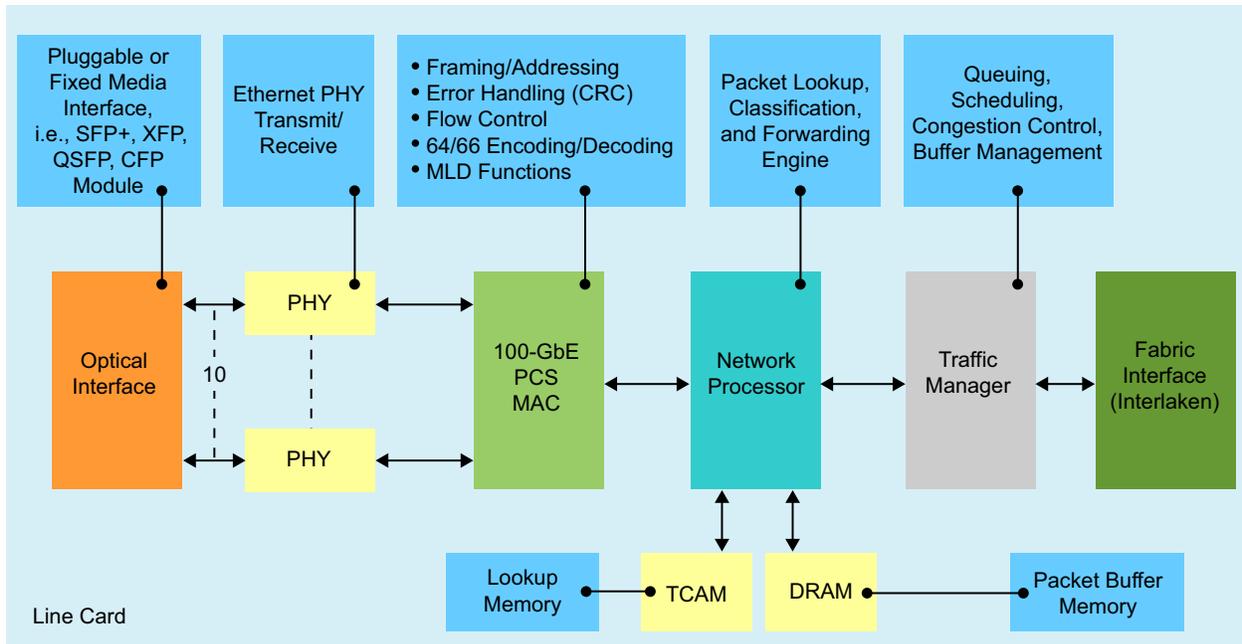
Security

With ubiquitous network connectivity, the need for security has become an increasingly critical need and challenge. A distributed network security model used by commercial networks is not necessarily sufficient for high military-grade protection. Legacy military networks being integrated by the GIG will need to account for potentially unique security architectures. Bridging and unifying multiple legacy security architectures into the GIG may require adapting many custom network protocols and interfaces to legacy cryptographic solutions. Additionally, advanced intrusion detection and protection (IDS/IPS) systems may be layered to monitor not only network endpoints but network core traffic as well.

Advanced FPGA Technology for 40G-100G and Beyond

Stratix V FPGAs address bandwidth, cost, and power challenges through processing techniques and unique architectural innovations that take a design beyond the benefits of Moore's law. Altera's FPGA technology provides the needed bandwidth, high transceiver count, 28-GHz I/O performance and embedded hard IP blocks to support multiple protocol standards on a single power-efficient device. By efficiently architecting the Stratix V FPGA around new and existing technology, designers now have many tools to optimize an FPGA design.

Altera Stratix V FPGAs make use of a myriad of power-saving techniques to optimize power such as Programmable Power Technology to reduce power in low performance signal paths. However, systems with large numbers of I/Os can be power limited if large numbers of high-speed I/Os are used, such as with 100G systems. To reduce this I/O scalability limitation, higher speed I/Os are needed. Altera's 28-GHz interfaces reduce the power per bit by as much as 50%. For example, 10 I/Os at 10.3 GHz require approximately 150 mW per I/O, resulting in 1.5 W of I/O power, while 4 I/Os at 28 GHz require less than 0.8 W and natively support 100-Gbps network interfaces.

While this reduction in I/O power is significant, additional power optimizing technology is needed to keep pace with the divergent growth curves of silicon technology and network bandwidth growth. To further optimize FPGA power, Altera has added Embedded HardCopy® Blocks (embedded hard IP (ASIC) partitions) within the FPGA, which improve performance and reduce power significantly.

By combining silicon technology advances with advanced FPGA architecture, programmable power technology, and ASIC technology, future FPGAs are capable of optimizing next-generation network processing using reprogrammable technology.

Embedded HardCopy Blocks

To achieve higher integration and performance on a single chip while reducing cost and power, Stratix V FPGAs (Figure 6) combine the reprogrammability of an FPGA with Embedded HardCopy Blocks in both the core and transceiver blocks to optimize power, performance, and time to market.

Figure 6. Hybrid FPGA and Embedded HardCopy Design

1.19M LEs or
14.3M ASIC Gates
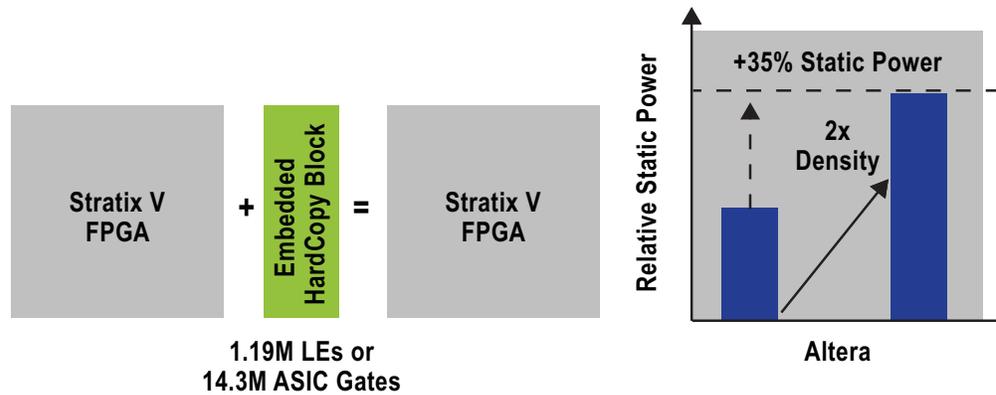
The Embedded HardCopy Blocks, shown in Figure 7, are customizable hard IP blocks that provide ASIC-like performance. This innovation substantially increases FPGA capabilities by dramatically increasing logic density per area while increasing performance and lowering power. The Embedded HardCopy Blocks are used to harden standard or logic-intensive functions such as interface protocols, application-specific functions, and proprietary custom IP as needed.

Figure 7. Hybrid FPGA HardCopy Implementation
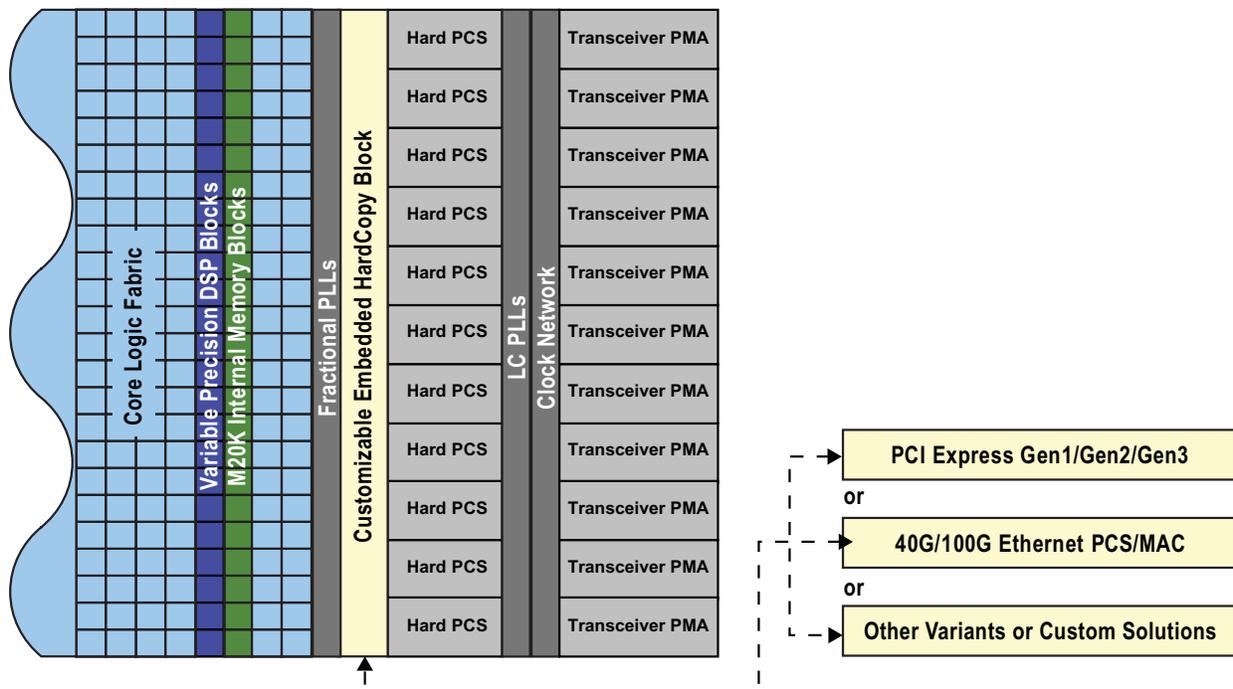
The complex integration of high-security networks relies on the ability to quickly and easily adapt to ever-changing protocol, security, and network challenges. Stratix V FPGAs provide the technical foundation needed for integrating very high performance networks, from network termination and packet processing to security-service integration and cryptographic bridging. Altera's advanced transceiver technology allows direct connectivity to the highest performance protocols and

Embedded HardCopy Blocks capable of interfacing with multiple custom network protocol variants while having the highest performance 28-nm reprogrammable logic available. This combination of technologies reduces the need and NRE required for costly ASIC development, and offer an adaptable and cost-effective commercial-off-the-shelf (COTS) solution.

Conclusion

The development and deployment of NCOW to integrate and connect the military's many separate networks is a long-term commitment. This type of next-generation network transformation relies on packet transport and optical networking as data traffic is expected to increase dramatically due to ISR data proliferation and a rapidly growing number of mobile users once JTRS and MUOS are fully deployed.

The technology increasingly utilized to deliver these network services are state-of-the-art FPGAs, such as Altera's Stratix V devices. These 28-nm FPGAs combine the flexibility needed to adapt to changing network standards and support legacy network interfaces and protocols, while offering the ASIC-like performance traditionally required for these applications. Stratix V FPGAs combine the highest performance silicon processes technology with 28-Gbps capable I/Os and Embedded HardCopy Blocks to create an entirely new class of reprogrammable devices.

This unprecedented combination of technological advances enables advanced network developers to implement and deploy military capabilities in a secure and flexible manner while dramatically reducing non-recurring engineering (NRE) and critical time to mission.

Further Information

1. U.S. General Accounting Office, Joint Warfighting: Attacking Time-Critical Targets, GAO-02-204R (Washington, D.C.: Nov. 30, 2001): www.gao.gov/new.items/d02204r.pdf

2. The Cryptography Transformation Initiative is part of DOD's broader Information Assurance program, which includes many security initiatives critical to the GIG.

3. Military End Market: www.altera.com/end-markets/military-aerospace/mil-index.html

4. Literature Military: www.altera.com/literature/end-markets/military-aerospace/lit-mil-aero.jsp

5. White Paper: *Introducing Innovations at 28 nm to Move Beyond Moore's Law*: www.altera.com/literature/wp/wp-01125-stxv-28nm-innovation.pdf

6. White Paper: *Addressing 100-GbE Line-Card Design Challenges on 28-nm FPGAs*: www.altera.com/literature/wp/wp-01128-stxv-100gbe-linecard.pdf

Acknowledgements

Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
September 2010	1.1	■ Added Figure 1 and Security. ■ Updated Embedded HardCopy Blocks.
September 2010	1.0	Initial release.