Corporate objectives, such as increasing profits and sales revenue while utilizing R&D efficiently, are putting severe pressure on today’s design engineering teams. The resulting system level challenges—creating new products and lowering the cost of existing “successful” products with fewer people and resources in less time—can be addressed by using a design philosophy based on FPGAs. A system architecture using FPGAs as a key component not only reduces new product-development R&D costs but also the TCO of a product’s entire life cycle. Altera’s new lowest cost, lowest power devices, the Cyclone IV FPGA family, will demonstrate how FPGAs can reduce total system costs.

Introduction

Global competition and economic factors are squeezing profits and sales of today’s high-tech products, putting tremendous pressure on design engineering teams to bring to market lower cost products. Investing R&D in new product development presents two different system challenges: creating completely new products that take advantage of the latest technologies, features, or solutions available in the market, and developing them for low cost.

For high-tech companies in today’s cost-conscious and power-sensitive “green” environment, the first challenge translates into creating a completely new product with functionality not offered by anyone else, while having a lower priced entry point and/or lower power footprint. For the second challenge, the cost reduction of existing successful products is typically handled by driving down the cost of the components from the product’s bill of materials (BOM). Another option is for design teams to redesign the product, not for new functionality, but to achieve more significant cost reductions.

Both of these system challenges are framed by a third challenge, which is especially relevant in today’s global economic situation: utilizing R&D for new and cost-reduced products with fewer people, less budget, and less time.

This white paper proposes a design philosophy that solves these three product-development challenges, as well as lowers costs throughout the product’s life cycle. This design philosophy is based on low-cost, low-power FPGAs. Although it is commonly known that FPGAs reduce the time to market for new product development, it is less well known that FPGAs reduce the total cost of ownership (TCO) during a product’s full life cycle. This FPGA-based design philosophy allows design engineers to:

- Easily and quickly add new functionality to products while reducing total power consumption
- Cost-reduce existing products with minimal functional changes
- Decrease a product’s TCO

Cyclone IV FPGAs

Altera’s Cyclone IV FPGAs, the lowest cost, lowest power devices with integrated transceiver options, are designed to lower the total system cost, defined as:

\[
\text{Total system cost} = \text{BOM costs} + \text{board costs} + \text{TCO}
\]

The Cyclone IV family comes in two different versions: the logic-only “E” variant and the “GX” variant with on-chip transceiver I/Os at speeds up to 3.125 Gbps. These high-speed transceivers support many serial I/O protocols, such as Gigabit Ethernet (GbE), PCI Express (PCIe), CPRI, XAUI, 3G Triple-Rate SDI, Serial RapidIO®, SATA, DisplayPort, and V-by-One, that are migrating from the cutting edge to the mainstream. Cyclone IV GX FPGAs also include an embedded PCIe hard IP block (Figure 1) that, when utilized by the design engineer, does not use any of the FPGA logic and supports more functionality than any other competing FPGA architecture.
As shown in Figure 2, Altera has worked with long-time fab partner TSMC to optimize the fabrication process to produce FPGAs with lower static and dynamic power, up to 25% and 30% less total power respectively compared to prior Cyclone families.

FPGAs are synonymous for getting products to market quickly by shortening the product development schedule. Engineers choosing Cyclone IV FPGAs, with up to 25% faster core performance (compared to competitor’s low-cost FPGAs), will spend fewer design iterations on timing closure because more timing margin is available. Furthermore, Altera’s Quartus® II design software has up to 50% faster compilation times versus competing software products, making engineers more productive, each and every day in the office.
For Cyclone IV GX FPGAs, Altera designed the transceiver I/O as small as possible to reduce costs and power, but created it in such a way that offers multiple clock sources from several on-chip phase locked loops (PLLs). Lowering the cost and power for the transceiver I/Os available in Cyclone IV GX FPGAs was a significant but necessary undertaking because mainstream adoption demands low price points and ease of use. This achievement leverages one of Altera’s key technological advantages, that of successfully designing and shipping transceiver-based FPGAs. As shown in Figure 3, Altera has already brought to market eight different product families across multiple device architectures, all designed by a single in-house design team.

Figure 3. Altera Transceiver Expertise

Based on this understanding of Cyclone IV FPGA features, the following five different application examples will illustrate how FPGAs can achieve lower total system costs.

**High-Definition Television**

This example (Figure 4) demonstrates how low-cost, low-power transceiver I/Os in a FPGA help to reduce total system costs by providing new functionality and higher bandwidth (using the V-by-One serial I/O protocol), while simultaneously reducing BOM and board costs. This 720p high-definition digital television (HDTV) uses 16 LVDS I/O signals between the tuner and panel printed circuit boards.

Figure 4. HDTV Display Example
Desirable new features for next-generation HDTVs include:

- Support for new video standards
- Increased image resolutions
- Move from 10-bit to 12-bit color
- Increased refresh rates to 240 Hz
- Maintain or reduce power and/or thermal dissipation

The bandwidth required to add these features needs as many as 36 LVDS I/Os, assuming the parallel I/O architecture between the tuner and panel boards is maintained. These I/Os will significantly increase the PCB size or PCB layer count, leading to increased costs. In addition, the greater number of LVDS I/O would significantly increase power dissipation. However, because HDTVs have become a mainstream consumer product, costs and power need to go down, not up.

One way to solve this system challenge is to reduce inter-board communication from 36 LVDS I/O pairs to four I/O pairs by implementing a new serial protocol standard called V-by-One. These four V-by-One pairs have enough bandwidth to support full HD resolution (i.e., 780p/1080p to 4K2K). This seemingly simple change in I/O standards helps to solve this system challenge in the following ways:

- Manufacturers typically measure FPGAs on a cost-per-density basis. A given number of I/Os come with each density FPGA. Because the number of I/O has been significantly reduced (36 to 4), a smaller density and therefore cheaper FPGA with fewer I/Os could be used (BOM cost reduction).
- The physical connection between the tuner and panel boards is implemented with a flex-cable plus connectors. By reducing the number of I/Os, the manufacturer can use a smaller, and therefore cheaper, flex-cable and associated connectors (BOM cost reduction).
- Because there are only four PCB traces to be routed instead of 36 traces, the PCB is smaller and less complex, and therefore costs less (board cost reduction).
- Because Cyclone IVGX FPGA only needs two power supplies, it uses fewer regulators than other transceiver-based FPGAs (BOM cost reduction).

A Cyclone IV GX FPGA-based solution also offers:

- Image-quality enhancements using the on-chip digital signal processing (DSP) resources along with video IP cores (designed into the FPGA logic)
- Better signal integrity using the smaller V-by-One protocol instead of LVDS cables and connectors

Re replacing ASICs and ASSPs

Figure 5 shows a product using low-cost ASIC and ASSP devices. This situation assumes new functionality is not yet available within an ASSP device or perhaps the ASSP is being obsolesced. FPGAs are commonly used to bridge devices with different voltage levels, voltage standards, or completely different protocols. The FPGA provides new functionality and higher bandwidth, but will the unit cost of the FPGA be higher or lower than the ASSP it replaces?
System costs savings from using an FPGA in this example include:

- No NRE cost and engineering time for an ASIC respin to support PCIe (TCO cost savings)
- No FPGA logic is used to implement the PCIe (MAC + PHY) functionality, so a smaller and cheaper FPGA can be used (BOM cost savings)
- Reduced inventory costs (TCO cost savings)

Using an FPGA does not require a manufacturer to purchase large quantities of inventory because FPGAs are inherently obsolescence-proof, with typical FPGA life cycles of 10 to 15 years, sometimes even 20 years. In comparison, if an ASSP is obsolesced, OEMs are forced to purchase large, multi-year quantities of “last-time buy” material.

**PCI Express**

While the previous example only shows the PCIe x1 lane endpoint functionality of the integrated hard IP block embedded in the Cyclone IV GX FPGAs, the PCIe hard IP block (shown in Figure 6) offers more. Cyclone IV GX devices are the only low-cost FPGAs to offer PCIe hard IP with up to x4 support for rootport and endpoint.

*Figure 6. Cyclone IV PCIe Hard IP Implementation*

Cyclone IV GX PCIe hard IP block features include:

- PCIe Gen1 performance
- x1, x2, x4 lane support
- Endpoint and rootport functionality

Cost savings of the Altera® PCIe hard IP block include:

- No IP core purchase is required (TCO cost savings)
- More functionality than any other hard IP block implementation in a low-cost FPGA
- No FPGA logic is used so a smaller and cheaper FPGA can be used (BOM cost savings) (*Figure 7*)
Embedded Controller

Because Moore’s law (the doubling of transistors density every two years) applies to FPGAs, Cyclone IV FPGAs can integrate more functions than ever before. How can increased FPGA integration provide cost savings to another common application, the embedded controller-based product? Figure 8 shows an older external microcontroller-based system that also contains an FPGA. Over the last several years, the purchasing department has negotiated lower prices for the all the components on this product’s BOM. Soon, price negotiations will be ineffective at providing significant cost reductions. One alternative for getting additional and significant cost reductions is to redesign the product, while maintaining the same or similar functionality.

Low-cost FPGAs have lots of available logic capacity at low prices. Designers can use Altera’s Nios® II 32-bit soft IP processor for control-plane applications, use the embedded 18x18 multipliers for executing massively parallel DSP or compute-intensive algorithms, and incorporate external transceivers, SERDES, or PHY ASSPs. Fewer external power supplies are needed because there are fewer components on the board, and because the Cyclone IV FPGA requires fewer power supplies as compared to prior generations and competing FPGAs. All of these features reduce the BOM cost. The lower number of components also results in a reduced PCB size or reduced layer count, both of which decrease the board costs.
Because the redesigned product has fewer components and lower total power, the system reliability is improved. Because the of the higher system reliability, money spent on servicing equipment in the field is reduced (lower field maintenance costs = TCO cost savings).

**Video Capture Card**

This final example, a video capture card, shows how today’s FPGA features match the industry trend to offer more video content at a higher resolution. Many CPUs, GPUs, and ASSPs[1](2) have standardized on PCIe to facilitate the flow of high bandwidth video content within electronic systems. Altera’s FPGA families offer several variants of the PCIe hard IP block. Figure 9 uses the Cyclone IV GX variant PCIe hard IP block, which results in up to 30% system cost savings.

![Figure 9. Up to 30% System Cost Savings for Broadcast Equipment Video Capture Card](image)

Cost savings for this example include:

- The cost of the external PCIe ASSP is now zero because it is integrated into the FPGA (BOM cost reduction).
- Several other ASSP device costs are reduced. For example, the equalizer and receiver ASSP is replaced by a lower cost Equalizer-only ASSP (BOM cost reduction).
- With smaller and fewer components, the PCB area and layer count are less, lowering the PCB cost (board cost reduction).
- Because Cyclone IV FPGAs require fewer power supplies, costs are reduced two-fold:
  - Fewer regulators to pay for (lower BOM cost).
  - Fewer regulators result in lower board costs, because fewer power supplies and the associated filter circuitry occupy a smaller, less complex PCB implementation.
- Use of the FPGA PCIe hard IP block frees up almost 15K logic elements (LEs), so a smaller density, cheaper FPGA can be used (BOM cost reduction).
- No need to purchase the PCIe soft IP core license (TCO cost reduction).
FPGAs Reduce Total Cost of Ownership

Some OEMs market their products using lower power, reliability, and flexibility as selling features. Mid- and upper-level managers are quickly discovering how a FPGA-based product development can lower the TCO of a product throughout the entire life cycle. Here are some advantages Altera FPGAs provide over ASIC and ASSPs, all of which help to reduce the TCO:

- FPGA-based development cuts weeks or months off design schedules (3), allowing designers greater flexibility and faster time to market at reasonable prices.
  - Faster time-to-market saves R&D dollars (4)
- Faster redesigns of existing “successful” products for aggressive cost reductions allow manufacturers to protect profits from declining as a result of copy-cat product introductions, to keep pace with rapid market changes, and to accommodate special customer requests for new functionality.
- Leveraging many customers using a single “standard” product in turn drives higher overall volumes and a stable revenue stream with a longer life expectancy.
- Lower power consumption lessens the reliance on mechanical components (e.g., fans and active cooling) further increasing system reliability.
- Remote updates support equipment already deployed with customers.
- Shorter BOM simplifies component inventory management.

Conclusion

As demonstrated in these five examples and the subsequent TCO discussion, Altera® FPGAs provide ample evidence for lowering total system costs by reducing BOM costs, board costs, and TCO.

Design professionals looking to align with corporate objectives (increasing profits and sales revenue while simultaneously trying to utilize R&D efficiently) should investigate adopting a FPGA-based design philosophy to meet the resulting system level challenges. Altera’s Cyclone IV FPGAs (E and GX variants) include the latest cost-saving features, such as integrated hard IP blocks, 3G I/Os, and two power supplies, thereby meeting the requirements of a large variety of end applications.
Further Information

1. PCI-SIG integrators list:
   www.pcisig.com/developers/compliance_program/integrators_list/pcie
2. Nvidia video:
   www.nvidia.com/object/IO_15195.html
3. HardCopy® System Development Methodology:
4. Military Productivity Factors in Large FPGA Designs:
5. Cyclone IV Literature (handbook, white papers, etc.):
   www.altera.com/literature/lit-cyclone-iv.jsp
6. Free Quartus II Web Edition design software:
7. Training classes:
   www.altera.com/education/training/trn-index.jsp

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