White Paper

Enabling Ethernet-Over-NG-SONET/SDH Solutions for MSPP Linecards

The combination of Altera's Arria II GX family and TPACK's 2.5-Gbps/10-Gbps Ethernet-over-SONET/SDH and 10-Gbps/20-Gbps switch/NPU solutions meet the requirements of next-generation MSPP linecards and maintain existing infrastructure.

Introduction

Traditionally, the development of application-specific chip products such as ASSPs is based on foundry manufacturing, either in-house or via commercial foundries. FPGAs also are based on this manufacturing process, but due to their broader and more generic application, the production volume that FPGAs attain justifies investment in the latest manufacturing processes and technology. In turn, this benefits the designer with lower power consumption and greater integration resulting in a lower cost per logic unit.

One company taking advantage of the power, cost, and integration benefits of FPGAs is TPACK. TPACK provides application-specific chip products based on FPGAs. This approach, called SOFTSILICON, uses the latest generation of Altera® FPGAs to provide efficient packet-processing, traffic-management, and packet-mapping chip solutions to telecom system vendors.

This white paper shows how TPACK uses Altera's Arria® II GX FPGAs to offer new SOFTSILICON products for carrier-Ethernet-transport and packet-transport applications. Designed for cost-sensitive applications, Arria II GX FPGAs are the lowest power FPGAs with up to 3.75-Gbps transceivers. This allows TPACK to deliver solutions superior to traditional ASSP products in terms of power, cost, and features.

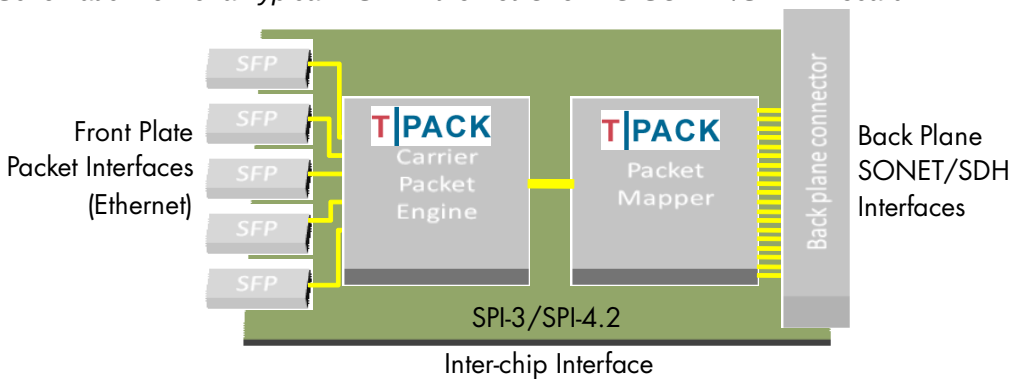
The Ethernet-Over-NG-SONET/SDH MSPP Market

Packet transport, and carrier-Ethernet transport in particular, can be achieved in a number of ways. One of the most widely deployed systems for packet transport is the trusted workhorse of voice networks, namely SONET/SDH multi-service provisioning platforms (MSPPs). An Ethernet-over-NG-SONET/SDH linecard in an existing MSPP allows incoming Ethernet packets to be mapped efficiently to SONET or SDH using a standard mapping mechanism, such as Generic Framing Procedure (GFP), Virtual Concatenation (VCAT), and Link Capacity Adjustment Scheme (LCAS).

Because Ethernet-over-NG-SONET/SDH is a mature technology, all of major telecom system vendors have developed MSPP carrier-Ethernet-transport linecards and deployed them over the last five years. These modules are based on packet-mapper ASSP chip devices from companies like AMCC, Vitesse, PMC-Sierra, and Infineon using 130- or 90-nm semiconductor manufacturing technology. TPACK also provides Ethernet-over-NG-SONET/SDH modules, the SOFTSILICON products based on Altera Stratix®, Stratix II, and Stratix III FPGAs, to this market.

Figure 1 shows an outline of a typical MSPP carrier-Ethernet linecard. The card has two major functional components: a carrier packet engine and an Ethernet-over-NG-SONET/SDH packet mapper. The carrier packet engine, such as the TPACK TPX3103, is a packet processor and traffic manager. The packet mapper, like the TPACK TPW48, maps packets into SONET/SDH timeslots via GFP, VCAT, and LCAS.

Figure 1. Schematic View of a Typical MSPP Ethernet-Over-NG-SONET/SDH Linecard



The overall trend in packet-transport networks is to migrate from existing SONET/SDH towards an all-packet-based network. Because most of today's data traffic is packet based, it would be most cost-effective to transport it over a packet-optimized network. However, this transition is expected to take 10 to 20 years. In today's financial situation, telecoms are even more likely to further extend the life of the existing SONET/SDH infrastructure rather than invest in a completely new network. This means that many equipment vendors are considering redesigning existing MSPP systems and carrier-Ethernet linecards that were previously scheduled to be in maintenance mode. Lowering the cost and power consumption of these modules will assist carriers in extending the cost-effective life of the infrastructure.

Since MSPPs and carrier-Ethernet linecards were expected to be in maintenance mode at this time, the ASSP vendors have already abandoned this market segment and have not invested in new designs. This is compounded by the fact that a large investment is required for 65-nm and even 40-nm designs, with a long and limited return on investment. Altera's Arria II GX architecture allows TPACK to benefit from the process and architectural improvements of prior-generation products and thereby directly address current system vendor and telecom needs in a much more economically sound way.

Addressing Cost-Sensitive Telecom Applications

Arria II GX FPGAs are based on a 40-nm, full-featured FPGA architecture that provides the optimal logic and memory capabilities while also integrating up to 16 transceivers that support data rates from 600 Mbps to 3.75 Gbps. These devices are optimized for cost- and power-sensitive telecom applications, such as Ethernet over SONET/SDH.

Arria II GX FPGAs with transceivers are optimized for cost and power, and support standard, emerging, and proprietary serial protocols up to 3.75 Gbps. The Arria II GX FPGAs include a number of features that ensure excellent jitter performance combined with superior signal integrity for both backplane and chip-to-chip applications. Many telecom applications require flexible support of a variety of front-end protocols (Ethernet, SONET/SDH), and the dynamic reconfiguration of the transceiver enables the support of multiple protocols and data rates on the same channel without reprogramming the FPGA. Table 1 shows some of the telecom protocols supported with Arria II GX FPGAs.

Table 1. Relevant Telecom Protocols Supported With Arria II GX FPGAs

Standards	Data Rate in Gbps
PCI Express (PCIe) Gen1	2.5
SGMII	1.25
Gigabit Ethernet (GbE)	1.25
10G Ethernet (XAUI)	3.125
GPON	1.244 uplink, 2.488 downlink
HiGig+	3.75
SONET OC-3/OC-12/OC-48	0.155, 0.622, 2.488
SPAUI	3.125

Arria II GX FPGAs also deliver the lowest power of any FPGA with up to 3.75-Gbps transceivers. The 0.9V core voltage on Arria II GX FPGAs provides significant power savings over competitive technologies. Architectural optimizations on the Arria II GX FPGAs, including the multi-threshold transistors, variable gate-length transistors, low-k dielectric, triple-gate oxide, super-thin gate oxide, and strained silicon, further contribute to lower power consumption. The devices are designed to deliver the correct performance for 3.75-Gbps transceiver applications while consuming less power. Even the largest Arria II GX FPGA consumes only between 5 to 8W of total power, which is easily dissipated, removing the need for expensive thermal management techniques.

Ethernet-Over-NG-SONET/SDH Packet Mappers

Of the popular Ethernet over NG-SONET/SDH packet-mapper products (Table 2), TPACK's SOFTSILICON products based on Arria II GX FPGAs are the only devices based on 40-nm technology. This enables TPACK to offer both dramatic power and cost advantages relative to ASSP devices. For example, although PMC-Sierra's PM5397 consumes lower power, it does not support critical features such as virtual concatenation of low-order (LO) SONET/SDH timeslots like VC-12/VC-11. Where other ASSPs do support LO mapping, they do not support new standards created after their development. In contrast, TPACK supports the International Telecommunications Union (ITU)'s standard for virtual concatenation of PDH channels, an important solution for mobile backhauling and central-office handoffs. New standards and customer-specific features also are supported by extending the SOFTSILICON solution. Since FPGAs are reprogrammable, this is achieved quickly and efficiently, and allows upgrading of field-deployed units.

Table 2. Comparison of Key Ethernet Over NG-SONET/SDH Packet Mapper Products (1)

Vendor	Product	Type	Capacity	40-nm Technology	Power	LO Mapping	VCAT of PDH Channels	Introduced
PMC-Sierra	PM5397	ASSP	2.5G	No	4W	No	No	2001
Vitesse	VCS9135	ASSP	2.5G	No	9W	Yes	No	2005
TPACK	TPW48	SOFTSILICON	2.5G	Yes	4.5W	Yes	Yes	2009
Vitesse	VCS9138	ASSP	10G	No	11W	Yes	No	2005
TPACK	TPW192	SOFTSILICON	10G	Yes	10W	Yes	No	2009

Note:
(1) Based on public information

Carrier Packet Engines

The carrier-packet engine of the Ethernet-over-NG-SONET/SDH linecard shown on Figure 1 is typically performed by an ASIC, an ASSP, a network-processing unit (NPU), or an FPGA device. Carrier-packet engines combine packet processing and traffic management and may need to support a broad range of packet protocols, such as Carrier Ethernet, IP/MPLS, VPLS/PWE3, PBB-TE/PBT, and MPLS-TP. Table 3 lists some of the most popular carrier packet engines for 20G switching capacities.

Table 3. Comparison of 20G Carrier Packet Engine Solutions (1)

Vendor	Product	Type	Capacity	Technology	Power	Traffic Manager	Introduced
EZchip	NP2	NPU	20G	130 nm	15-18W	Yes	2004
Xelerated	X11	NPU	20G	130 nm	9-19W	No	2004
TPACK	TPX3104	SOFTSILICON	20G	40 nm	8W	Yes	2009

Note:
(1) Based on public information

Comparing carrier packet engines requires deep analysis of both packet processing and traffic manager features. Xelerated's X11 does not have an integrated traffic manager, so a comparable system would need an additional device on the board leading to higher cost and power. In contrast, TPACK's TPX3100 does have a traffic manager and is implemented in an Arria II GX FPGA, which results in 50 percent lower power and compelling cost advantages.

While EZchip's NP2 also has an integrated traffic manager, its functionality is fixed in silicon. Again, because TPACK's TPX3100 is based on reprogrammable FPGAs, it supports the dynamic requirements of traffic management.

Conclusion

The transport of packets over existing SONET/SDH infrastructure is a resilient solution that will last for many years to come. However, ensuring that existing systems support the latest protocols and features, while meeting lower capital expenses, operating expenses, and power consumption targets requires a new type of solution. By leveraging the latest generation of Arria II GX FPGAs, TPACK has developed Ethernet over NG-SONET/SDH solutions that support the latest protocols and features at a cost point and power-consumption level that should prove attractive to MSPP system vendors and their telecom customers.

Further Information

- TPACK:
  www.tpack.com
- *40-nm FPGA Power Management and Advantages*:
  www.altera.com/literature/wp/wp-01059-stratix-iv-40nm-power-management.pdf

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101 Innovation Drive
San Jose, CA 95134
www.altera.com