White Paper

Generating Functionally Equivalent FPGAs and ASICs With a Single Set of RTL and Synthesis/Timing Constraints

Electronic systems designers use FPGAs for their prototype implementations, taking advantage of the devices' reprogrammability to validate hardware and software. Once the design is ready for volume production, designers are finding that certain types of ASICs—specifically, ASICs with a silicon platform and toolset that enable concurrent design with the FPGA, using identical I/Os, memory resources, and IP—help them meet power, performance, and cost targets. With these criteria, the designer can lower the risk of generating an ASIC-based design containing functional or timing errors. This paper discusses the evolution, architecture, and capabilities of Altera HardCopy ASICs as a package- and pin-compatible FPGA counterpart that is ideal for taking designs into volume production.

Introduction

Altera first introduced the 180-nm CMOS-technology HardCopy® series of ASICs, with their "seamless prototyping" capabilities, in 2001. The premise behind this first-generation HardCopy ASIC product was to "harden" the look-up table (LUT) structure of the FPGA and replace the programmable switch fabric with a direct wire (ASIC) interconnect using a small number of customized interconnect layers. Other blocks of "hardened" logic in the FPGA prototype, including I/Os, phase-locked loops (PLLs), memories, and serializer/deserializer (SERDES) channels, are used verbatim in the HardCopy ASIC. Since the introduction of that first-generation device, Altera has offered subsequent HardCopy ASIC products in 130-nm, 90-nm, and 40-nm CMOS technology. The HardCopy ASIC has attributes similar to gate array technology in that common partially fabricated "bases" are staged in inventory. The tape-out of a specific design results in a two-metal/two-via set of masks of custom metallization layers that define a unique device. The base wafer is then processed with custom metal masks, and tested and assembled in a package that is 100 percent socket-compatible and based on the same silicon process as the FPGA prototype.

This new HardCopy ASIC results in lower NRE costs versus comparable standard-cell implementations, and reduces the time to fabricate the ASIC since base wafers are pre-staged up to the custom interconnect wafer processing steps. The HardCopy ASIC is feature-equivalent to the corresponding Altera® Stratix® series FPGA, and offers comparable resources as the FPGA but with reduced die size and power. The final HardCopy ASIC is a pin-for-pin replacement of the FPGA prototype; therefore, the same system board and software can be retained between prototyping/field trials and the final production device. Additional overall board savings can be realized by using the HardCopy ASIC for production, since it requires no boot device. The flash memory boot device does not need to be mounted on the HardCopy version of the board.

HardCopy ASIC Families

Table 1 shows how HardCopy ASICs have followed Moore's law of device complexity over three production and two new generations of devices. Architectural advancements and improvements include an overhaul of the logic implementation in the 90-nm third generation of the HardCopy ASIC that improves density, power, and performance. 40-nm HardCopy ASICs include up to 11.5M equivalent ASIC gates, 20.3 Mbits internal RAM, 36 SERDES channels, and 736 I/Os. These HardCopy III and HardCopy IV ASICs are assembled in a variety of packages, starting with cost-optimized 484 wirebond packages up to 1,517-pin flip-chip packages with internal decoupling capacitors. Core frequencies can run upwards of 400 MHz, and SERDES operation exceeds 6.5 Gbps.

Table 1. Five Generations of HardCopy ASICs

Device	Technology Node	Usable Gates	Internal Memory	I/Os	SERDES Channels
HardCopy APEX™ 20KE	180 nm	622K	442 Kbits	808	-
HardCopy Stratix	130 nm	1.82M	5.65 Mbits	773	-
HardCopy II	90 nm	3.6M	8.8 Mbits	951	-
HardCopy III	40 nm	6.9M	16.3 Mbits	880	-
HardCopy IV GX	40 nm	11.5M	20.3 Mbits	736	36 channels

WP-01095-1.2

HardCopy Power Consumption

An important feature of the HardCopy architecture is power reduction from the FPGA prototype. Because the HardCopy ASIC has an array/direct-wire architecture which substantially reduces the transistor count required to implement the logic, there's much less power consumption compared to a LUT/switch-fabric architecture. HardCopy ASICs also do not need the large amount of internal configuration RAM space required for FPGA reprogramming. Because the HardCopy ASIC is used for only a single function, the resources in the base device that require power are connected to the power distribution network while unused devices are not connected to this network. On average, HardCopy ASICs provide a 50 percent reduction in power over their corresponding FPGA prototypes. The actual power reduction from FPGA prototype to HardCopy ASIC depends on the ratio of logic used versus other resources, such as internal memories or I/Os, which do not reduce power at the same ratio as the FPGA prototype.

HardCopy Performance

The array/direct wire structure of the HardCopy ASIC does not require the transistor overhead of LUT/switch fabric architectures of FPGAs. This circuit simplification improves performance for core logic timing critical paths. The HardCopy design methodology allows for separate timing constraints for both the FPGA and the HardCopy ASIC, maintaining logic equivalence while allowing the designer to take advantage of the improved performance of the HardCopy architecture. In one instance, a 90-nm FPGA project with peak frequency of 280 MHz achieved 432-MHz operation in the HardCopy fabric. Table 2 shows additional examples.

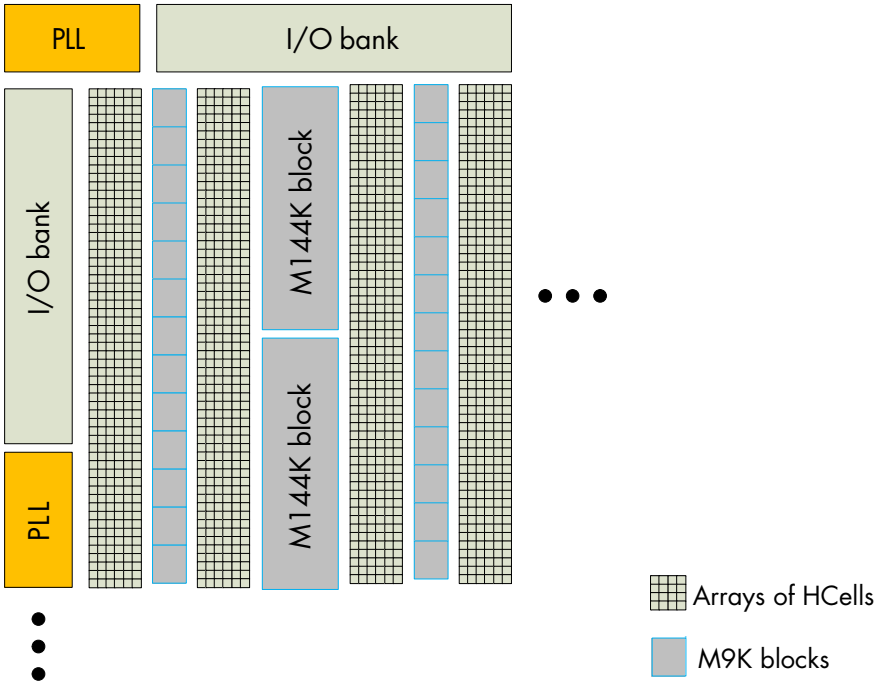
Table 2. Examples of Improved Performance Using HardCopy ASICs

Project	90-nm FPGA	90-nm HardCopy ASIC
A	150 MHz	234 MHz
B	175 MHz	325 MHz
C	280 MHz	432 MHz
D	125 MHz	250 MHz

HardCopy ASIC Architecture

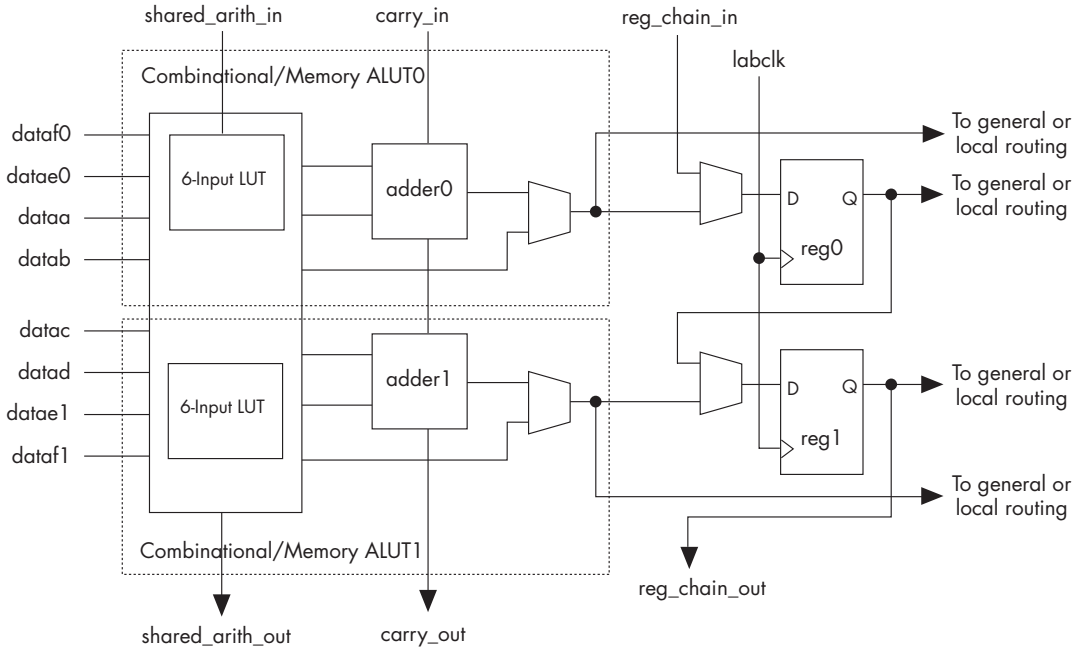
At 40 nm, the HardCopy III and HardCopy IV architecture uses a logic array cell called an HCell, which consists of 24 transistors. One to six HCells are tiled together to form HCell macros (HCMs), which are logic functions used to replace the LUT structure of the corresponding Stratix series FPGA prototype. The construction of logic using HCells allows flexible functionality such that when HCells are combined into HCMs and wire connections, all viable combinations of the corresponding FPGA's function are replicated. Other resources in the 40-nm HardCopy base device are memories, I/O elements (IOEs), PLLs, delay-locked loops (DLLs), and SERDES channels. Internal memories in 40-nm HardCopy ASICs are comprised of 9-Kbit, 144-Kbit, and 640-bit register array (MLAB) memories. The M9K and M144K blocks in HardCopy ASICs are nearly identical to their corresponding Stratix FPGA prototype, with the exception that configuration memory bits are replaced with via programming. The 640-bit register array (MLAB) cell built from LUTs in the FPGA are replaced with MLABs built from HCells. Figure 1 shows an example floorplan of the 40-nm HardCopy III ASIC.

Figure 1. Example Block Diagram of HardCopy III ASIC



The basis of Altera's FPGA LUT function is called an adaptive logic module (ALM). As illustrated in Figure 2, each ALM contains a variety of LUT-based resources that can be divided between two combinational adaptive LUTs and two registers. With up to eight inputs to the two combinational ALUTs, one ALM can implement various combinations of two functions. One ALM can implement any function up to six inputs and certain seven-input functions. The flexibility of the ALM structure improves the overall efficiency and utilization of the Stratix series of FPGAs.

Figure 2. ALM



The 24-transistor patented HCell was chosen as the basis for the HardCopy architecture because it provides the ideal mix of density and ability to customize the desired logic function with a minimal number of configurable metal and via layers. An individual HCell consists of six functions (Figure 3): two 2-to-1 multiplexers, two 2-input NAND gates, and two inverters. For every possible configuration mode of the LUT (ALM), there is a one-to-one corresponding mapping to a collection of HCMs (Figure 4), which are, in turn, a collection of one to six HCells. The connections between functions within the HCell are programmable through a customized via layer.

Figure 3. Functions Included in the HCell

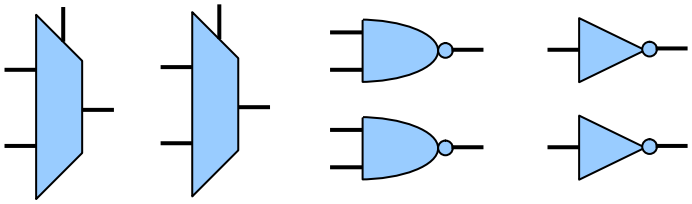
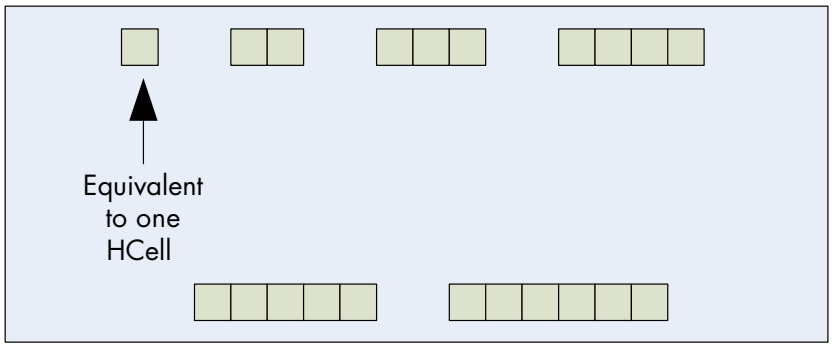
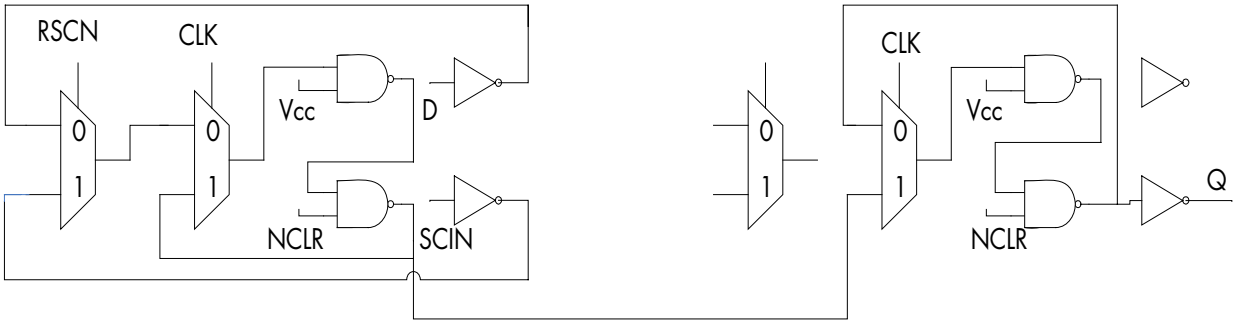


Figure 4. HCells Combine to Form HCMs of Varying Sizes



The functions included in the HCell combine to create numerous combinational and register functions. As an example, consider a scan register built from two HCells as shown in Figure 5. The multiplexers are configured as master/slave latches and the NAND gates and inverters are used for applying the asynchronous clear and buffering. This example of a scan register with clear is one of thousands of configurations realizable with the HCell architecture.

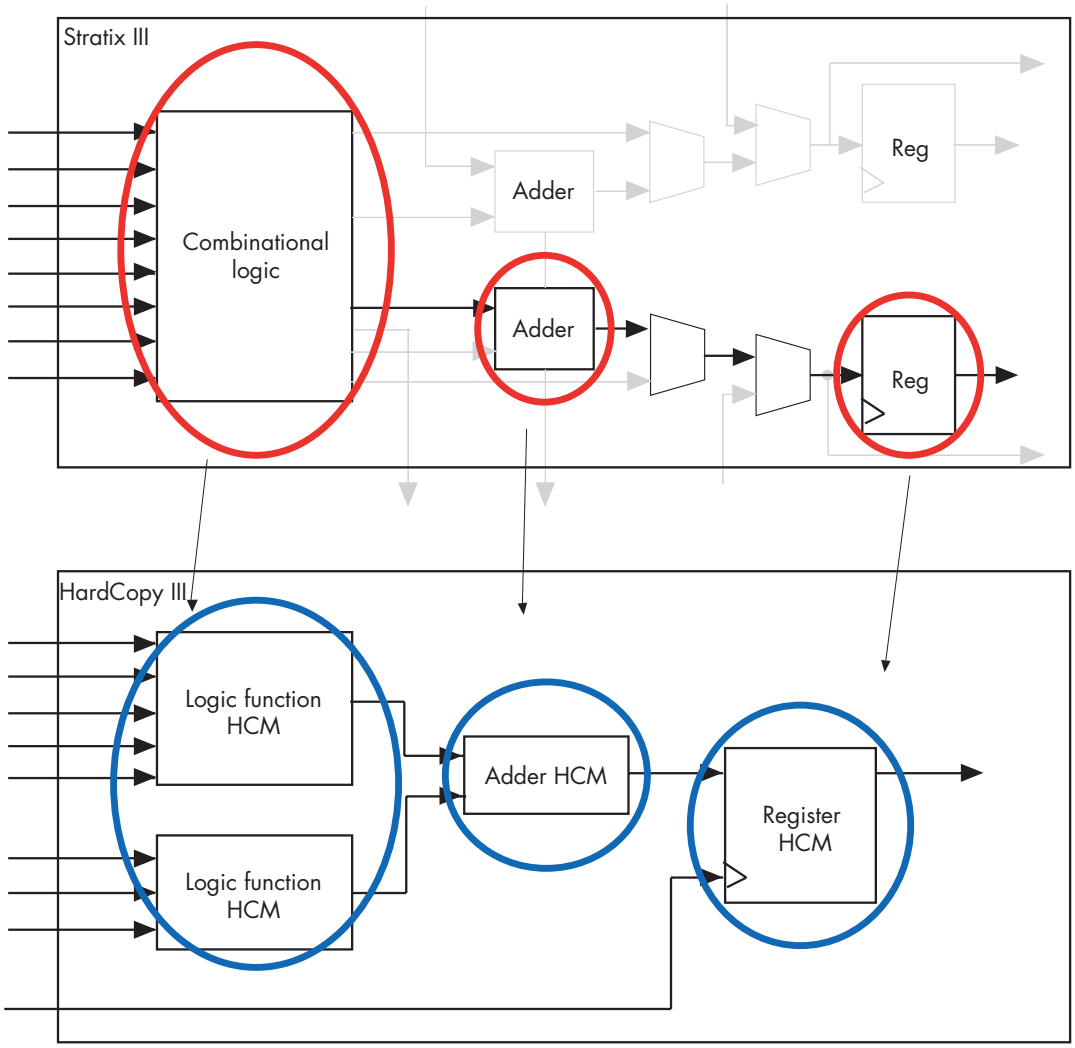
Figure 5. 2 HCells Configured to Form Register With Scan and Reset



Altera's Quartus® II design software, used for synthesis and fitting of the FPGA, is also used for mapping the ALM function to HCells, creating the HardCopy netlist representation of the design, and for placement and global routing of the HardCopy ASIC. It is important to note that the mapping of ALMs to HCells is a one-to-one mapping function and does not require resynthesis of the register transfer level (RTL). This significantly lowers the risk of errors in design translation from FPGA to ASIC. Figure 6 shows how a specific function implemented in ALMs is mapped to HCMs. The one-to-one mapping step (as opposed to RTL resynthesis in traditional FPGA to standard-cell ASIC

implementation flows) creates a HardCopy design database with instance and net names that are recognizable by the designer and can be constrained with a common timing constraint file, streamlining analysis of design and timing reports between the FPGA and ASIC implementations.

Figure 6. Example of ALM Functions Mapped to HCMs



FPGAs contain other building blocks besides ALMs: memories, PLLs, SERDES channels, I/O banks, and digital signal processing (DSP) blocks. The DSP functional block consists of eight 18-bit x 18-bit multipliers plus two accumulators with various configuration options for pipelining, signing, rounding and saturation. 40-nm HardCopy ASICs do not contain these dedicated DSP blocks as the FPGA does, since this resource may or may not be used. Instead, the HardCopy ASIC replicates the DSP functionality with DSP macros with equivalent functionality of the FPGA prototype built from HCells.

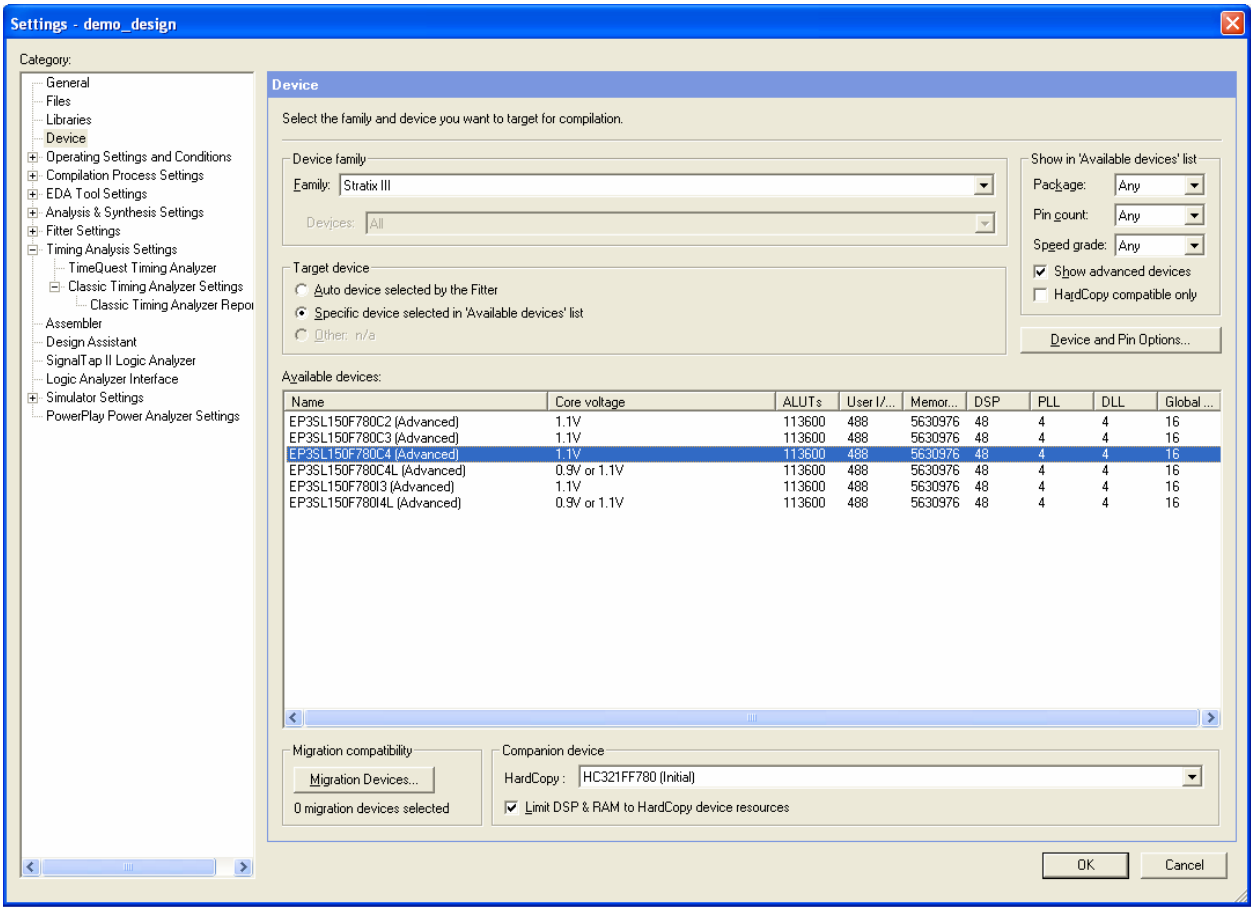
Front-End Design Flow

The front-end design flow for HardCopy ASICs utilizes the same steps required for the FPGA prototype development plus compilation of the companion HardCopy database. Altera's Quartus II toolset is used for both FPGA and HardCopy design, and serves as a common platform for designers to simultaneously design FPGAs and HardCopy ASICs. Quartus II software has numerous features, including:

- RTL synthesis
- Package pinout definition
- Fitting (placement and routing for both FPGAs and ASICs)
- Timing analysis and closure based on Synopsys Design Constraints (SDC) (an industry-standard timing constraint format) specifications for both FPGAs and HardCopy ASICs
- Simulator (a version of ModelSim® VHDL or Verilog simulator is included)
- Intellectual property (IP) generation for numerous blocks (internal memories, PLLs, I/O interfaces such as DDR and PCI, external memory interfaces, embedded soft processor and associated peripherals, DSP functions, and many more)
- RTL code review that analyzes the design for ASIC-compatible clocking and reset structures

Some mappings from FPGA to HardCopy ASIC utilize 100 percent resource compatibility. In other cases, the resources of the FPGA exceed those that are available in the HardCopy base device (in order to optimize the HardCopy cost structure). To ensure project success, pair the FPGA and HardCopy ASIC from the onset of the FPGA design so that design resources and pins common to both design implementations are compatible. This ensures delivery of a 100 percent socket-replacement HardCopy ASIC that can be quickly verified and qualified for production in the existing FPGA prototype PC board. During the device selection process, the designer selects the FPGA and HardCopy ASICs as a pair, as shown in Figure 7.

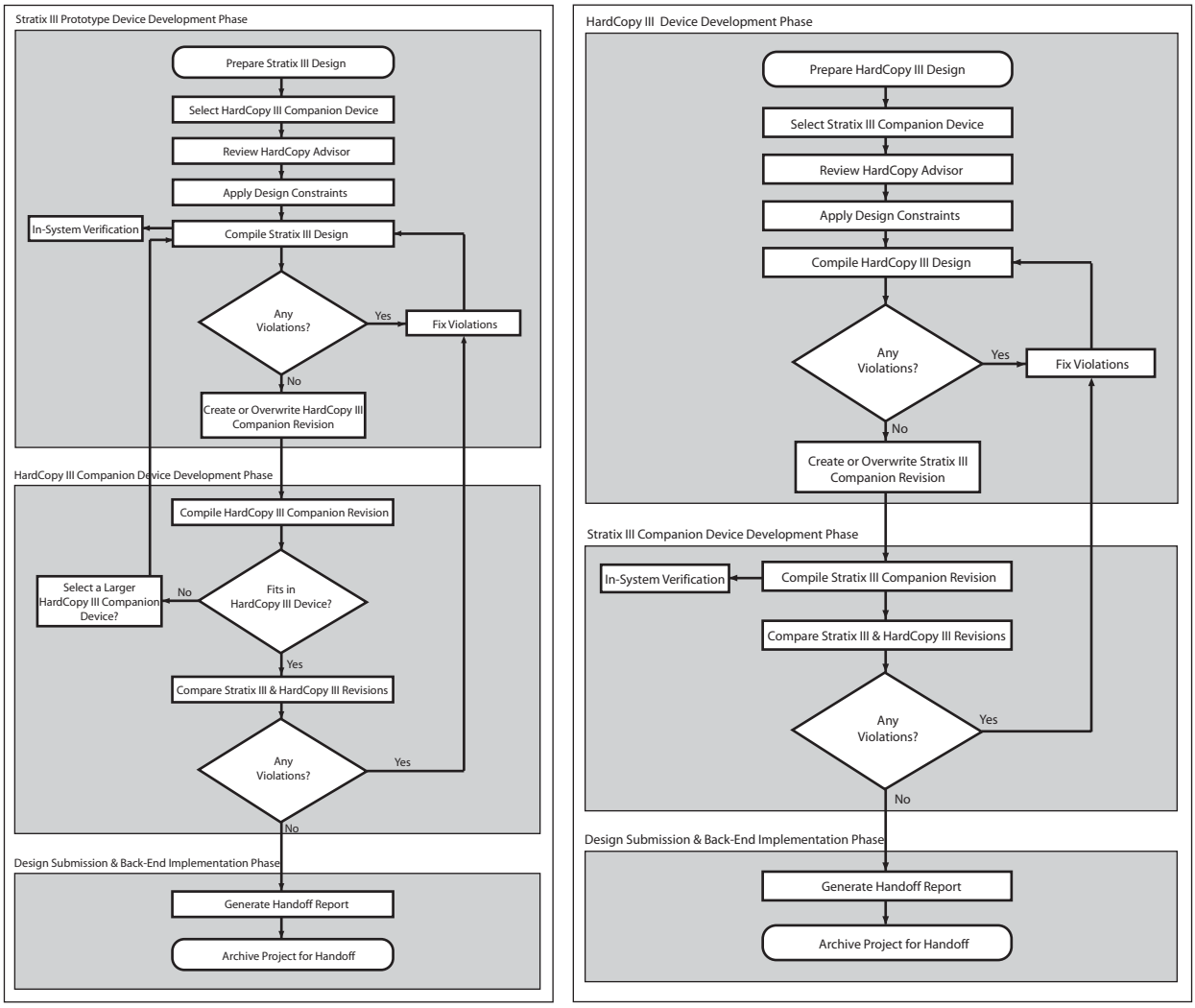
Figure 7. Selection of the FPGA/HardCopy ASIC Pair in Quartus II Software



After selecting the FPGA/HardCopy ASIC pair, the designer has the option of first synthesizing and fitting the FPGA or the HardCopy ASIC (see Figure 8). Although the FPGA will be validated in system first, the “HardCopy first”

flow allows the designer to concentrate on iterating through synthesis and timing closure of the HardCopy device for maximum timing performance from the HardCopy ASIC. During various design checkpoints, or once HardCopy timing targets are met, the designer can then target the FPGA for a slower speed prototyping device.

Figure 8. Comparison of FPGA-First Flow (left) vs. HardCopy ASIC-First Flow (right)



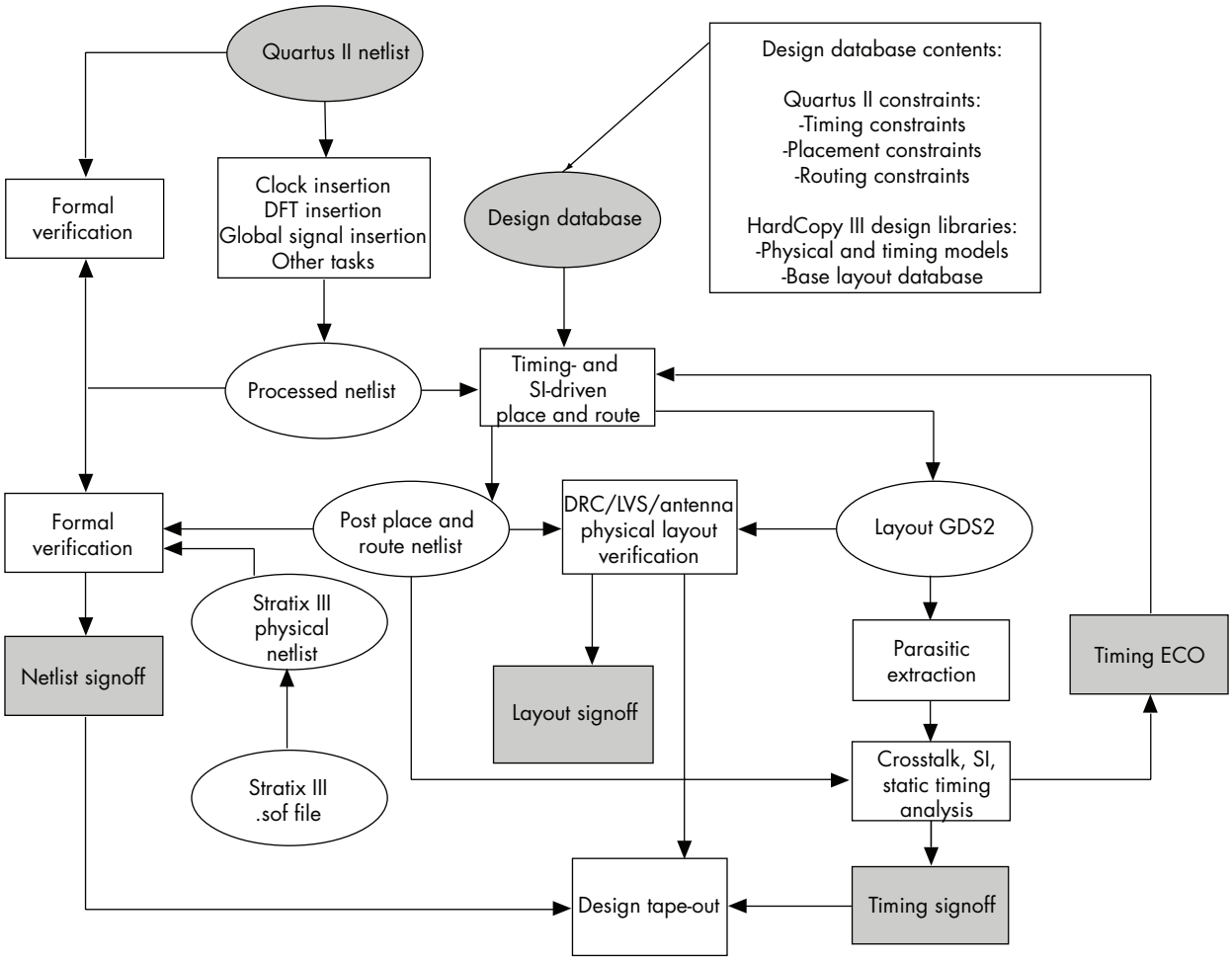
Quartus II software has an internal formal verification mechanism to ensure that the RTL source code for the FPGA and HardCopy databases is identical. A database containing a single set of source code is the basis of two compilation revisions. The Compare HardCopy Companion Revision feature in Quartus II software assures that the functionality and compilation settings match between the FPGA and HardCopy ASIC and remain unchanged. This comparison feature must run error-free prior to submission to the HardCopy Design Center for back-end processing.

Back-End Design Flow

The back-end design flow from netlist/constraint handoff through custom-layer tape-out is executed as a turnkey development at Altera's HardCopy Design Center. The front-end designer runs the Quartus II tool, which generates a HardCopy HCell-targeted Verilog gate-level netlist, placement constraints, and global route guides that are included in the design database handoff. The designer and the HardCopy Design Center participate in a series of reviews to ensure that the design meets final handoff criteria.

As shown in Figure 9, the back-end flow utilizes many of the same steps that are used for standard-cell ASIC designs, using commercial EDA tools from Synopsys and Cadence. Because the HardCopy back-end design process is implemented numerous times on the exact same base die, common steps are automated and predictable, as differences from design to design are only variations in resource counts, not base dies redesigned from the ground up. Standard-cell implementation steps such as power mesh design and current/resistance (IR) drop analysis, electrostatic discharge (ESD) cell placement and analysis, power segment cuts, and balance and tuning of clock networks are pre-built into the base die; as such, they are not needed for each HardCopy back-end implementation. This improves the HardCopy ASIC's back-end turnaround time to a predictable four to six weeks, making each tape-out more predictable and lower in risk.

Figure 9. HardCopy Backend Flow



Testing

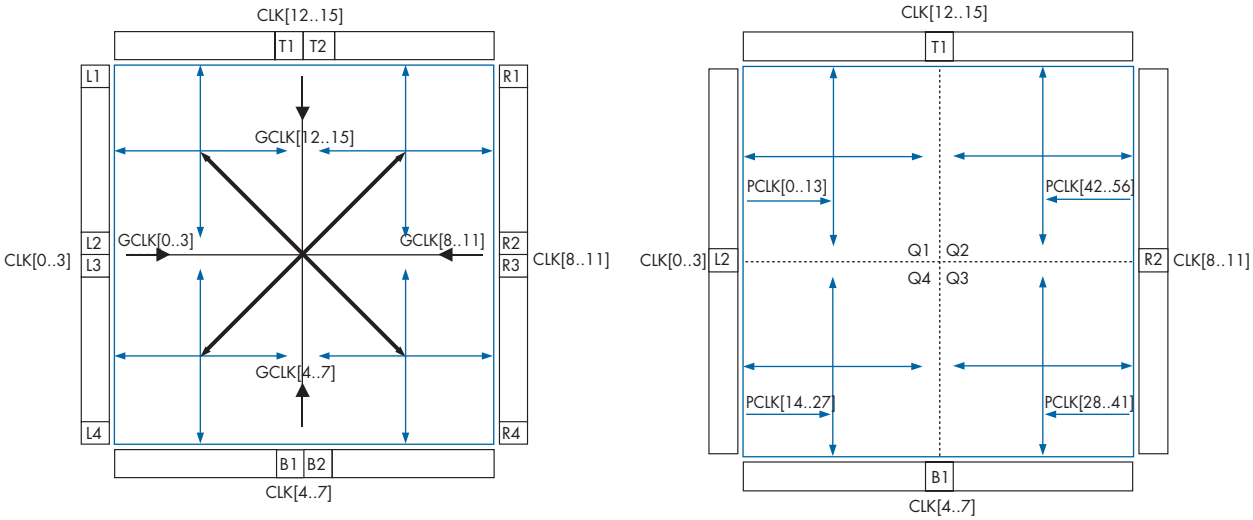
The HardCopy Design Center starts the back-end process by inserting the necessary test structures into the Verilog gate-level netlist. Test structures include full-scan capable registers and associated scan chains, JTAG, PLL built-in self test (BIST), SERDES BIST, and memory testing. The FPGA/HardCopy front-end designer should not be concerned with instantiating test structures or test design preparation strategies commonly required of standard-cell designs. For instance, controlling resets from an external I/O pin or functional/test I/O pin sharing are not required. Test logic, inserted in the back-end flow, is transparent to the designer.

The HardCopy ASIC uses the scan chains for both full scan and delay fault testing. Memories are tested at speed using 47N march patterns and include fuse programmable redundant rows and columns for yield enhancement. Analog, high-speed serial I/Os, PLLs, and DLLs are tested with BIST at chip operating frequency. Logic is tested with a combination of stuck-at-fault patterns and delay fault patterns. I/O buffer DC and AC behavior is tested using parametric patterns and the JTAG boundary scan registers. Design-independent speed paths using thin and thick oxide transistors are embedded in the HardCopy base to ensure that the device functions in the allowable silicon process window. Wafers are tested at room temperature and packaged parts at room temperature and 100°C to ensure proper screening for early life defects. Test coverage is consistently over 98 percent for all commonly measured deep submicron CMOS silicon failure modes.

Clocking

The pre-built clock structures in the Stratix FPGAs and HardCopy ASICs use a common architecture of pre-built clocks. Clocks in both devices are pre-built networks that exhibit minimal skew since the number of metal layers traversed from the clock root to every endpoint is balanced and shielded from crosstalk effects. There are three categories of pre-built clocks in HardCopy silicon: global (Figure 10, left), regional (Figure 10, right), and periphery clocks. Clocks are organized in a hierarchical structure that offers up to 220 unique clock domains: (16 GCLK + 88 RCLK + 116 PCLK).

Figure 10. 16 Global Clock Networks (left) and 88 Regional Clock Networks (right) Span the Entire Chip



The Quartus II compiler defines the assignment of pre-built clock networks; however, the designer can re-assign clock resources as desired to meet specific design objectives. There are a couple of differences between the FPGA clock and the HardCopy clock networks. Since the HardCopy ASIC is considerably smaller than its FPGA prototype, the clock network has less insertion delay. If a PLL is used, this insertion delay is compensated out; however, if the clock is directly applied from an input pad, then the timing will be different. The HardCopy ASIC requires thorough timing constraints, so even though micro-timing within the device is different, the timing constraints make sure that the design is closed to system-level timing budgets.

The other difference in clock networks is in the final tributary branch of the clock that drives registers. With the HardCopy array of HCells, it is most optimal not to predefine where registers are placed or confined based on the clock network. When Quartus II software compiles the HardCopy database, it has free rein to place registers where it sees fit (within global, quadrant, or I/O boundaries). The HardCopy clock network is pre-built up to the final tributary branch. During the design back-end flow in the HardCopy Design Center, the final buffering stage and routing to actual register locations is completed using Synopsys Clock Tree Synthesis tools. This serves the dual purpose of allowing flexible register placement and implementing a low-skew clock network.

Formal Verification

Quartus II software includes a HardCopy revision comparison utility as a check to make sure that the same RTL code, I/Os, and timing assignments are used to compile both the FPGA and the HardCopy ASIC. This step ensures the integrity of the final handoff database. During back-end processing, a number of modifications are made to the netlist for test insertion and timing closure. These steps are not intended to modify the functionality of the design, and must be proven to ensure high confidence in the quality of the tape-out database. The Cadence Conformal equivalence checking software is used to create a Boolean model of both reference netlist and modified (test, buffering) netlist, and assures they are functionally equivalent. The most important step in formal verification is proof that the FPGA and final HardCopy tape-out netlist are indeed functionally equivalent. This step is accomplished by taking the FPGA physical netlist (the FPGA tape-out netlist, including the configuration RAM bits) and HardCopy tape-out netlist and running equivalence checks on the two databases. For this proof, the FPGA physical netlist is combined with the programming file (the ROM code which configures the SRAM-based FPGA) and compared to the HardCopy final tape-out netlist. Because memories, I/Os, PLLs, and other resources are constructed similarly in the two devices, the proof assures that settings are the same, and that LUT- and HCell-based logic implementations are mathematically equivalent. This proof is only possible in the HardCopy flow, since only Altera has the full understanding of the underlying structures that comprise both FPGAs and HardCopy ASICs.

Timing Closure

Core timing paths in the HardCopy ASIC can perform as much as 100 percent faster than their FPGA implementation. The LUT/switch fabric architecture requires considerably more levels of logic compared to the HardCopy array cell/direct wire architecture. The focus for most front-end designers is to first close FPGA timing, since FPGA timing closure requires considerably more effort than so with the HardCopy counterpart. In most cases, the HardCopy core timing is closed in the first pass of Quartus II compilation using default settings. Quartus II software translates the FPGA ALMs to HardCopy HCell equivalents, and runs a full placement and global route during its compile stage. This database is analyzed using Quartus II software's TimeQuest timing analyzer feature. Before handoff to Altera's design center, the design must be 100 percent constrained using SDC-style syntax with Altera's TimeQuest timing analyzer. In addition, all timing paths must exhibit positive timing slack. The FPGA and HardCopy ASIC are not intended to have equivalent slack on a path-for-path basis; the flow guarantees that timing constraints will be met (positive slack) for both implementations, which is quite different than path slack being identical for each timing path.

The HardCopy Design Center imports the HardCopy seed netlist, Quartus II software-generated placement, and SDC into the Synopsys back-end flow. If the timing needs to be adjusted in order to achieve positive slack, the HardCopy Design Center will run timing-closure techniques such as buffering, load splitting, hold-time-delay cell insertion, and PLL phase-shift adjustments to gain timing closure. Upon timing closure, the design center runs the HardCopy database through layout versus schematic (LVS) and design rule checks (DRC) to ensure the design physical layout database matches the netlist and that all foundry process design rules are followed. The final step prior to tape-out is a layer-by-layer comparison that ensures only the four custom layers are modified and other layers match the base silicon.

Conclusion

FPGAs are the technology of choice for many systems prototyping requirements. When FPGA technology does not meet cost, power, or performance targets, a design can be easily mapped to ASIC technology that is specifically developed as a FPGA companion. The HardCopy ASIC's unique architecture is constructed specifically to create a 100 percent functional match with Altera's Stratix series FPGAs. This goal is accomplished by adopting all FPGA resources except the LUTs and the programmable interconnect fabric into the HardCopy ASIC, while changing the logic implementation from LUT/switch fabric to an array cell/direct wire implementation. The new device is a socket replacement of the FPGA with identical functionality that meets common SDC timing constraints. The back-end flow process is performed turnkey, and ensures that functionality and timing are met, and testability features are incorporated in a well defined implementation and engagement process.

Further Information

- *HardCopy III Device Family Overview*: www.altera.com/literature/hb/hardcopy-iii/hiii51001.pdf
- Literature: HardCopy IV Devices: www.altera.com/products/devices/hardcopy-asics/hardcopy-iv/literature/hciv-literature.jsp
- Literature: HardCopy III Devices: www.altera.com/products/devices/hardcopy-asics/hardcopy-iii/literature/hc3-literature.jsp
- Literature: HardCopy II Devices: www.altera.com/products/devices/hardcopy-asics/hardcopy-ii/literature/hr2-literature.jsp

Acknowledgements

- Larry Landis, Senior HardCopy Project Manager, HardCopy Product Group, Altera Corporation

101 Innovation Drive
San Jose, CA 95134
www.altera.com