Understanding 40-nm FPGA Solutions for SATA/SAS

WP-01093-2.0 White Paper

This white paper describes the SATA and SAS protocols, how the protocols are used, explains the value SATA and SAS in terms of usage in an FPGA, and illustrates how Altera® FPGAs can be used to develop a SATA or SAS solution.

Introduction

Serial ATA (SATA) and Serial Attached SCSI (SAS) are computer bus standards that have the primary function of transferring data (directly or otherwise) between the motherboard and mass storage devices (such as hard disk drives, optical drives, and solid-state disks) inside and outside the computer. These serial storage protocols offer several advantages over older parallel storage protocols (ATA and SCSI) interfaces:

- Faster data transfer
- Ability to remove or add devices while operating (hot swapping) (only when supported by operating system)
- Thinner cables for more efficient air cooling
- More reliable operation

Cables and connectors for SATA and SAS are interchangeable to a certain extent, in that a SATA storage device, cable, and connector can be used by a SAS host controller, but a SAS storage device and connectors cannot be used by a SATA host controller. This flexibility enables system designers the option of designing for SAS, a higher performance and higher cost solution, but using SATA as a lower cost option. Several versions of the SATA and SAS standards have been released so far, with each version primarily addressing the speed of a single data link. Table 1 lists the released standards and their associated speeds.

Table 1. SATA/SAS Standards and Speeds

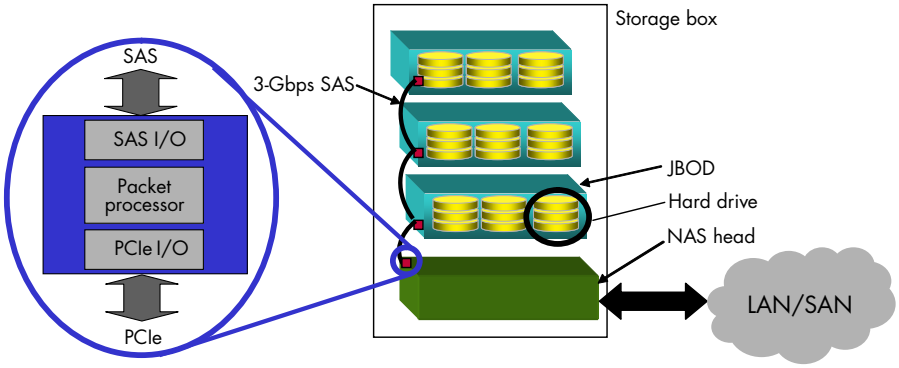
SATA/SAS Standards	Speeds
SATA 1.0	1.5 Gbps
SATA 2.0, SAS 1.0	3 Gbps
SATA 3.0, SAS 2.0	6 Gbps

Applications Using SAS and SATA

Because SATA and SAS are storage protocols, they are used as an interface to storage devices. Storage devices that use the SATA and SAS protocols are hard disk drives, optical drives, and solid-state disks. These storage devices reside in appliances like PCs, JBODs, disk arrays (SAN and NAS), multifunction printers, set-top boxes, and any other appliance that requires data to be stored for any length of time. Figure 1 depicts a typical appliance in which SATA or SAS would be used.

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Figure 1. SAS Disk Array Example



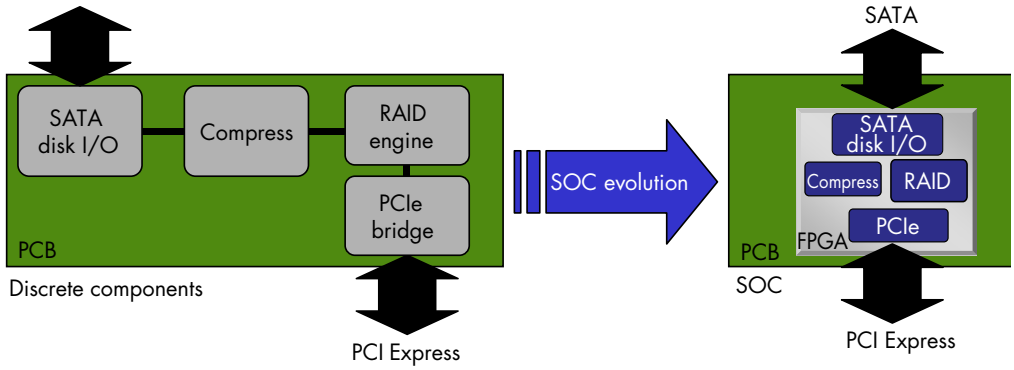
SATA is used in cost-sensitive applications, like PCs, set top boxes, SOHO storage enclosures, and other consumer-based applications. Designed as a replacement for ATA/IDE, this protocol predominantly is found in devices where low cost is essential.

In comparison, SAS is used in higher end systems, like SAN and NAS disk arrays, that are designed for high availability and little to no down time. These systems typically reside in data centers and provide five (5) nine's (9's) of availability, which means up-time 99.999% of the time. Applications needing this type of fault-tolerant storage are in the banking and stock trading industries. This type of reliability offered by SAS comes with a higher price tag, a justifiable return on investment when handling mission-critical data storage. SAS was designed as a replacement for SCSI, the protocol previously used for this type of storage.

FPGA Use of SATA and SAS

Supporting a storage interface is just one of many different application needs to which an FPGA can conform, but is not the only way an FPGA can be used in storage appliances. The FPGA also can bridge different protocols, such as bridging simple bus I/Os like PCI Express® (PCIe®) to SATA or SAS, or more exotically, bridging network interfaces such as Gigabit Ethernet (GbE), Fibre Channel, or SONET to SATA or SAS. In addition, an FPGA provides value-added functions to simple bridging applications, making the FPGA a system on chip (SOC). These value-added SOC functions include RAID, data compression, packet processing, and many more. By enabling development of SOC solutions, the FPGA simplifies system design, meaning that the FPGA reduces the need for multiple discrete devices by consolidating those functions in a single device. Figure 2 demonstrates how an FPGA integrates functions to create an SOC for a RAID controller.

Figure 2. SOC Example



The FPGA offers an excellent platform on which to integrate many discrete ASIC or ASSP functions into a single chip solution. Now that Altera FPGAs support SAS and SATA natively with the integrated transceivers, it is possible to leverage the integration option for storage applications.

Altera SATA/SAS Solutions

Altera has developed SATA and SAS solutions based on the latest 40-nm Stratix® IV GX, Arria® II GX, and Arria II GZ FPGAs with transceivers and 40-nm HardCopy® IV GX ASICs with transceivers. All of these device families support transceiver rates in excess of 6 Gbps, and can support all of the SATA and SAS data rates listed in Table 1. The Altera FPGAs and ASICs, coupled with SATA and SAS intellectual property (IP), offer a solution for developing storage interfaces on a single chip. This section describes which SATA and SAS standards are supported by Altera transceiver solutions, the electrical specification compliance of the transceivers (Table 2), and the IP used for SATA and SAS.

Table 2. Altera Hardware Support

Device	Logic	Transceivers	Memory	SATA/SAS
Arria II GX FPGA	Up to 256 K	Up to 16 at 6.375 Gbps	DDR3 at 400 MHz	SATA I, II/SAS I
Arria II GZ FPGA	Up to 350K	Up to 24 at 6.375 Gbps	DDR3 at 400 MHz	SATA I, II, III/SAS I, II
Stratix IV GX FPGA	Up to 530K	Up to 32 at 8.5 Gbps, up to 16 additional at 6.5 Gbps	DDR3 at 533 MHz	SATA I, II, III/SAS I, II
HardCopy IV GX	Up to 11.5M gates	Up to 36 at 6.5 Gbps	DDR3 at 533 MHz	SATA I, II, III/SAS I, II

Altera Hardware Solution

The transceivers comply with the electrical standards for both SATA and SAS. Compliance to the electrical standards is accomplished using either built-in features in the transceiver block or with a small number of logic-based designs. Altera's partner companies have several IP offerings that complete the SATA and SAS solutions, ranging from SATA 1 to SAS 2 in both host and device modes, which are summarized in Table 3.

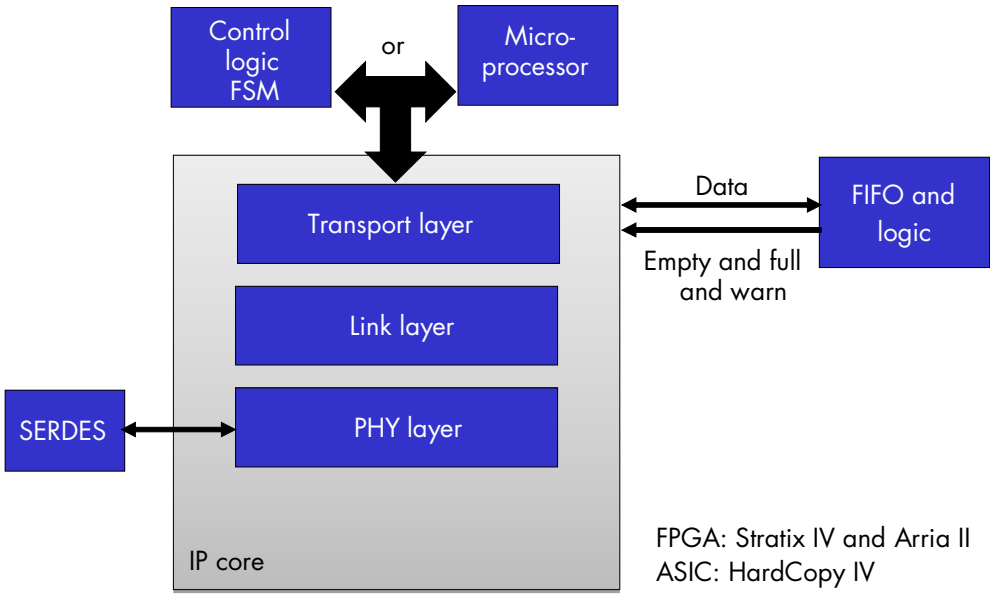
Table 3. Altera Hardware Compliance

SATA/SAS Specification	Arria II GX, Arria II GZ, Stratix IV GX, and HardCopy IV GX
Out of band signaling (OOB)	✔
Auto speed negotiation	✔
Rx/Tx electrical and jitter	✔
Spread spectrum clock (SSC)	✔
PPM tolerance	✔
Round-trip latency	✔
eSATA (cable)	✔

SATA/SAS IP Solution

The IP portion of the Altera solution is core to the SATA and SAS I/O connectivity. The FPGA and ASIC provide the foundation, but the IP makes the SATA and SAS I/O possible. Altera has partners that have developed SATA and SAS IP for both host and device interfaces. As shown in Figure 3, the IP core has all the basic components of a SATA and SAS interface: a physical layer interface that connects to the embedded transceivers, a link layer, and a transport layer. In addition, the IP core includes a processor interface that provides a pathway for a host system to monitor core and provide control instructions. The core uses the 8b/10b coding block, the DPRIO block, and the signal detect and electrical idle—all in the Altera transceivers—for protocol coding, speed negotiation, and out-of-band signaling.

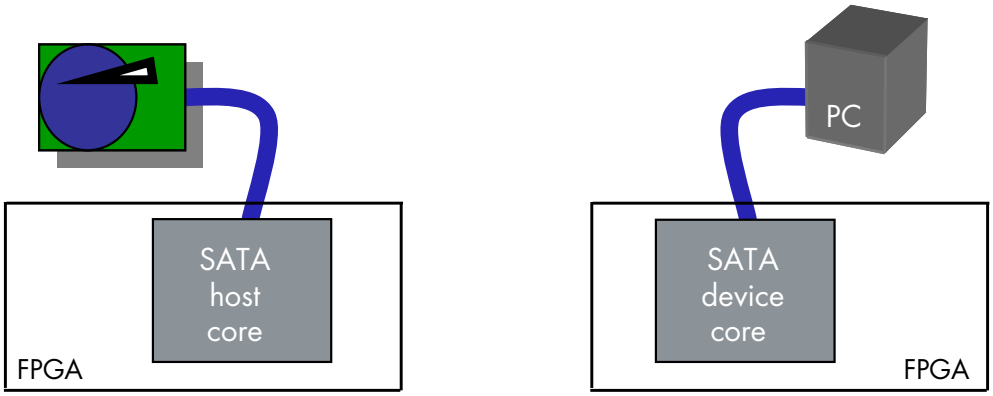
Figure 3. SATA/SAS IP Core



Building a SATA and SAS Solution with IP and Altera Hardware

A good way to demonstrate the capability of the Altera-based SATA and SAS solution is with a design that can test both host and target (device side) functions. This can be done in an FPGA by using a host or device IP core, a FPGA, and a host controller in a PC or disk drive. While SATA is used in Figure 4, either a SATA or SAS core may be used in the host or device designs. In the target design, the FPGA acts as a storage device for the host controller in the PC. In the host design, the FPGA performs host controller functions and stores data on the hard drive. The SATA host controller reads and writes data to and from the SATA hard disk drive, and a SATA target provides an endpoint storage interface for stored data to the PC.

Figure 4. Host (left) and Device (right) Design Examples



The FPGA and IP provide the foundation for SATA interface to both host and target devices, but more is needed. For a complete target (device) solution, a storage device like a hard drive or flash drive must be connected to the FPGA. A complete host solution needs application layer software added to the IP to enable data to be passed from one application to a storage device connected to the FPGA. Both the host design and target design are used for interoperability and industry compliance testing, as these allow both host and device functionality to be verified.

Altera Development Platforms

For design validation testing, Altera has three hardware platforms, two of which are based on Stratix IV GX FPGAs and one based on the Arria II GX FPGA. The Stratix IV GX platforms include the Stratix IV GX signal integrity board (Figure 5) used in conjunction with an SMA to SATA paddle card for SATA I/O connectivity, and the Stratix IV PCIe development board (Figure 6) with the high-speed mezzanine card (HSMC) to SATA/SAS paddle card. The Arria II GX platform includes the Arria II GX PCIe development board (Figure 7) with the HSMC to SATA/SAS paddle card. These hardware platforms plus a soft SATA/SAS IP core can be used for functionality, specification-compliance, interoperability, and performance testing.

Figure 5. Stratix IV GX FPGA Platform with SATA/SAS SMA Paddle Card

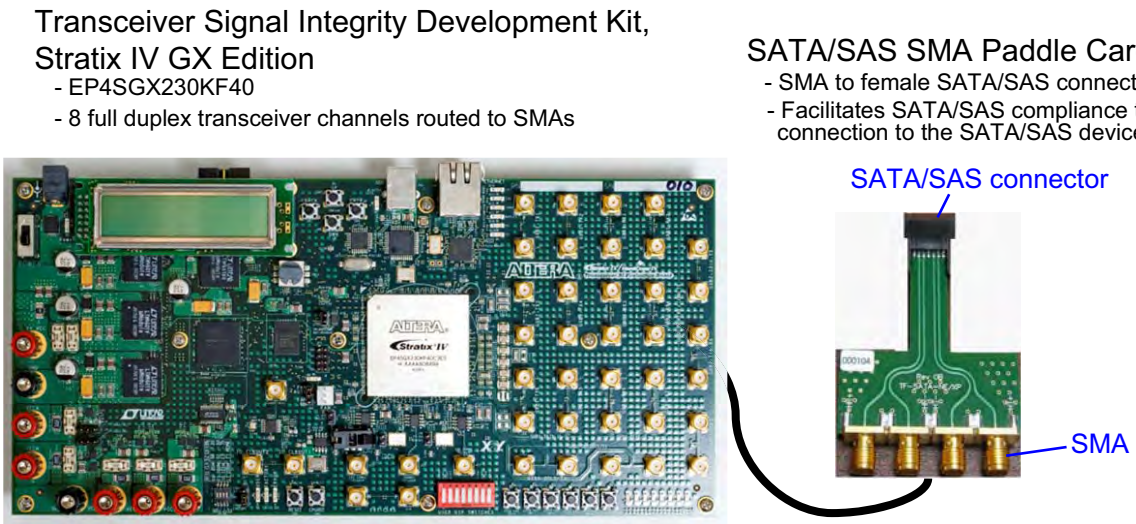


Figure 6. Stratix IV GX FPGA Development Kit with SATA HSMC Daughter Card

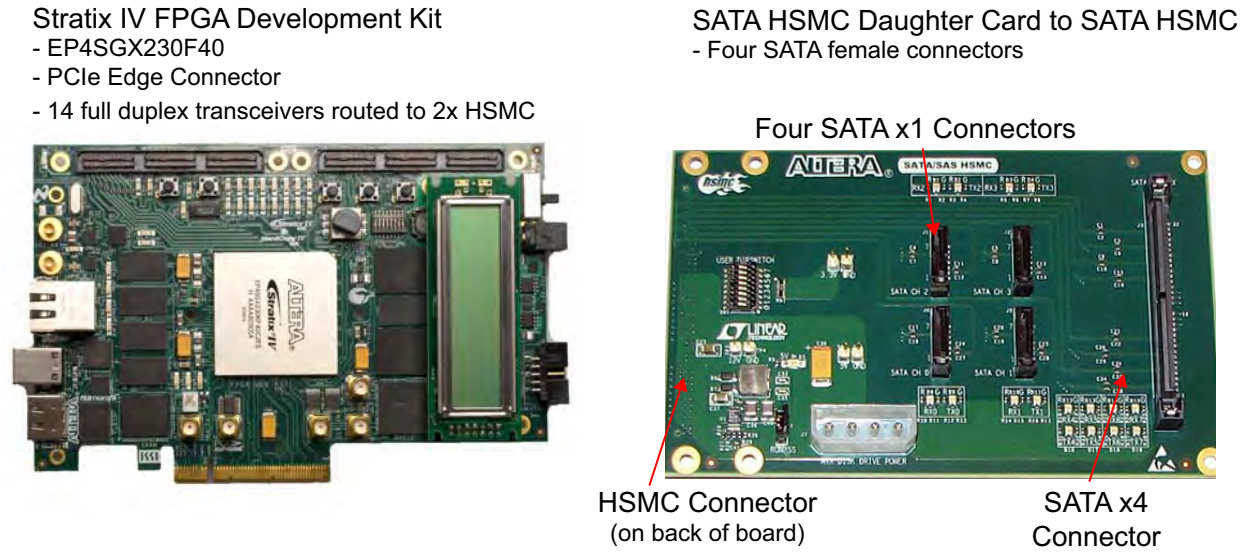
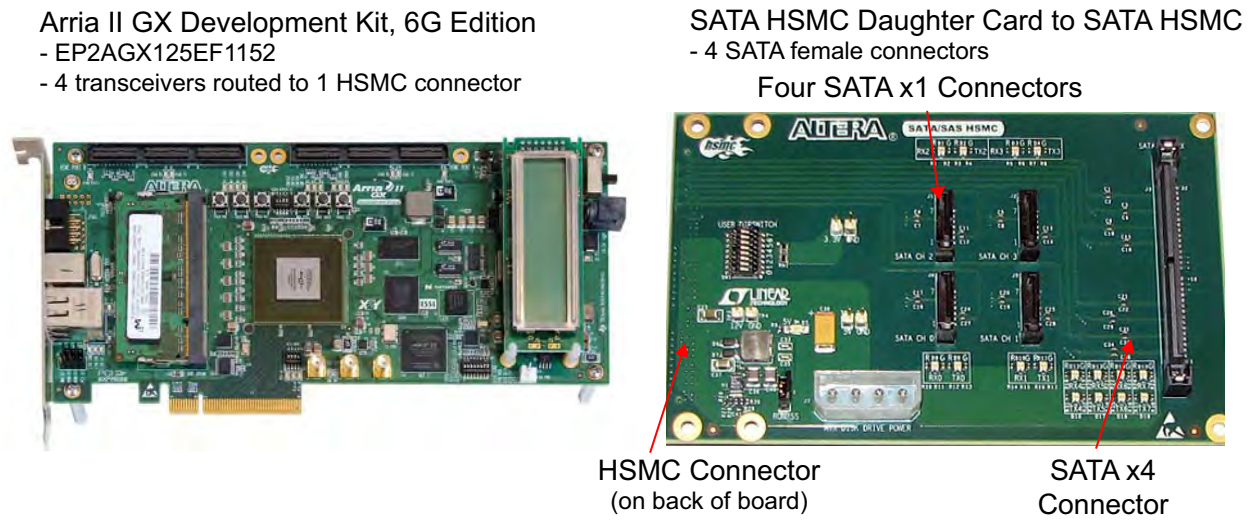


Figure 7. Arria II GX FPGA Development Kit with SATA HSMC Daughter Card



Conclusion

Altera's 40-nm FPGAs and ASICs with transceivers provide an excellent way to develop SOC solutions for storage applications. The FPGA fabric enables system designers to integrate more functions in a single-chip solution, simplifying solution design and enabling integration of transceivers for SATA/SAS I/O connectivity. Altera's portfolio of 40-nm FPGAs and ASICs transceivers in combination with SATA/SAS IP cores creates a interface that can be used for a SATA/SAS solution.

Further Information

- SATA and SAS:
  www.altera.com/technology/high_speed/protocols/sata-sas/pro-sata-sas.html
- Arria II FPGAs: Cost-Optimized, Lowest Power 6G Transceiver FPGAs:
  www.altera.com/products/devices/arria-fpgas/arria-ii-gx/aiigx-index.jsp
- Literature: Arria II GX and Arria II GZ Devices:
  www.altera.com/literature/lit-arria-ii-gx.jsp
- Literature: Stratix IV Devices (E, GX, and GT variants):
  www.altera.com/literature/lit-stratix-iv.jsp
- Transceiver Signal Integrity Development Kit, Stratix IV GX Edition
  www.altera.com/products/devkits/altera/kit-signal_integrity_sivgx.html
- Stratix IV GX FPGA Development Kit
  www.altera.com/products/devkits/altera/kit-siv-gx.html
- Arria II GX FPGA Development Kit, 6G Edition
  www.altera.com/products/devkits/altera/kit-arria-ii-gx-6-gbps.html
- Serial ATA (SATA):
  www.serialata.org
- Serial Attached SCSI (SAS):
  www.scsita.org

Acknowledgements

- Bryce Mackin, Product Marketing Manager, I/O Solutions, High-End Product Marketing, Altera Corporation

Document Revision History

Table 4 shows the revision history for this document.

Table 4. Document Revision History

Date	Version	Changes
July 2010	2.0	■ Added Table 2, Figure 6, and Figure 7. ■ Updated Table 3 (previously Table 2), Figure 5 (previously Figure 6), Altera SATA/SAS Solutions, Altera Development Platforms, Further Information. ■ Removed Figure 3. ■ Minor text edits.
March 2009	1.3	Updated Bridging Solution, Development Platform, Figures 2, and Figure 5.
February 2009	1.2	Updated Figure 6.
February 2009	1.1	Minor text edits.
February 2009	1.0	Initial release.