White Paper

Military Benefits of the Managed Risk Process at 40 nm

Introduction

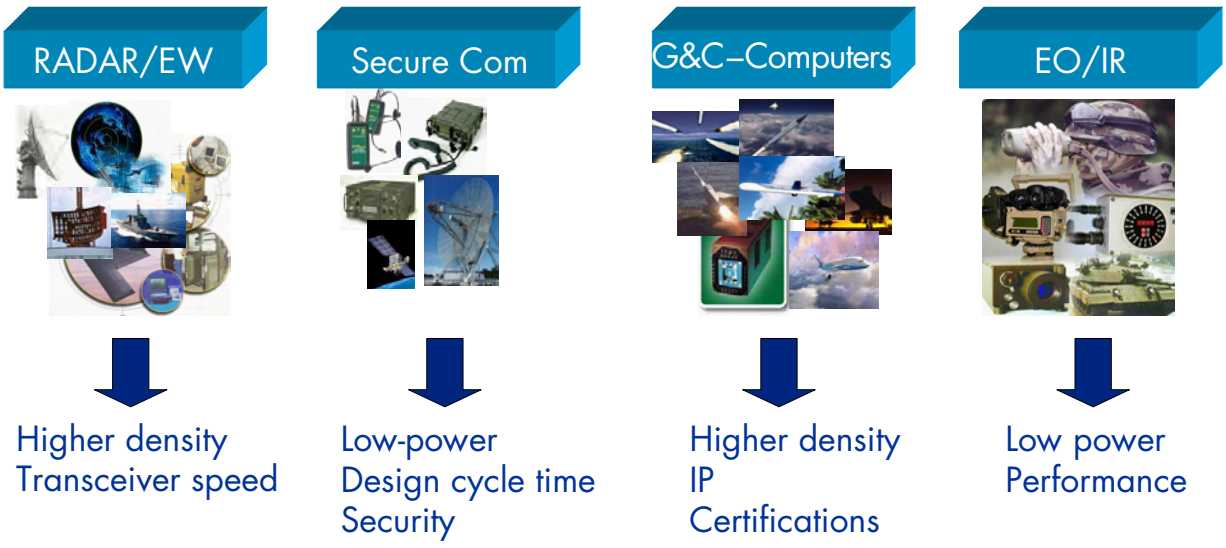
Every successive technology node in the silicon manufacturing process timeline presents new and significant technical challenges. Historically, these challenges have been addressed head-on with the knowledge that increasingly dense FPGAs will always have buyers because of the steady demand created by Moore's Law across most industries. Military designers have traditionally spanned the entire space between "early adopters" and "followers" in design cycles by adopting more dense logic devices for size, weight, and power reduction, depending on the mission criticality of performance (and price sensitivity) of the digital logic in these designs.

As silicon manufacturing technology moves ahead to each new and lower process technology node, a very careful risk decision must be made by both manufacturers, such as Altera, and digital designers. Altera works to ensure that the next process node is instituted at the right time to provide the right price point, while designers need to be assured that the added functionality and capability justifies the cost and risk of overcomplicating the design process and silicon delivery schedule. This process has led to the decision to accelerate the development of the 40-nm silicon development node, and make higher density and higher speed transceiver technology available to military users by the beginning of 2009. Military customers can be assured that a measured risk management process has been applied in manufacturing design and production. By communicating the risks and opportunities of 40-nm FPGAs to our military customers, Altera aims to help digital designers measure the risks and opportunities in defense electronics with these larger and more power-efficient devices.

Military User Requirements

Military users of FPGAs vary widely in their design requirements, but can be broadly characterized by the features that FPGAs currently drive in their designs (see Figure 1). The application areas where extremely high-density Altera® Stratix® IV GX FPGAs will see the most use is in radar and electronic warfare, and in high-capacity waveforms in secure communications. As these systems incorporate more digital up- and downconversion, sampling, fast Fourier transform (FFT), pulse compression, and filtering functions, system-on-a-chip (SOC) solutions will extend state-of-the-art sensor discrimination by allowing for more sensor channels with higher resolution.

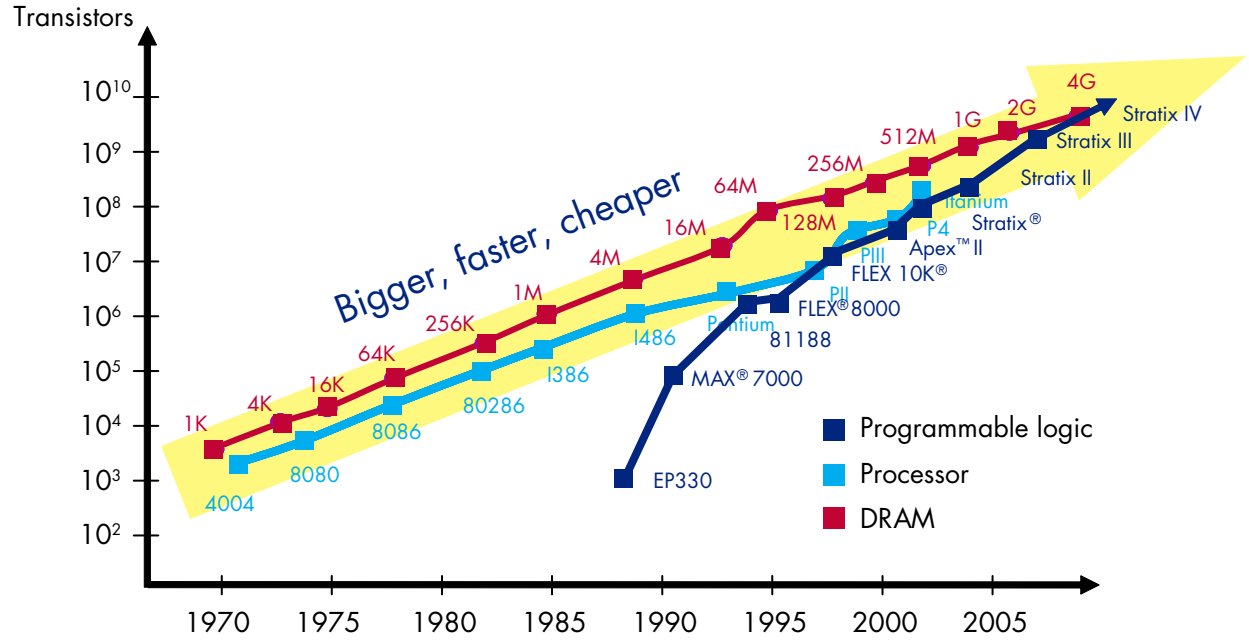
Figure 1. High-Level Overview of Military Customer Requirements



FPGAs at the Heart of the System

FPGA transistor densities (usable transistors) in the Stratix IV family are now in the same class as processors and DRAMs. A growth curve in processor, memory, and programmable logic transistor density is shown in Figure 2.

Figure 2. FPGAs Tracking to Moore's Law



With these more complex devices come significant opportunities to consolidate complex algorithms, reduce component count, and create systems that are more flexible with FPGA designs. This flexibility comes at a potential cost in design effort and verification.

Product History

Today's military applications use FPGAs fabricated at the 130-nm, 90-nm, and 65-nm process technology nodes. Each generation of Stratix and Cyclone® FPGA products has not only kept pace with Moore's Law, but also offered military customers substantial advantages in power management, dedicated digital signal processing (DSP) logic, and embedded memory. Embedded soft processors and integrated microprocessors have given designers multiple, flexible options for device integration.

Altera and competitor FPGA product releases at each silicon development node have focused on first bringing high-density logic to production, then pursuing variants of the FPGA devices with high-speed serial transceivers. However, this steady march of product releases undergoes a strategic shift at both the 65-nm and 40-nm process nodes, as transceiver-capable devices will be available first with Stratix IV GX FPGA devices.

Opportunities in Moving to 40 nm

Altera FPGA test chips from Taiwan Semiconductor Manufacturing Company (TSMC) at 65 nm have had unprecedented success in design and process technology. Both logic modules and transceiver designs were successfully tested and fabricated with the confidence to inspire the shrinkage of the 65-nm architecture to 40 nm. Stratix IV test chips on early 40-nm processing technology have been equally successful.

Rather than remain satisfied with successful Stratix III 65-nm products, Altera and TSMC saw an opportunity to accelerate the move to Stratix IV 40-nm devices. This frees up engineering resources to focus on offering 40-nm transceiver devices to military customers earlier. This, in turn, enables an accelerated pace of military designs and

provided the opportunity for enhanced obsolescence management at a single transceiver technology node. Table 1 lists the advantages of Stratix IV devices for defense systems.

Table 1. Technology Opportunities With Altera Stratix IV 40-nm FPGA Devices

Improvements	Advantages
Up to 680K logic elements (LEs)	Larger designs integrate more functions in one chip
Flexible power settings	Control of the performance-vs.-power balance
Up to 1360 18 x 18 multipliers	Higher density signal processing
Up to 22.4 Mbits memory	Use fewer off-chip resources
Up to 48 transceivers at speeds up to 8.5 Gbps	Massive increase in on-chip\off-chip bandwidth
Up to 16 global, 88 regional clocks	More flexible clock management

Risks of Moving to 40 nm

The opportunities and advantages of moving to a new technology node are carefully balanced against the risks of making the move. Potential risks for military system FPGA designers include on-time availability of the devices (both initial and full production), manufacturing defects in new devices, price uncertainty, and the design complexity and device utilization of the larger Stratix IV devices. Utilizing (or optimizing) proprietary intellectual property (IP) designed for lower technology nodes is also an important consideration. Each of these risks should be investigated and managed to confidently design with 40-nm Stratix IV devices.

Opportunity and Risk Management

The 40-nm manufacturing process leverages all of the advantages of the 65-nm architecture, as both were developed on a common platform. In addition to this low-risk, high-opportunity approach, manufacturing risk, design complexity and compile time, and cross-platform design porting opportunities are being actively managed.

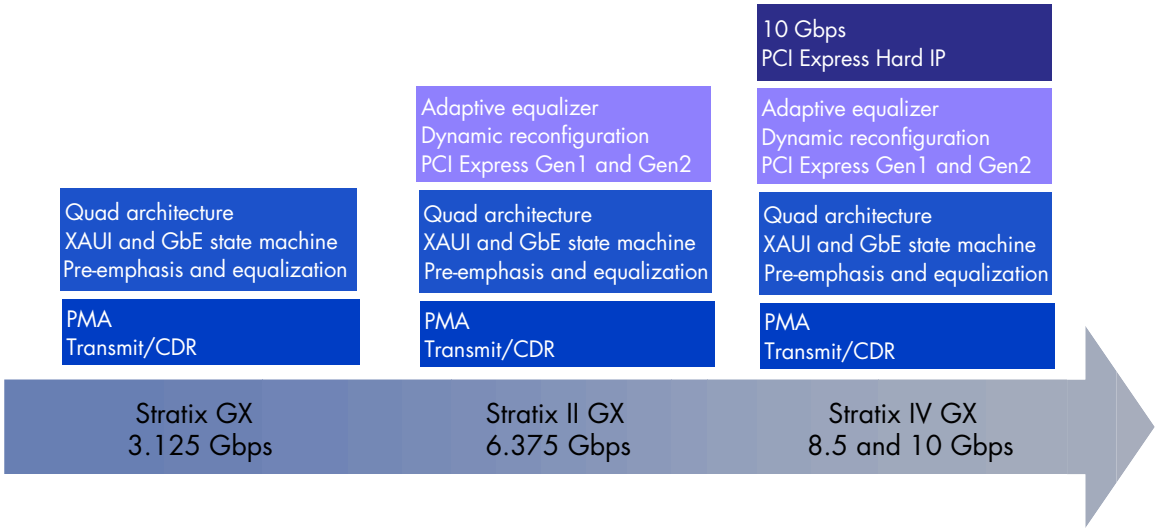
Manufacturing

Why should systems designers be concerned about the manufacturing source of the FPGA? Military electronics users probably have the highest vested interest in looking deep into the operations of their potential programmable logic supplier for several reasons. Military electronics systems have exceptionally long design and verification cycles. Military design architects must seriously consider the trade-off between remaining one technology generation behind competitors with market-tested silicon, or make the move to leading-edge technologies to gain device speed and bandwidth. The most efficient way to assess the risk of leading-edge technology is to evaluate the active risk management procedures of the FPGA manufacturing process.

An important part of the FPGA supplier decision is existing manufacturing relationships. Risk factors include strength of the manufacturer relationship, the number of years the partnership has been in place, and the technology leadership position of the manufacturer. Manufacturing risk at any silicon technology node translates into supplier schedule risk and device reliability risk. Altera and TSMC have maintained a manufacturing relationship for over 15 years, and shared the research and development expenses of 40-nm manufacturing. In return for this investment, Altera is the lead customer for 40-nm devices.

An additional risk factor in manufacturing is transceiver design consistency. Transceiver designs can be migrated from one silicon node to the next with minimal risk when a consistent methodology is used and a stable design team is in place. As shown in Figure 3, Altera has maintained the same transceiver design team for each iteration of Stratix transceiver technology.

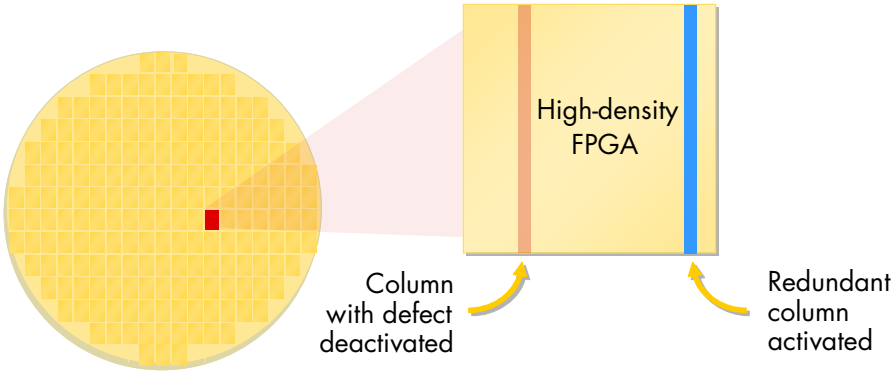
Figure 3. Altera Transceivers Are Built on a Consistent Process With a Single Design Team



Altera utilizes a patented redundancy technology (Figure 4) in manufacturing that ensures high yield, and lowers manufacturing risk for Altera and its customers. This technology allows Altera to embrace new process technologies with confidence and a risk-mitigation strategy. The technology also allows individual logic rows to be activated and deactivated in early fabrication testing to increase usable wafer silicon significantly.

Additional details on TSMC's manufacturing technology and Altera's redundant column circuitry can be found in the white paper *Leveraging the 40-nm Process Node to Deliver the World's Most Advanced Custom Logic Device*.

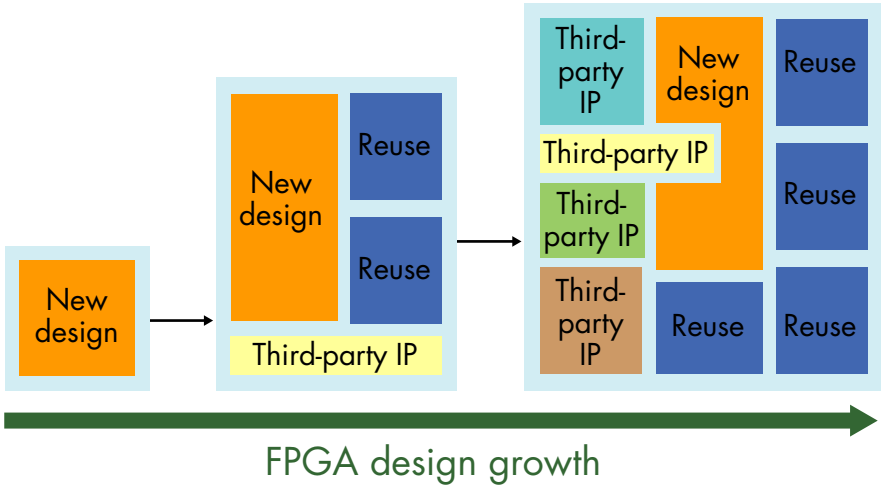
Figure 4. Altera's Patented Redundancy Technology Reduces Manufacturing Yield Risk



Design Complexity and Compile Times

Some of the risks in designing larger and larger FPGAs are the significant impacts design complexity and compile times have on defense electronics design schedules. If not managed with smart approaches to design software, design times will scale logarithmically, as shown in Figure 5. In order to manage this risk, Altera has made a significant investment in design tools and coordinated the release of these next-generation tools for larger Stratix IV FPGAs.

Figure 5. As FPGA Size Increases, Design Complexity Becomes Both Risk and Opportunity



Compile times in FPGA design are a function of the design tool environment, design complexity, and constraint environment. The more constrained a user is regarding power and chip utilization, the more time will be spent on exploring place-and-route design space. Altera's Quartus® II design software reduces compile time risk in FPGA placement and routing through advances in parallel processing support, large bus operating system support, and user tools (Incremental Compile and Logic Lock) to allow design segmentation and partition lockdown.

Porting FPGA Designs Across Platforms

As FPGAs have become more complex, very few designs are now accomplished from the ground up. The re-use of IP blocks—either purchased from a third party or encapsulated and re-used within an engineering organization—is a critical part of military FPGA design.

Purchasing or re-using high-speed, serial data cores is a low-risk approach to system design, especially when these cores can be verified to a commercial performance standard. However, for algorithmic blocks and very special-purpose IP, there is a level of assurance and trust implicit in using third-party applications. In this case, reductions in development risk are offset by increases in interoperability and performance risk.

There are four specific risks involved with the portability of IP between defense programs, or "block" implementations within a defense program. The first is transferring IP blocks from one design to another using similar FPGA design tools and devices. Despite the cost savings in not having to create each building block from scratch, there is a risk that the IP blocks are imperfectly encapsulated. This means that there may be unnecessary timing constraints to be met when reusing blocks. The best way to address this risk is with careful internal IP documentation and third-party synthesis tools.

The second risk is transferring IP blocks from one generation of FPGA to the next (i.e., from 90 nm or 65 nm to 40 nm). For IP offered by an FPGA provider, these IP blocks are often re-released for optimal performance on all geometries. However, there is a risk that transferring IP to a more modern device may affect its performance and timing. The process of evaluating the impact on IP and modifying the blocks can be assisted by design partitioning tools available from nearly all FPGA vendors.

The third risk is transferring IP from an FPGA implementation to an ASIC when high volumes, cost sensitivities, or possibly radiation-vulnerable applications are factors. Most design recommendations for FPGA-to-ASIC designs advise that the third-party IP be certified. For HardCopy® ASIC designs, however, transferring this IP is virtually risk free. The design software for FPGA and ASIC is the same, generates both FPGA and ASIC netlists from the same HDL design, and even accounts for voltage changes.

The final and most difficult risk to address is transferring IP from one FPGA vendor to another. Several companies are working on "FPGA-agnostic" application layers to embed computing products, a project that is being driven by government customers who prefer a two-supplier model for defense components. "Changing horses in midstream" is particularly risky in defense electronics, but the risk can be reduced significantly by adopting a single-flow software design system such as Quartus II design software.

Conclusion

As delineated in Table 2, assessing opportunities and risks of 40-nm FPGA technology focuses on confidence of on-time market availability, design productivity, and generational improvements in digital signal processing. Additional resources are available for performing a more in-depth risk analysis for defense customers that can account for special program requirements and schedule sensitivity.

Table 2. Risks and Opportunities of 40-nm FPGA Design

Risk	Opportunity
■ First 40-nm FPGA transceiver to market ■ No 65-nm generation transceiver productized *Impact: Technical issues, delays*	■ Leading-edge technology in on- and off-chip bandwidth ■ Most logic, multipliers, memory, power efficiency at high density ■ Ability to transition to structured ASIC with transceivers *Impact: Significant generational increases in digital logic capability*
Risk Management	**Opportunity Management**
■ Long series of test chips with excellent results ■ High-confidence characterization and re-use of power-efficient 65-nm process *Impact: Confidence in delivery of 40-nm technology*	■ Strong investment in design productivity for high-density design ■ Exclusive partnership with industry silicon-fabrication leader *Impact: Immediate availability to design and leverage opportunities in 40-nm technology*

As with most new technologies, taking advantage of the full capabilities of Stratix IV FPGAs will necessitate architectural changes in most applications. More of the management and processing functions in military embedded systems can be handled effectively and efficiently with reprogrammable logic or in reconfigurable soft processors. With the amount of available logic resources and the ability to capture more IP as portable VHDL code, Stratix IV design opportunities for military developers offer significant returns in design process and reuse.

Further Information

- Altera's Military Risk and Productivity Management:
  www.altera.com/products/devices/stratix-fpgas/stratix-iv/end-markets-applications/stxiv-military.html
- *Leveraging the 40-nm Process Node to Deliver the World's Most Advanced Custom Logic Device*:
  www.altera.com/literature/wp/wp-01058-stratix-iv-40nm-process-node-custom-logic-devices.pdf
- *40-nm FPGAs and the Defense Electronic Design Organization*:
  www.altera.com/literature/wp/wp-01064-40nm-fpgas-and-defense-electronic-design-organization.pdf
- *Increasing Productivity With Quartus II Incremental Compile*:
  www.altera.com/literature/wp/wp-01062-quartus-ii-increasing-productivity-incremental-compilation.pdf
- *Comparing IP Integration Approaches for FPGA Implementation*:
  www.altera.com/literature/wp/wp-01032.pdf
- Quartus II Design Software:
  www.altera.com/products/software/sfw-index.jsp
- Increasing Productivity with SOPC Builder:
  www.altera.com/products/software/products/sopc/sop-index.html
- Altera's Enhanced COTS Initiative:
  www.altera.com/end-markets/military-aerospace/overview/mil-overview.html
- Altera's 40-nm Portfolio:
  www.altera.com/b/40-nm-devices.html

Acknowledgements

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