

## Developing MSAN Equipment Using Low-Cost FPGAs

### Introduction

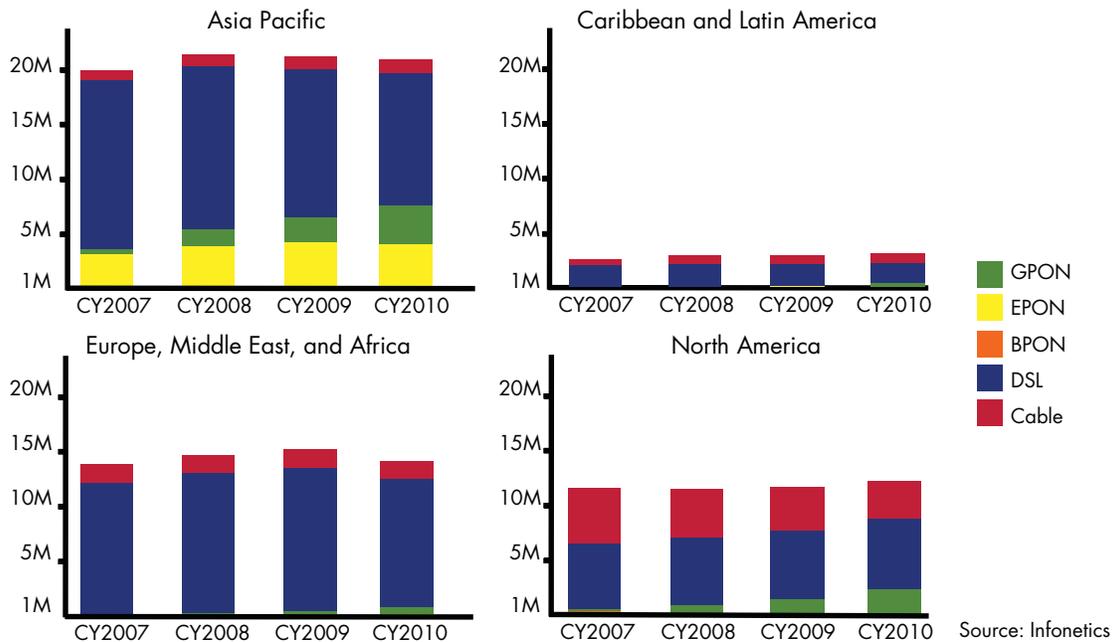
In this paper, we will look at the trends in the multi-service access node (MSAN) equipment market that are forcing developers to re-examine the architectures they have used in the past, as well as driving more and more MSAN OEMs to move to FPGAs to create scalable platforms for MSAN applications. This paper also looks at some of the key features of the low-cost Cyclone® III FPGA family that make it an optimal solution for 5- to 10-Gbps MSAN applications.

### Evolution of the Access Networks

Broadband access networks have evolved over time from copper-based infrastructure to a mix of fiber and copper networks. Different technologies, such as ADSL, VDSL, Cable, EPON, BPON and GPON, are deployed in various regions of the world, with the development to support increasingly high data rates leading to differing regional requirements.

As an example, [Figure 1](#) highlights the regional variations for new broadcast subscriber forecasts. Infonetics forecasts that by 2010, over half of the cable broadband subscribers will be based in North America due to the high penetration of cable television service within the region. Passive optical network (PON) subscribers are expected to grow dramatically at a compound annual growth of 150% through 2010 in North America and Asia Pacific, with Gigabit PON (GPON) gaining traction in China and North America, and Ethernet PON (EPON) dominating Japan. European broadband subscribers will continue to be largely DSL subscribers, although each region has its own variations within it.

Figure 1. New Broadband Subscriber Forecast



Based on these projected variations, standards organizations such as the DSL Forum target specifications for “agnostic access network architectures that deliver inherent quality, scalability, resiliency, and interworking capabilities that enable services to be delivered via multiple business models.” The emerging network requires an access platform that can be configured uniquely for a specific deployment.

## Common MSAN Requirements

Although the structure and requirements for global MSAN equipment are divergent, the business requirements for MSAN equipment are very congruent. All MSAN equipment suppliers are trying to solve the same common issues:

- Supporting evolving business requirements with a scalable architecture
- Meeting aggressive cost/power budgets
- Accelerating time to market
- Developing competitive differentiation
- Reducing total cost of ownership
- Managing risk

ASSP solutions fall short in a number of these key areas, as they have limited flexibility to support evolving requirements, limited or no scalability, increasing power consumption with increased clock rates, limited competitive differentiation options, a huge risk of part obsolescence, and an increased cost of ownership and delayed time to market if network processing unit (NPU) architectures must be changed. [Table 1](#) highlights how fewer high-end NPU ASSP suppliers are available in 2007 versus the number of suppliers available in 2003, due to a large amount of consolidation and several vendors choosing to leave this market completely.

*Table 1. High-End NPU Providers in 2003 vs. 2007*

High-End NPU Providers (2003)	High-End NPU Providers (2007)
Agere	Agere
AMCC	AMCC
Bay Micro	Bay Micro
EZ Chip	EZ Chip
Greenfield	Greenfield
IBM	IBM
Intel	Intel
Motorola	Motorola
Procket	Procket
Raza	Raza
Xelerated	Xelerated
	Cavium

As regional implementations and requirements have evolved and become divergent, it has been hard for fixed-function ASSP devices to keep up. The other problem with fixed function solutions is that they typically have to pick a target application and optimize to that target, which prevents them from leveraging the development costs across many regional markets. Choosing an NPU is a daunting task. The designer must first make sure the NPU is technically capable to meet the bandwidth requirements now and in the future and that it is cost effective at meeting those requirements. Additionally, the designer must be certain that the NPU will not be discontinued, which would effectively kill off all of the code and intellectual property investment for a particular architecture and drastically raise the total cost of the solution.

## Meeting MSAN Requirements Using FPGAs

Altera® low-cost FPGAs offer an optimal solution for developing scalable, flexible solutions meeting stringent technical and business MSAN equipment requirements.

### *Supporting Evolving Business Requirements*

Low-cost FPGAs provide a flexible solution for today's applications as well as a defined roadmap for tomorrow's needs either by migrating to a larger pin-compatible device in the same low-cost FPGA family or by migrating to a

larger, higher performance FPGA family or a high-performance, low-cost structured ASIC solution, as shown in Figure 2.

Figure 2. Altera's Flexible Solutions

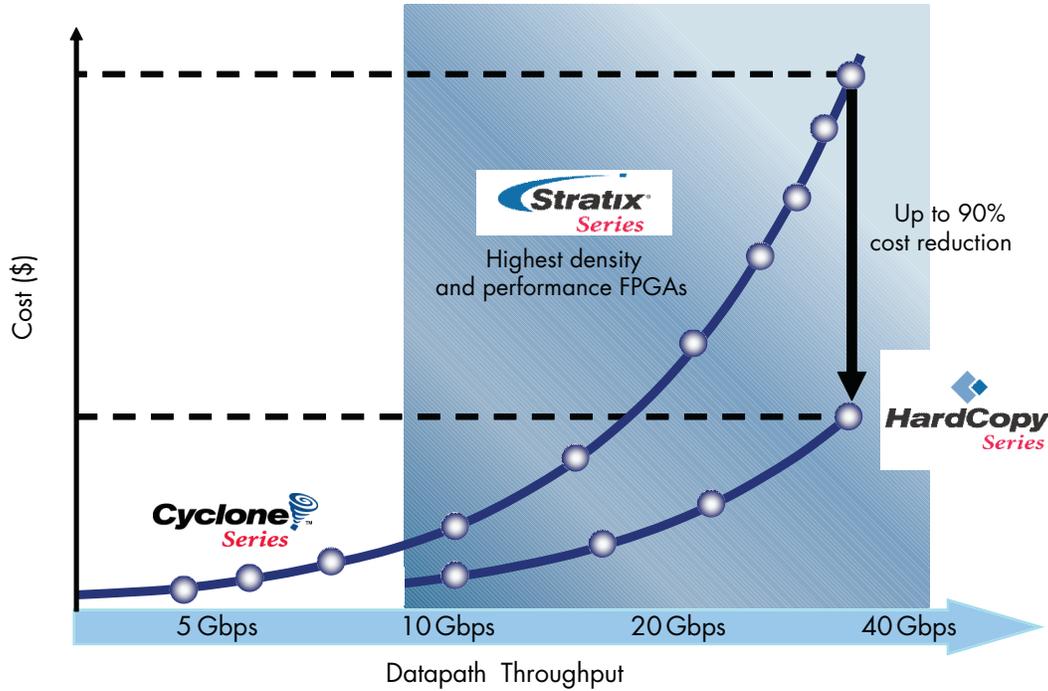


Table 2 compares key factors in supporting evolving packet-processing needs using ASICs, internally developed or ASSP-based NPUs, and FPGA solutions.

Table 2. Evolving Packet-Processing Needs

	In-House ASIC Development	In-House NPU-Based Development	ASSP-Based Development	Packet Processor on FPGA Solutions
Time to Market	Slow	Depends on programming complexity	Fast, if feature set fits; otherwise must wait for next design cycle.	Fast
Flexibility in First Design	High (as long as basic building blocks are in place)	High	High	High
Flexibility to Accommodate New Features	None	Possible if throughput and processors available, but not for dedicated functions	None	Fully flexible, if FPGA resources available; can replace existing features
Development Time	Up to 2 years	1 to 2 years, depending on complexity	6 to 9 months	6 to 9 months
Volume Cost Performance	High volumes	Medium to high volumes	High volumes	Low to medium volumes
Platform Maturity/ Security of Supply	Developed per application, can be difficult to secure supply	Platform per company and generation, questionable supply security	Dependent on vendor and vendor market share, in-house fab, or fabless model	Altera dominates FPGA market, providing widely supported, de facto standard platforms

### Meeting Stringent Cost/Power Budgets

Next-generation MSAN designs require more processing power, yet are constrained by pre-existing power supply budgets and the need for lower power consumption. The Cyclone III FPGA family is an example of how low-cost FPGAs can be used to increase processing and integration resources while lowering power consumption.

### Lower Cost and Higher Functionality

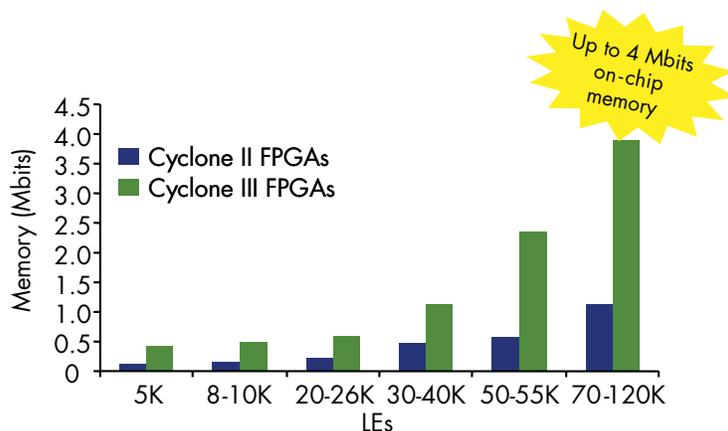
The Cyclone III family is composed of eight devices ranging from 5K to 120K logic elements (LEs) and up to 535 user I/O pins. As shown in Table 3, Cyclone III devices offer up to 4 Mbits of embedded memory, 288 embedded 18-bit x 18-bit multipliers, dedicated external memory interface circuitry, phase-locked loops (PLLs), and high-speed differential I/O capabilities.

Table 3. Cyclone III FPGA Overview

Device	EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
M9K Embedded Memory Blocks (1)	46	46	56	66	126	260	305	432
Total RAM (Kbits)	414	414	504	594	1,134	2,340	2,745	3,888
Embedded 18-bit x 18-bit Multipliers	23	23	56	66	126	156	244	288
PLLs	2	2	4	4	4	4	4	4
Maximum User I/O Pins	182	182	346	215	535	377	429	531
Differential Channels	70	70	140	83	227	163	181	233

Built on Taiwan Semiconductor Manufacturing Company’s (TSMC’s) 65-nm low-power (LP) process technology, Cyclone III devices offer the lowest power consumption of any 65-nm FPGA. An optimal set of silicon and software features drives high-bandwidth parallel processing along with many other cost-sensitive and power-sensitive applications. The Cyclone III family includes specific optimizations beyond previous Cyclone FPGA families and competing low-cost FPGAs to better serve MSAN applications. The most significant improvement is a sharp increase in memory-to-logic ratios, which is directly related to the needs of memory intensive packet processing applications common in MSAN equipment. Figure 3 depicts the increase in memory per logic density between Cyclone III and Cyclone II FPGA families.

Figure 3. Cyclone III Increase Memory to Logic Ratios for MSAN Applications



### Lower Power

Power consumption is a major topic in electronics design today. Whether the limiting factor is a thermal ceiling or a fixed power source to a board that cannot be changed, how much power the device consumes and how much heat it dissipates is now a major battle and affects the competitiveness of the end system. By lowering the power

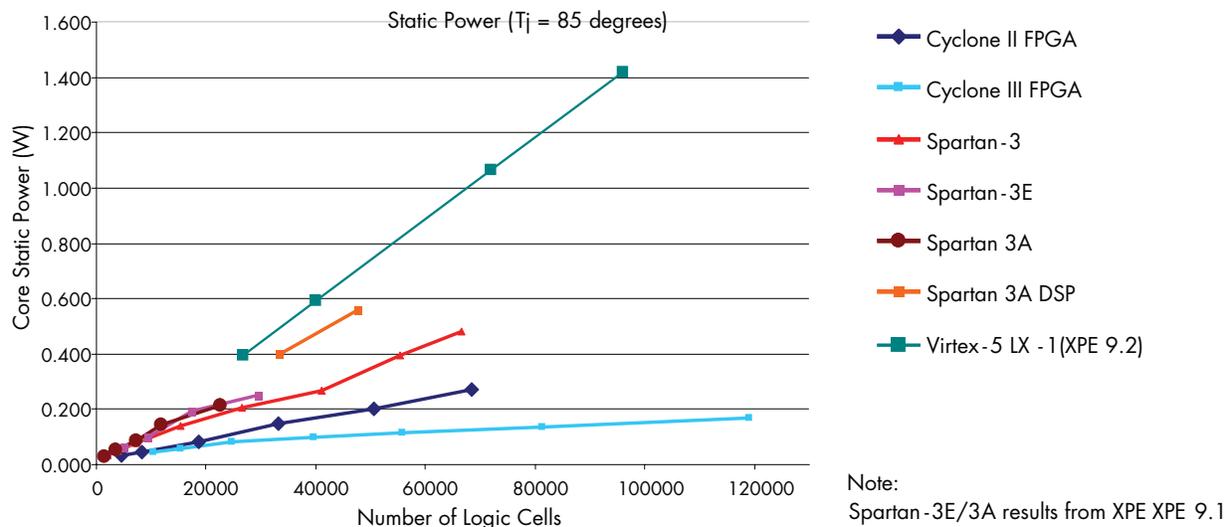
consumption of the FPGA dramatically, FPGA companies can increase logic and other resources included on the device, allowing designers to add next-generation features to systems while still realizing a net reduction in power.

The number one goal in developing the Altera Cyclone III FPGA family was to maintain performance for customer designs while reducing relative power consumption of the device. To realize this goal, Altera chose to use the latest 65-nm LP technology available from TSMC, the same process technology employed for mobile phone chip sets, and the first time an FPGA was designed on a low-power process. In addition, careful consideration was used to determine transistor types for each circuit element to balance performance needs with the need for low leakage currents.

Transistor threshold voltage is the minimum voltage that needs to be applied to the transistor gate to turn on the transistor. Higher transistor thresholds slow down performance but reduce leakage current. High-threshold transistors can be used in non-speed critical circuits such as configuration RAM. Lower transistor threshold voltages improve performance by allowing transistors to be turned on faster at the expense of higher leakage current. These transistors are used only in performance-critical circuits such as those in the LE data path. Another technique to lower leakage current is to use a low-threshold voltage transistor but extend the transistor channel length to reduce the leakage current while maintaining relatively high performance.

The choice of using LP technology and intelligent design optimizations by Altera to reduce power gives Cyclone III FPGAs dramatic power consumption benefits versus other low-cost FPGA families. [Figure 4](#) shows core static power on the y-axis versus the number of logic cells on the x-axis. Cyclone III devices offer a static power advantage at all densities with the benefit growing as densities increase. Remember that static power is a component of total power consumption when the design is stopped and when the design is running, keeping static power low can become a big advantage in meeting aggressive power budget requirements.

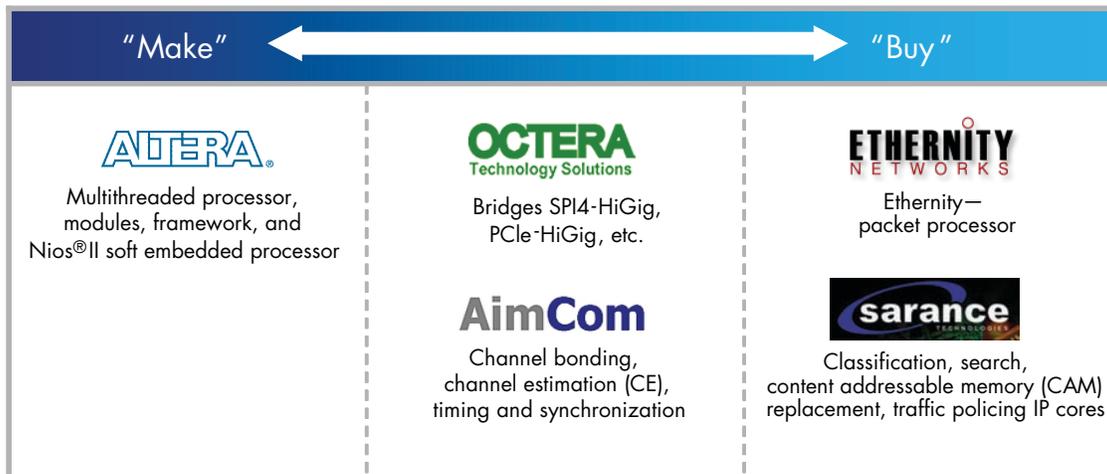
**Figure 4. Cyclone III FPGA Static Power Advantage**



### Accelerated Time to Market and Competitive Differentiation

There is a rich library of intellectual property (IP), reference designs, and turnkey solutions from Altera and partners for key MSAN application areas. Cyclone III devices allow these solutions to be easily customized and differentiated for backplane interfaces, packet processing, and Utopia/POS-PHY interfaces in IP-DSLAM equipment. Depending on the time to market and customization needs, the designer has the option of creating a custom solution or buying a turnkey solution. In either case, IP, reference designs, and IP from Altera and its partners, shown in [Figure 5](#), can provide a head start.

Figure 5. Overview of Altera's FPGA MSAN Solutions Offerings and Partners



### Reduced Cost of Ownership and Risk

Low-cost FPGAs are applicable for a wide variety of wireline communications, wireless infrastructure equipment, automotive infotainment and networking applications, medical, military, and even consumer electronics applications. This broad user base helps FPGA suppliers drive up volumes to reduce unit costs substantially and to keep the parts in the market longer than a fixed-function ASSP device with limited application uses. Many of these application areas have long development and product life cycles that only a programmable logic device can support reliably. Because FPGA source code is portable, designers can rest assured that even if a particular part becomes obsolete, they can easily port the design to a next-generation FPGA device leveraging the same software and IP.

### Conclusion

Low-cost FPGAs can provide MSAN equipment manufacturers a competitive edge by effectively addressing common business and technical requirements required for these applications including:

- Supporting evolving business requirements with a scalable architecture
- Meeting aggressive cost/power budgets
- Accelerating time to market
- Developing competitive differentiation
- Reducing total cost of ownership
- Managing risk

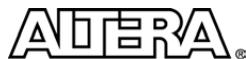
Not all low-cost FPGAs are created equal. Selecting a low-cost FPGA targeting high system integration and low power operation can effectively lower a design's system costs, operating costs, and total cost of ownership.

### Further Information

- *Customizing Multi-Service Access Network Silicon:*  
[www.altera.com/literature/wp/wp-01030.pdf](http://www.altera.com/literature/wp/wp-01030.pdf)
- Infonetics:  
[www.infonetics.com](http://www.infonetics.com)

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