

This white paper discusses the major challenges associated with accurately predicting power consumption in FPGAs, namely, obtaining accurate signal activities, static power modeling, and dynamic power modeling, as well as how Altera addresses these challenges through the PowerPlay early power estimator and the Quartus® II PowerPlay power analyzer. This paper also presents the accuracy of the model by comparing predicted power consumption with actual silicon measurements using an extensive suite of real-world customer designs. Using these best-in-class power analysis tools, a designer can model the power consumption of their design to within, on average, $\pm 10\%$ accuracy when used with accurate design information.

Introduction

As designs get larger and add more system functions implemented on FPGAs, and as the advanced silicon process technology moves into smaller geometries, power consumption is increasingly a concern for today's FPGAs. When designing a printed circuit board (PCB), the power consumed by a device determines not only the power supply, but also the cooling system required for the device. Therefore, obtaining an accurate estimate of power consumption is essential to design a system's power supplies, voltage regulators, heat sink, and cooling system, and is crucial in developing an appropriate power budget for the entire system.

Factors Contributing to Accurate Power Estimates

Obtaining an accurate power estimate relies on two important factors: accurate signal activities and accurate power models. Power models define the power characteristics of the device, and the signal activities define the behavioral characteristics of each signal in the design. While the power models are provided by FPGA vendors, the designer must provide accurate signal activities to obtain the best possible estimate of overall power consumption.

Signal Activities

A good power analysis tool should provide a flexible framework for specifying signal activities. Using representative signal activity data during power analysis is important, as inaccurate signal activity data is the largest source of power estimation error.

Altera's PowerPlay power analysis tools use the following sources to provide information on signal activity:

- Simulation results
- User-entered node, entity, and clock assignments

- User-entered default toggle rate assignment
- Vectorless estimation

For some Altera® device families, the PowerPlay power analyzer automatically estimates signal activity on nodes that have incomplete simulation or user-entered signal-activity data. Vectorless estimation statistically estimates the signal activity of a node based on the signal activities of all nodes feeding that node, and on the actual logic function that is implemented by the node. In addition to combinational logic functions, vectorless estimation also estimates signal activity data for nodes that are the outputs of multipliers, memories, and other blocks. Vectorless estimation is generally accurate for combinational nodes, but not for registered nodes. Therefore, simulation data for at least the registered nodes and I/O nodes is needed to ensure accuracy.

Power Models

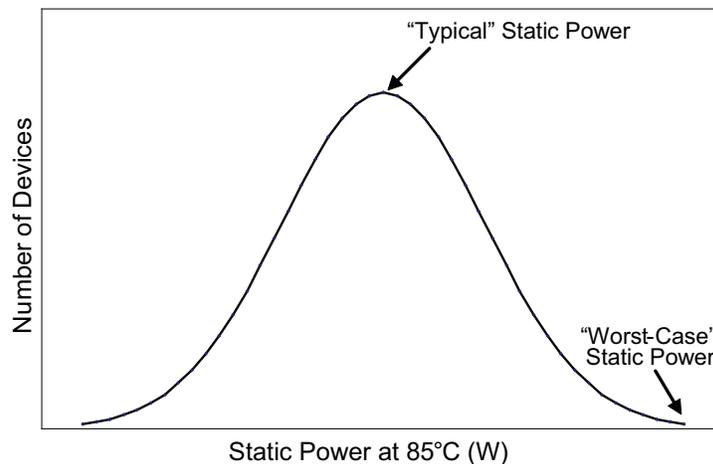
The other critical component of accurate power analysis is the power models that the power analysis tools use to characterize power consumption in the device. Device power consumption is comprised of static power and dynamic power, and each should be modeled separately by the power analysis tools. When combined with representative signal activity data, this approach provides the best and most accurate estimate of the design's overall power consumption.

Static Power Models

Static power is the power consumed by a device due to leakage currents when in quiescent state, that is, with no activity or switching in the design. The amount of leakage current varies with die size, junction temperature, and process variation. Static power can be modeled using a set of exponential equations that vary with junction temperature (T_j): $P_{\text{static}} = Ae^{BT_j} + C$.

The dependence of static power on process variation is modeled using separate static power equations for “typical” and “worst-case” devices. Every device shipped is guaranteed to have static power within the worst-case curve, while the typical curve represents the more likely static power consumption of a typical device, as shown in Figure 1.

Figure 1. Static Power Distribution Curve



Dynamic Power Models

Dynamic power is the additional power consumed through device operation caused by signals toggling and capacitive loads charging and discharging. As shown in [Figure 2](#), the main variables affecting dynamic power are capacitance charging, supply voltage, and clock frequency.

Figure 2. Variables Affecting Dynamic Power

$$P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$$

The diagram shows the equation $P_{dynamic} = \left[\frac{1}{2} CV^2 + Q_{ShortCircuit} V \right] f \cdot activity$. Three arrows point from labels below to terms in the equation:

- An arrow points from "Capacitance Charging" to $\frac{1}{2} CV^2$.
- An arrow points from "Short Circuit Charge During Switching" to $Q_{ShortCircuit} V$.
- An arrow points from "Percent of Circuit that Switches Each Cycle" to $activity$.

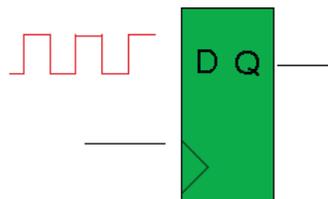
It is important to use software tools that accurately predict the dynamic power consumption of a design. Unsophisticated power analysis tools simply model each circuit as a lumped capacitance. In contrast, the PowerPlay power analysis tools use two very detailed dynamic power models: simulation-based power models and empirical power models.

Simulation-Based Dynamic Power Models

Simulation-based dynamic power models are used to model blocks on the device that are highly configurable, such as the adaptive logic module (ALM) for Stratix® series or logic element (LE) for Cyclone® series FPGAs. It is impractical to generate measurement patterns that cover all supported configurations of these blocks. Instead, the block is broken up into sub-blocks, each with a small number of supported configurations. The detailed block power model is developed by simulating every configuration of each sub-block and modeling the resource as a network of these sub-blocks. The simulation-based power models are then incorporated into the PowerPlay power analysis tools and correlated to silicon measurements.

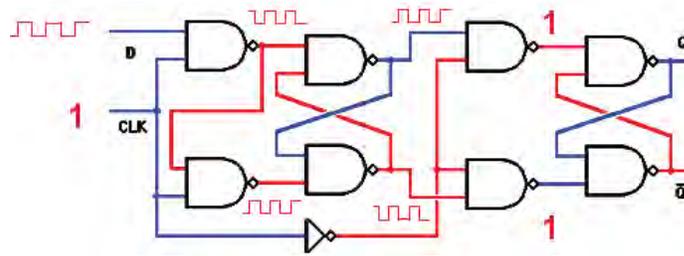
While other unsophisticated power analysis tools treat each block as a simple black box where only input and output transitions are measured, PowerPlay power analysis also measures each block's internal transitions. For example, if the input of a simple register is toggled and the clock held high, as shown in [Figure 3](#), a black box model would simply assume that because the output does not toggle, no power is consumed.

Figure 3. Simple Register



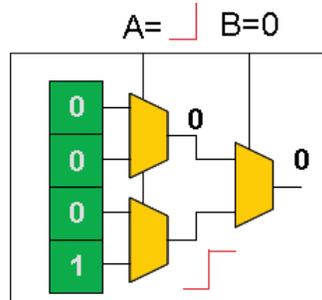
The PowerPlay power analyzer, however, can still accurately predict power consumed in internal nodes by modeling the register's entire internal structure, as shown in [Figure 4](#).

Figure 4. Internal Toggling of Register



Another example is a simple 2-input AND function that can be implemented in an ALM or LE. If one input is held low and another input toggles, a black box model would assume that no power is consumed because the output does not toggle. However, PowerPlay power analysis tools consider every internal multiplexer, buffer, and wire in the block, so power consumed by internal toggles is correctly counted, in this case by the first-stage multiplexer of the look-up table (LUT) shown in [Figure 5](#).

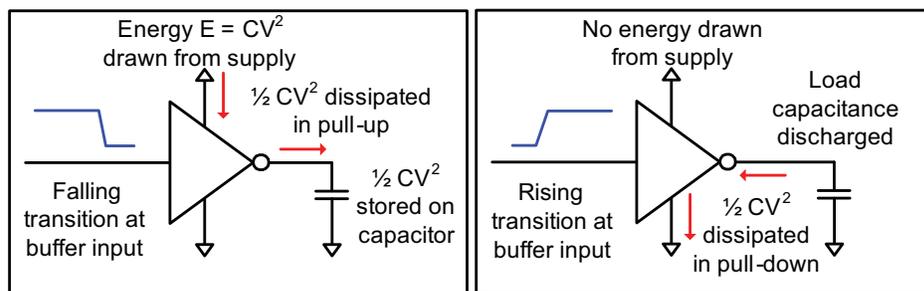
Figure 5. Internal Toggling of AND Gate



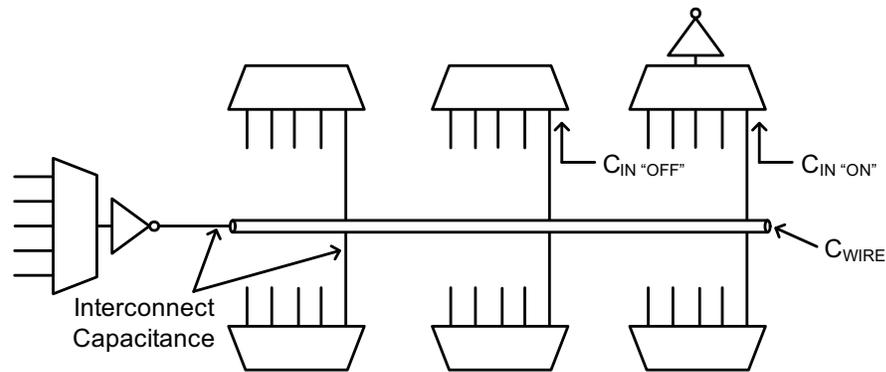
Routing Power Model

A significant portion of total dynamic power is consumed in the programmable routing fabric of the FPGA. Dynamic routing power has two main components: short-circuit current and power dissipated in charging and discharging load capacitances. [Figure 6](#) illustrates how power is consumed when an inverter switches a capacitive load.

Figure 6. Power Consumed in an Inverter



For FPGA routing switches, the load is the lumped capacitance of all downstream circuitry, including the metal capacitance of the wire and other interconnect, and the input capacitances of multiplexers and gates that listen to the wire. The loading on a typical FPGA routing wire is shown in [Figure 7](#).

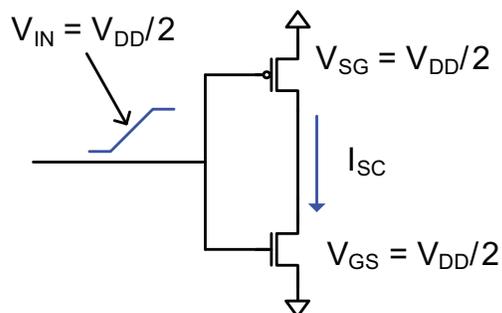
Figure 7. Loading on a Typical FPGA Wire

The input capacitance of each multiplexer is determined by its configuration. Quartus II software uses a transistor-level model of each listening multiplexer to accurately calculate its input capacitance based on configuration and type.

The metal capacitance of the wire is determined by its length, thickness, separation from its neighbors, and the metal layer where it is implemented. Quartus II software has a database with the precise capacitance of every routing wire on the device for use in power and timing analysis. These capacitances are extracted from device layouts and account for all physical and geometric effects.

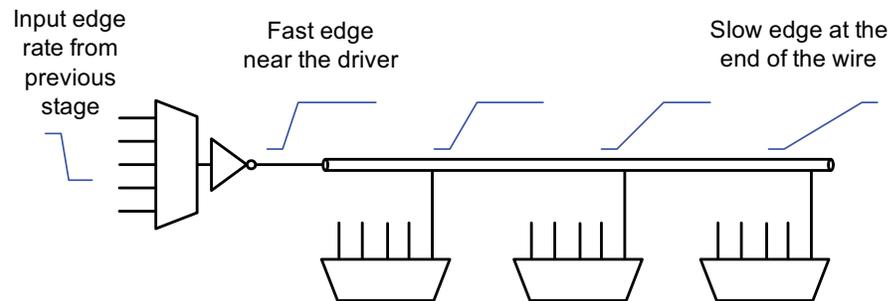
For most circuits, charging load capacitances is the dominant component of dynamic power. However, the FPGA routing fabric uses large inverters to drive long interconnect lines. These drivers can conduct significant short-circuit currents, so this effect cannot be ignored.

Short-circuit current occurs because switching signals cannot transition instantaneously—they have non-zero rise and fall times. During the transition, the pull-up and pull-down transistors of the inverter are both turned on for a period of time. Current flows directly from the supply to ground and is dissipated in the NMOS and PMOS transistors. Figure 8 shows the state of a switching inverter when its input is crossing through the half-supply point.

Figure 8. Short Circuit Current

For an inverter, power consumption due to short-circuit current scales roughly linearly with input transition time. Slower input transitions create a larger short-circuit window where both transistors are turned on, so more power is consumed. In an FPGA's programmable routing fabric, the transition time at the input to each buffer depends strongly on device configuration and physical wire parameters. Interconnect wires have significant distributed resistance and capacitance. As a transition propagates along a net, its edge rate is degraded by resistor capacitor (RC) filtering. Multiplexers listening to the wire add load capacitance along its length and worsen this effect, as shown in Figure 9.

Figure 9. Effect of Load Capacitance on Edge Rate



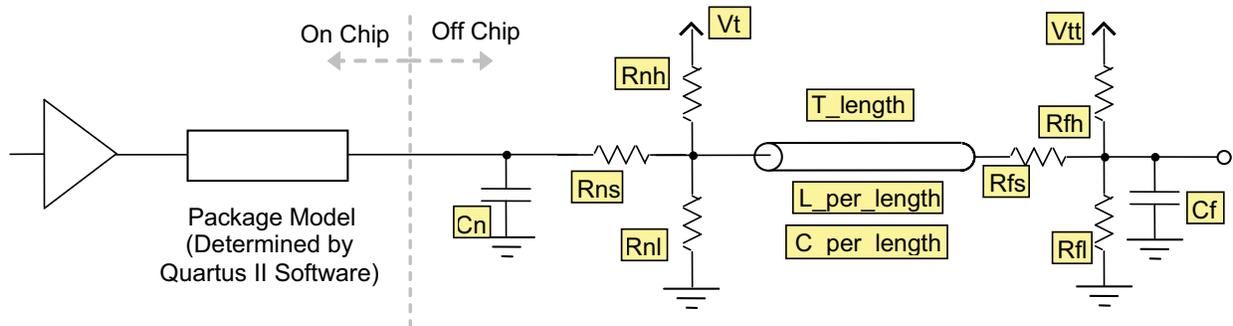
Determining accurate transition times at buffer inputs requires a detailed analysis of each wire. Physical wire parameters and loading effects (including the type and position of each load) must be considered.

During compilation, Quartus II software performs a transistor-level simulation of every routing path in the design using a fast internal SPICE-like simulator. The extracted capacitance and resistance of each wire are combined with information about the input capacitance and position of each listening multiplexer to determine the edge rate at each position along the net. Precise rising and falling transition times are calculated at the input to each routing switch. These waveforms are used as the input to subsequent simulations and accurate edge rates are propagated through the circuit. The total capacitive load seen by each switch is calculated based on the configuration of its fan-out. These values are used to accurately predict the short-circuit and capacitive switching power consumed in each routing element.

Accurate modeling of dynamic routing power is a critical step in the power analysis flow. The Quartus II PowerPlay power analyzer combines detailed device information and physical models with a sophisticated transistor-level simulation engine. The result is an accurate estimate of dynamic routing power that accounts for the numerous physical phenomena affecting the operation of deep-sub-micron VLSI circuits.

I/O Power Models

The I/O power model is another simulation-based power model with a very unique feature. With Altera's device families, such as Stratix III and Cyclone III FPGAs, the PowerPlay power analyzer does not simply model each I/O pin as having a capacitive load. Instead, it takes into account every possible parameter describing the off-chip board trace at each I/O pin, including relevant termination networks and transmission line effects, as shown in Figure 10.

Figure 10. Advanced I/O Power Board Trace Model

When the PowerPlay power analyzer performs advanced I/O power analysis, the entire board trace model is simulated using a sophisticated SPICE-like simulator built into the Quartus II design software. These simulations run for each I/O, allowing the PowerPlay power analyzer to calculate an extremely accurate power estimate specific to each individual customer's board design.

Empirical Dynamic Power Models

Empirical dynamic power models are based entirely on measured data. These models are used for blocks, such as embedded SRAM memories and embedded multipliers, that are too large to simulate in a reasonable amount of time, but have a small enough set of supported configurations that a parameterized measured model will suffice.

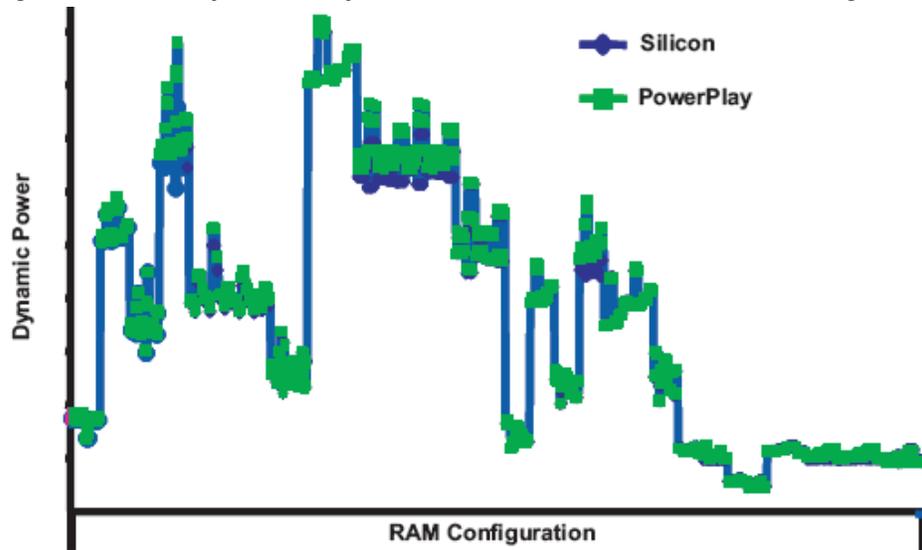
The development methodology is very straightforward and very accurate. The best way to accurately measure the power of a single block in a specific configuration in the FPGA is to configure the FPGA with all instances of a block measured in the configuration state under analysis. All other logic and functional blocks are configured for the lower power operating mode and are not stimulated. Then, well-designed and repeatable stimulus patterns are run through all instances of the block being measured to generate an understood power profile. The resulting power consumed by the chip is largely the result of the large number of blocks under test, and the excess power can be subtracted from the total power. The resulting power, divided by the number of blocks configured, gives an accurate view of power for that mode of that block.

Accuracy

Altera's PowerPlay early power estimator has the industry's most accurate models of the functional components within the FPGA. Because it is used before an RTL design is available, however, it lacks critical information such as logic configuration, placement, and routing, limiting its overall accuracy. The Quartus II PowerPlay power analyzer is a far more detailed power analysis tool that uses actual design placement and routing and logic configuration, and can use simulated waveforms to estimate dynamic power very accurately. On average, the PowerPlay power analyzer usually provides $\pm 10\%$ accuracy when used with accurate design information.

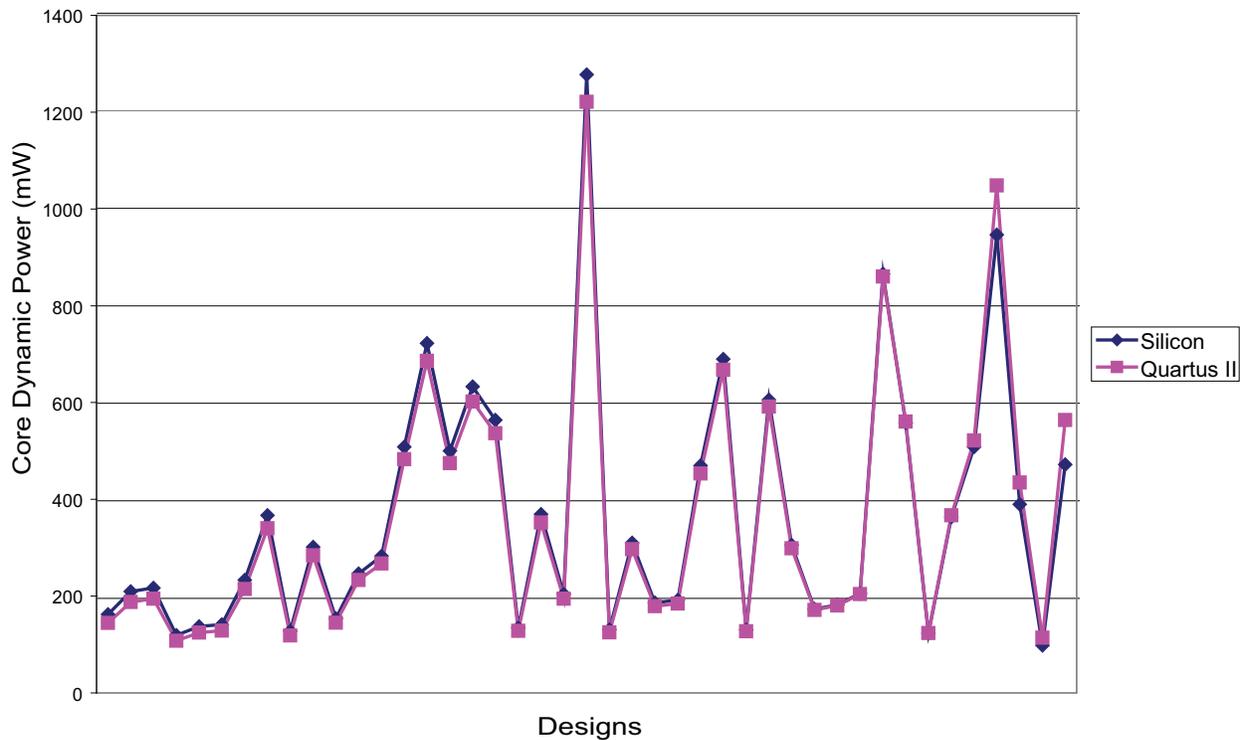
PowerPlay power analysis tools power models closely correlate to actual silicon measurements. Altera uses over 8,500 different test configurations to measure the power of individual blocks on a device (see [Figure 11](#)). Each configuration measures a single FPGA circuit component in a specific configuration.

Figure 11. PowerPlay Power Analyzer vs. Silicon Measurements for All RAM Configurations



In addition, Altera has built up an extensive suite of customer designs that are frequently used to test the overall accuracy of the PowerPlay power analyzer. These designs are compiled and simulated, and then the power is analyzed using the PowerPlay power analyzer. These power predictions are compared to actual silicon measurements (Figure 12), ensuring that the PowerPlay power analysis tools are not only accurate when analyzing specific blocks, but that they are also accurate when predicting power for designs that reflect what real customers are compiling.

Figure 12. PowerPlay Power Analyzer vs. Silicon Measurements for Customer Designs



Conclusion

Altera's PowerPlay early power estimator and the Quartus II PowerPlay power analyzer provide best-in-class tools to deliver accurate estimation of power consumption from early design concept through design implementation. These tools not only help designers verify that the design is within the power and thermal management budget, but also optimize designs for power. As process shrinks and increasing design complexity make power a more important issue for designers, the PowerPlay power analysis tools provide the most advanced power analysis tools for Altera FPGAs today.

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Document Revision History

Table 1 shows the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
December 2010	2.0	<ul style="list-style-type: none"> ■ Added Abstract. ■ Minor text edits. ■ Updated Figure 2 and Figure 6.
November 2007	1.0	Initial release.