White Paper

Optimizing Radar and Advanced Sensors Functions With FPGAs

Introduction

Modern warfare in urban and coastal environments depends heavily upon situational awareness. Soldiers in the air, at sea, and on the ground need to understand the environment around them and identify threats as early as possible.

State-of-the-art military sensors have unprecedented requirements in the volume of environmental data to be measured and processed. To handle this data and provide "actionable intelligence" to the soldier as soon as possible, sensor system logic requires optimized combinations of logic and digital signal processing (DSP) density, high-speed transceivers, power-versus-performance design flexibility, and high-assurance design flow to meet end-user requirements.

As shown in Figure 1, radar systems are used in many different platform sizes, both military and non-military. As more of these systems adopt array and conformal array technologies, the digital logic requirements of these systems will increase, and need to fit into smaller components and boards.

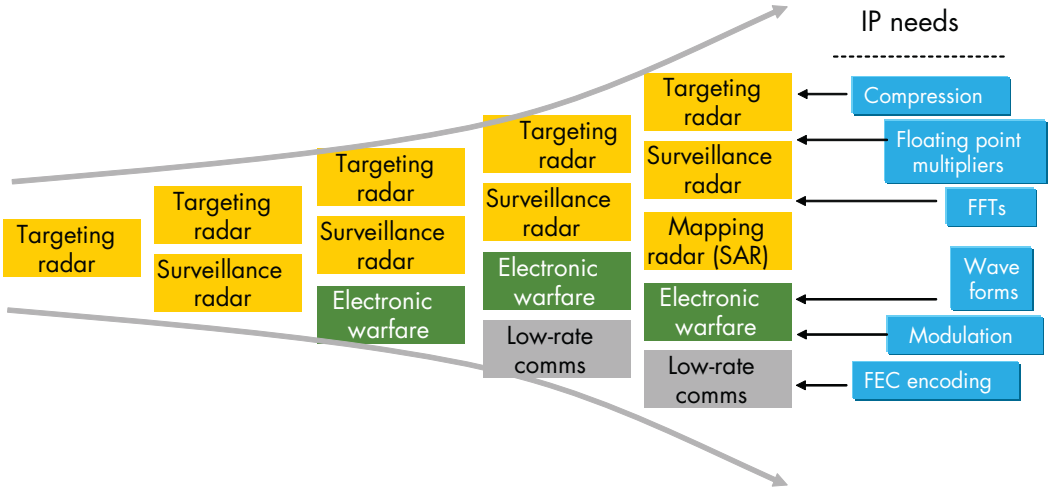
Figure 1. Radar Applications

Altera's simple and reliable tool flow, intellectual property (IP) library, and power efficient logic devices are highly advantageous to designers in the military-focused advanced sensor market.

Convergence of Military Electronics Systems

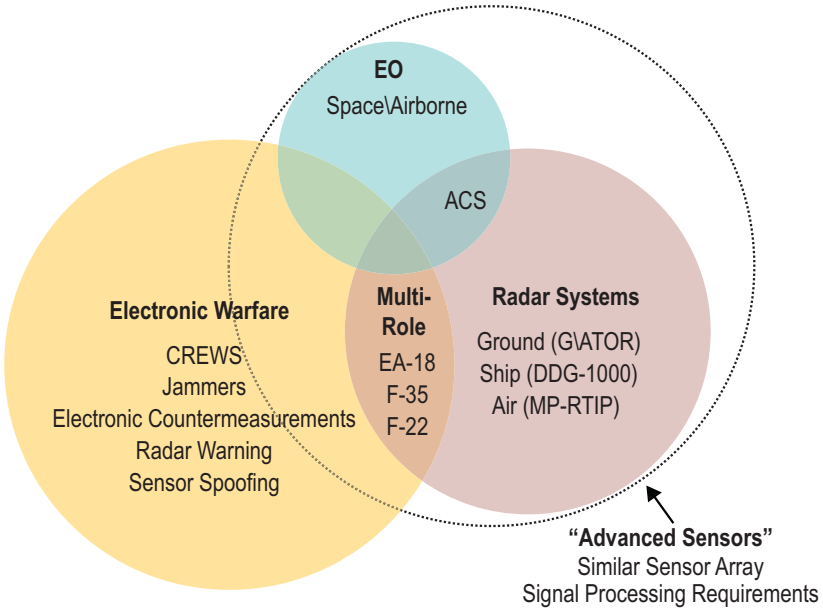
Military systems and vehicles traditionally have housed many separate electronic subsystems. Among the most sophisticated of these are targeting radar, surveillance radar, electronic warfare and countermeasures, imaging, and radio communications equipment. As shown in Figure 2, these functions have been converging in many military systems, utilizing multi-mode active electronically scanned arrays (AESA). This increases the digital- and state-logic requirements of the system significantly, and demands industry responses with more sophisticated fixed and programmable logic devices (PLDs).

Figure 2. Electronic Missions Converge in Military Systems



The markets for these individual military missions are beginning to overlap significantly (Figure 3). The capability to perform these activities in multi-role systems is enabled by the explosive growth in memory and semi-conductor capacity. Altera® FPGAs and structured ASICs play a significant part in this technology trend, with powerful and easy-to-use software and reliable compatibility with logic-design software partners. Extensive libraries of IP blocks are available to simplify these complex military designs.

Figure 3. Overlap in Military Electronics Markets



Other Technology Impacts

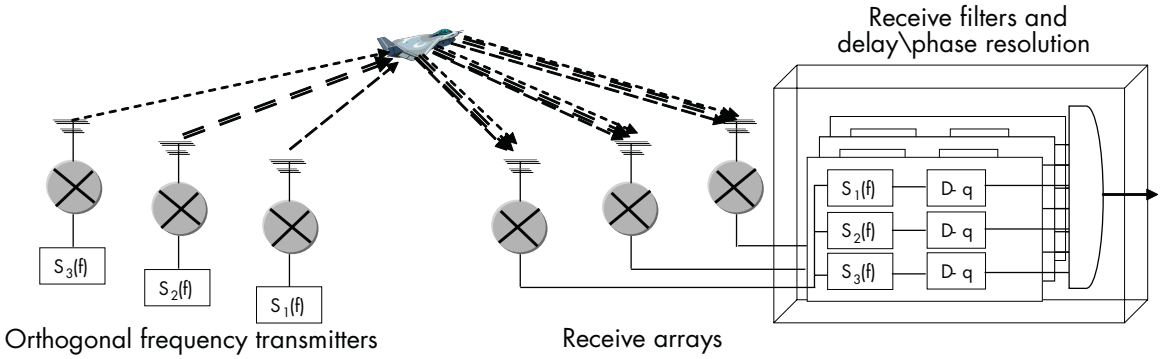
The proliferation of active arrays in sensors is the primary technology driver in logic device content. A larger number of array elements equals more design work, more beamforming algorithms, more integration and testing, and a longer logistics tail for the system.

In order to meet the diverse computing needs of military systems, Government customers have been investing in reconfigurable processors that can perform of both front-end and back-end processing. While some of these

technologies may yet see production use, programmable logic is an excellent interim design step for critical sensor requirements.

An exciting new dimension to sensor design is experimentation with multiple-input, multiple-output (MIMO) sensor arrays (shown in Figure 4). Receivers in a MIMO system perform phase-delay correlation between multiple orthogonal transmitted waveforms, exploiting advances in electronics density and computing capability. Developers who will lead in this market will be the ones that best take advantage of the most advanced and logic-intensive devices with the simplest design flow and most efficient compilation profiles.

Figure 4. MIMO Sensors



Making AESAs More Flexible

AESAs are a powerful technology for creating highly adaptive steerable beams able to track multiple targets or focus electromagnetic energy in one location. In order to take full advantage of a system's steering capabilities, designers work to move as much signal processing capability as possible into the forward radiating elements of the system. This may include waveform creation and compression, beamforming, correlation, and pre-processing. As more of these functions are performed in optimized, parallel FPGA logic, beamforming algorithms and waveform adaptivity can be accelerated, increasing reaction times in the system.

High-density Stratix® series FPGAs are the right tool for optimizing radar system performance. High logic density allows more functions in a single chip. Increased DSP elements streamline matrix mathematical functions and increase flexibility. Highly flexible 18x18-bit multipliers can be split into 9x9-bit elements, or combined into power- and logic-efficient 54-bit multipliers for floating-point operations. Altera's floating point operators have been tested and characterized for several high-performance applications.

Advanced Sensor Requirements

The challenges in military advanced sensor design are unique compared to other engineering fields. All of the design constraints of the commercial marketplace apply, plus sustainability, rigorous test and verification, and extended design and implementation life cycles that occur over the course of two or three generations of component technology. Some examples of these constraints are:

- *High serial data-streaming capacity:* Digital antenna technology moves analog-to-digital conversion closer to the receiver, and requires more signal resolution in order to perform digital filtering.
- *Complex math operations:* Signal pre-processing and matrix operations require large numbers of DSP block elements to assume the roles traditionally filled by digital signal processors.
- *Sensitivity to heat dissipation:* Sensor systems often have a long, if not continuous, mission life, requiring the dissipation of heat from continuous operation.
- *Logic density for multi-role electronics:* With so many military missions being performed with the same array, logic requirements are extremely high in transmit and receive electronics.

- *Speed and latency performance:* The speed grade and latency of the logic devices in a sensor array, as well as all the latency of interfaces between logic devices, affect the reaction times and beamforming algorithm performance.
- *Parts availability:* Sensor systems are very complex, and the impact of even one part received behind schedule can have expensive consequences for the rest of the system.
- *Tool-flow ease of use:* As millions of logic elements (LEs) are integrated into a system design, the design, compilation, and test of large pieces of logic code is a substantial driver of both cost and schedule.
- *Signal integrity:* As more receiver elements provide data to be correlated with one another in final processing, small signal errors have larger impacts on sensor algorithms. Signal integrity in digital components is therefore paramount.

High-Speed Serial I/Os

Military sensor systems use a variety of high-speed serial interfaces (see Table 1) to handle the large volumes of data generated in the transmit\receive element. Altera provides internal and partner solutions for the majority of these protocols, as well as the proprietary SerialLite II standard for minimal overhead and latency.

Table 1. Standard and High-Speed Interface Protocol Support With Altera and Partners

Interface Type	Protocols
Communications	Packet over SONET (POS)
	PHY 2/3
	SPI-4.2
	SONET
	8b/10b
	Utopia
	High-Level Data Link Controller (HDLC)
	Cyclical redundancy check (CRC)
Ethernet	10/100/1000 Mbps media access control (MAC) and physical coding sublayer (PCS)
	10G MAC and PCS
	1588 Industrial Ethernet
	Any speed MAC
High Speed	RapidIO®
	HyperTransport™
	SerialLite II
	Multi-Gbyte fibre channel
PCI	32-/64-bit PCI
	PCI-X
	PCI Express /1, /4, /8
Serial	USB 2.0 function
	I²C
	CAN
	MediaLB
	SATA
Video	Serial Digital Interface (SDI)
	Asynchronous Serial Interface (ASI)

Altera's internally developed SerialLite II protocol has several features that are attractive for military sensor design, including:

- 1X to 16X speeds, up to 6.375 Gbps
- Very low latency and efficient LE implementation
- Support for non-reciprocal speed and half-duplex throughput requirements, ideal for one-way sensor streaming

High-speed sensor data-streaming products, like the upcoming Curtis Wright Controls® FibreXtreme Serial FPDP (ANSI/VITA 17.1-2003) data link, utilize Altera FPGAs for high-reliability serial interfaces with proven signal integrity and high data rate performance.

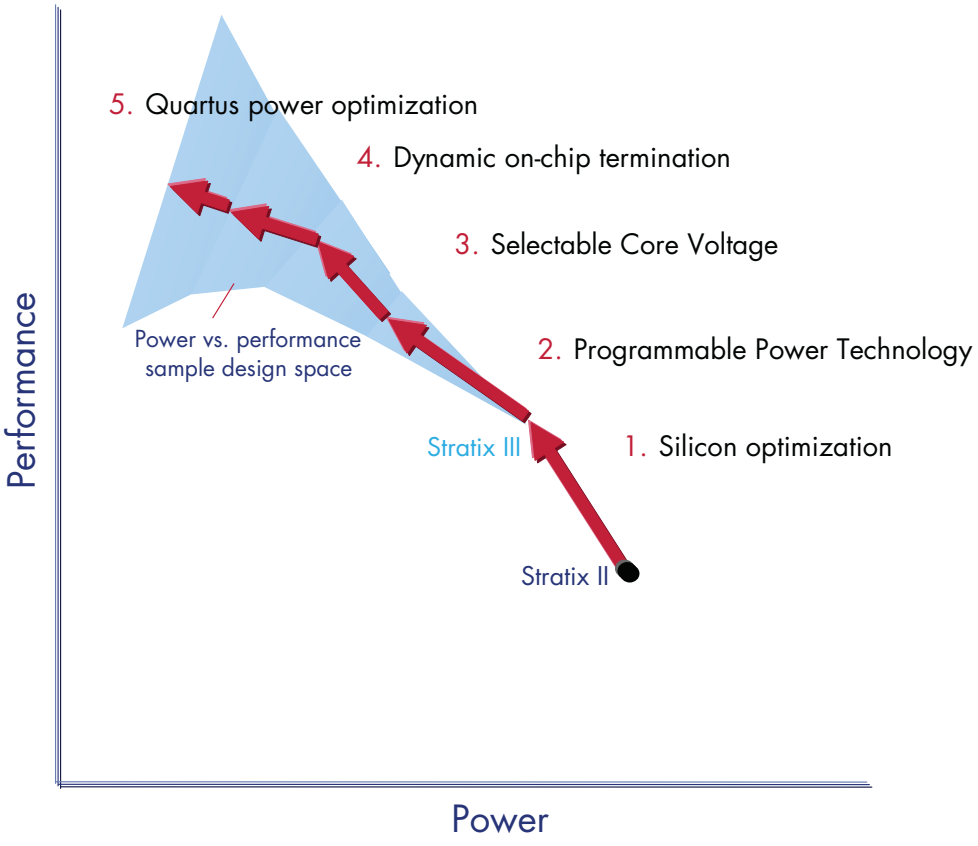
Power and Heat Advantages

Military users are demanding more radiating elements in sensor arrays in order to increase flexibility and precision, and want this increased sensor capability without increased system size or weight. This means more compact sensor electronics, complicating power and heat dissipation requirements.

Never before have system designers had such direct control over the power consumption and heat dissipation of their programmable logic. The Altera design flow offers five advantages for selecting the optimal balance of power and performance in a system. Altera's patented Programmable Power Technology allows the designer to channel power to the critical logic path where it is needed, and to reduce power where it is not needed. The designer can select between 0.9V and 1.1V FPGA core voltage, trading between power and performance. In addition, the powerful Altera Quartus® II design system has two new features: the intelligence to terminate unused power connections dynamically, and the ability to optimize power routing.

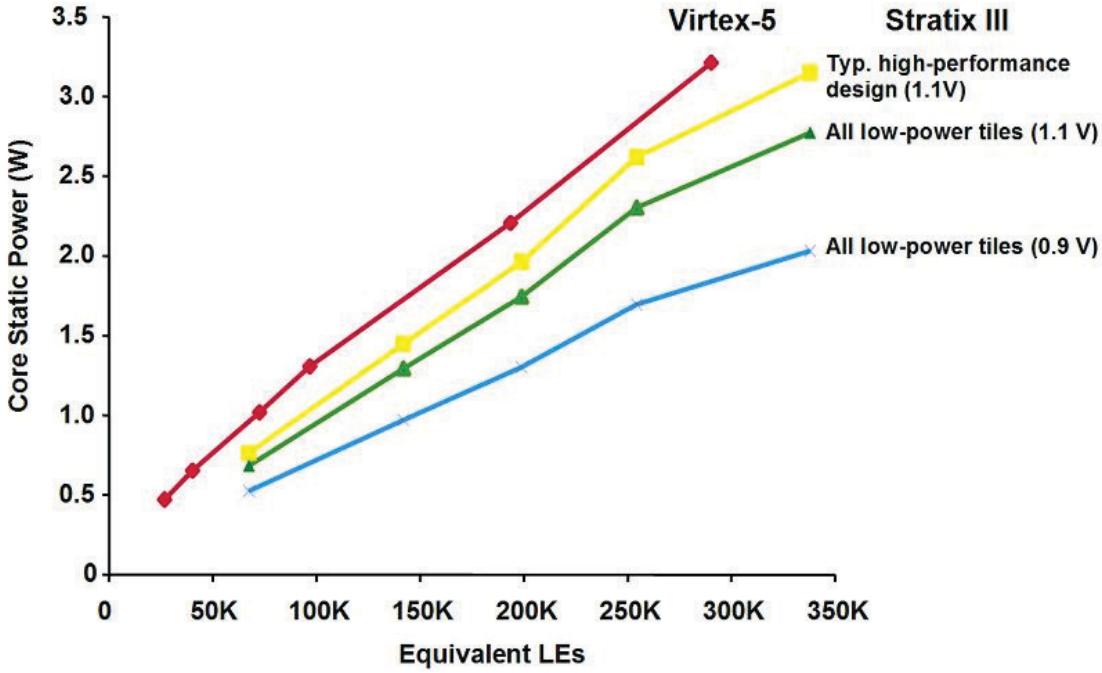
As shown in Figure 5, an FPGA designer has a flexible design space to tailor an application for both power and performance requirements.

Figure 5. Five Ways Military Designers Can Optimize Designs for Power and Performance



For the 65-nm technology node of FPGAs (Stratix III and Virtex-5), Figure 6 shows the power-per-equivalent-LE curves. Stratix series FPGAs offer better power efficiency at the high-performance point, with the opportunity to lower power even further based on system requirement trade-offs. Power savings can be as high as 23 percent for designs with 1.1V core voltage, and up to 40 percent when utilizing the 0.9V core voltage.

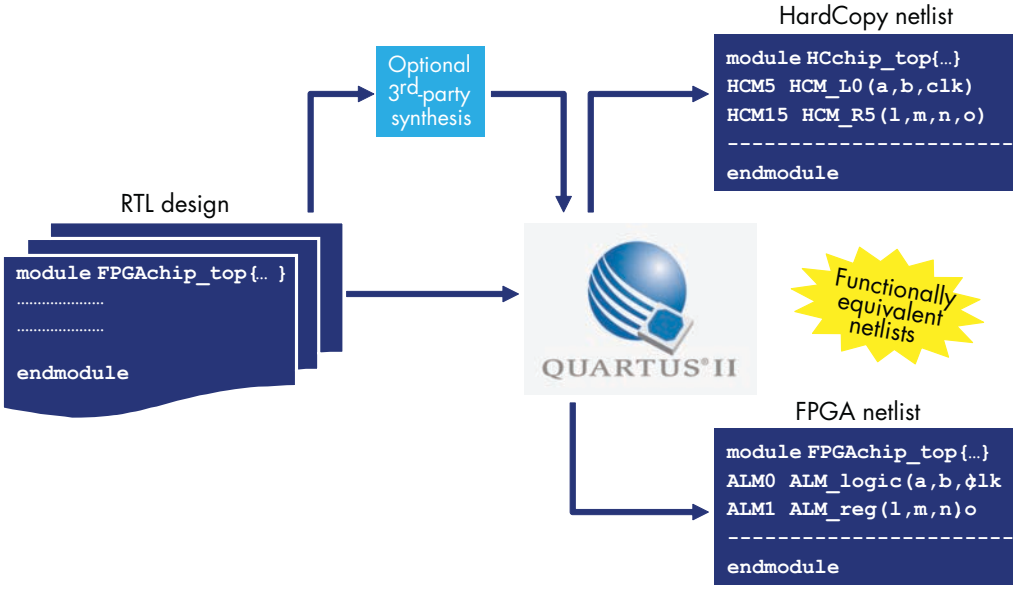
Figure 6. Typical Power Curves for Stratix and Virtex Series FPGAs



System Prototyping With FPGAs—Move to ASIC With Zero Risk

Another opportunity to reduce power in sensor systems is to transition the digital logic in the system from a Stratix series FPGA to a HardCopy® structured ASIC (Figure 7). The decision to transition to ASIC can be made well into prototype design, with no a priori engineering planning or investment. This transition can be made as part of a product improvement, engineering change proposal, or production proposal.

Figure 7. Quartus II Software Enables Designers to Transition Quickly From FPGA to Structured ASIC



As shown in Table 2, this allows designers to reduce dynamic and static power in their programmable logic by up to 90 percent and 50 percent respectively. This can be done with minimal non-recurring engineering (NRE)—about 20 percent of ASIC design costs, with virtually no schedule or technical risk. The power reduction allows sensor systems to accelerate performance and continue to improve tactics and scanning algorithms well into initial production.

Table 2. Seamless Migration to Lowest Power Solution

Requirement	HardCopy Structured ASIC Solutions
Low Power and Heat	Up to 90% lower static power and up to 50% lower dynamic power than FPGAs
High Density and Performance	Up to 2.2M LEs and 1.4M DSP blocks
	Up to 2X FPGA performance
Low Technical and Schedule Risk	From FPGA design to structured ASIC in about 20 weeks with zero risk
Other Features and Functionality	Single event upset (SEU) immunity
	NRE about 20% of traditional ASIC design
	International Trade in Arms Regulations (ITAR)-compliant design and manufacturing flow
	Design can be pin-compatible with FPGA

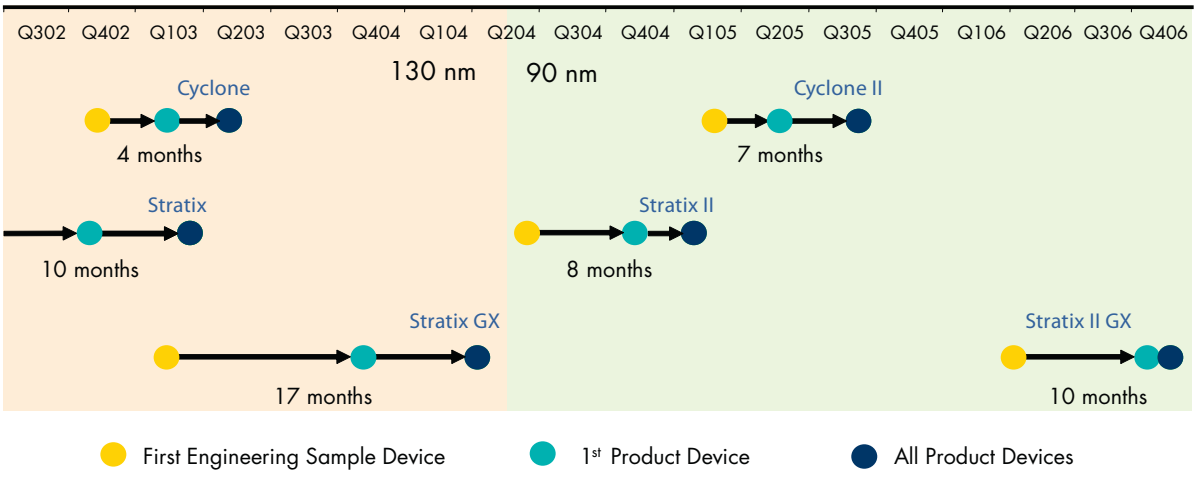
When designing with Altera FPGAs and the Quartus II design software, there is always an opportunity to trade-off between retaining the flexibility and reprogrammability of an FPGA, or significantly reducing the heat dissipation of the programmable logic in the system with a structured ASIC. This is a powerful design option for meeting stringent system power and cooling requirements in military sensors.

Parts Availability

The development of military systems with complex sensors tends to be among the most difficult projects to manage. Dozens of technologies are integrated, some of which are untested beyond initial prototypes.

Historically, Altera has delivered all FPGA devices on time or ahead of schedule (see Figure 8). Release schedules for the most recent generations of low-power Cyclone® III and flexible, logic-dense Stratix III FPGAs are likewise proceeding flawlessly to early customers. By using Altera PLDs in radar and advanced sensor systems, program managers significantly reduce technical and schedule risk, allowing them to focus on their hard technical problems.

Figure 8. Altera's Product Release History Includes 100% On-Time Delivery

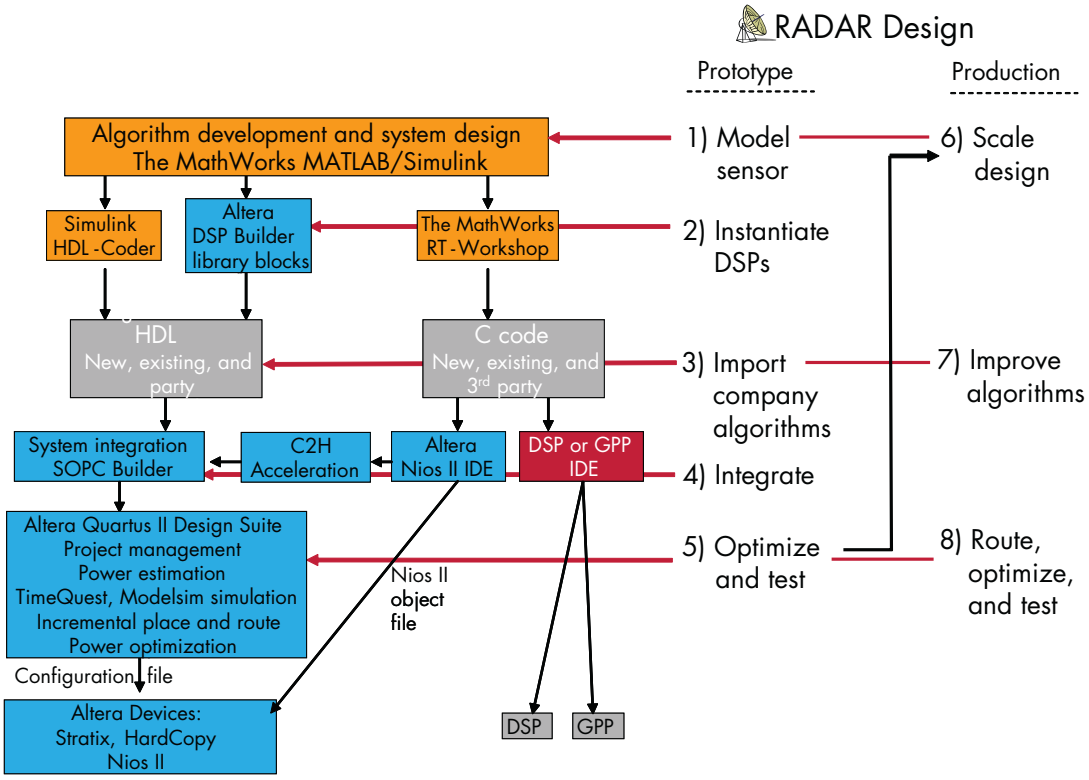


Simplified Design Flow

The complexity of radar and advanced sensor system design is increasing almost exponentially. Designers need tools that reduce compile times, manage design risk, and streamline test and verification time, yet still offer powerful DSP design features.

Getting started on Altera design tools is easy—Altera's Quartus II development software is the only design solution that includes everything a designer needs for the entire cycle of FPGA and ASIC design for radar and advanced sensor systems. As shown in Figure 9, Quartus II software includes DSP Builder block set support for The MathWorks MATLAB, SOPC Builder, Power Estimator, Incremental Place and Route, Power Optimizer, and TimeQuest timing analyzer.

Figure 9. The Altera Design Tool Flow is Easy to Use, With Low Start-Up Cost



Many advanced sensor algorithms are designed and simulated in The MathWorks MATLAB. From here, designers have the capability to transition the entire design into HDL using Simulink and Altera's DSP Builder tool.

SOPC Builder is the next tool in the value chain for sensor design. Utilizing Altera's proprietary Avalon® interface, SOPC Builder easily integrates several partitioned logic systems together, automating interface protocols and bit widths. SOPC Builder is an excellent tool for encapsulating company IP for reuse from one product design to another. The Quartus II design suite includes all of the other tools needed to optimize HDL design for implementation on silicon.

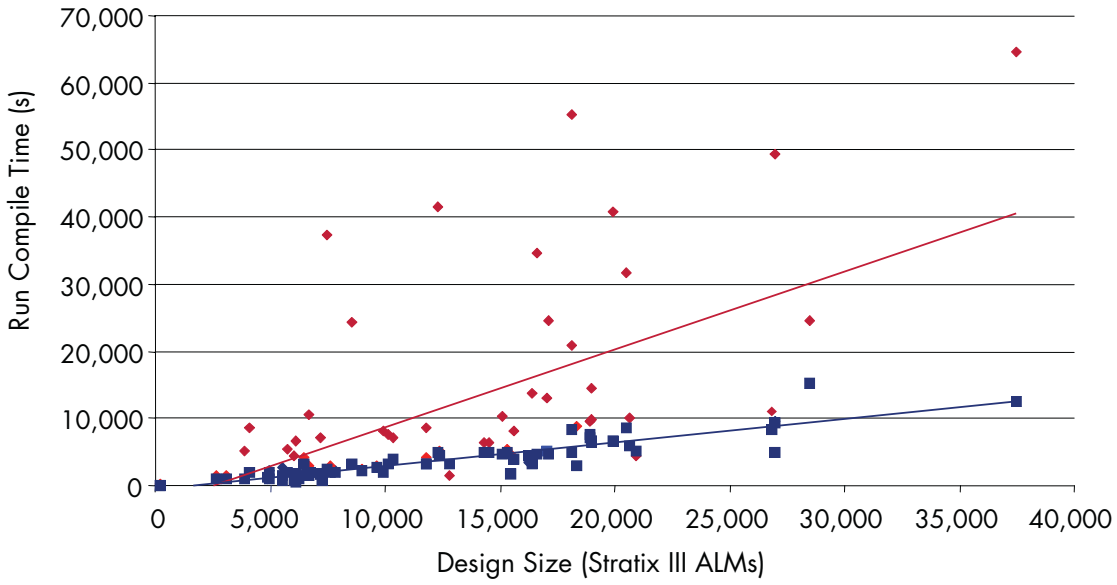
There are numerous features (shown in Table 3) in the Quartus II design suite that improve compile time performance in advanced sensor design. The primary differences between Quartus II development software and Xilinx compiler software are memory requirements and compile times: Quartus II software requires up to 50 percent less memory to compile chip designs, and has much lower compile times (see Figure 10).

Table 3. Altera Design Flow Advantages for Advanced Sensor Systems

Requirement	Altera Design Solution
DDR3 Memory	Quartus II software in combination with 65-nm FPGAs are the only benchmarked design solution to support DDR3 memory, with twice the density and 50% more bandwidth than DDR2.
Timing Support	Only the TimeQuest Timing Analyzer offers native support of Synopsis Design Constraint (SDC) standard for timing analysis.
Fast Compile Times	Common design benchmarks show Altera designs compile twice as fast as the nearest competitor at 65 nm.
	Only Quartus II software supports multi-CPU processors, complete with performance-increase benchmarks
	Quartus II software is the only design software with full 64-bit support on the Windows OS, supporting more memory (>2 Gbytes) for faster compile times.
	Altera's simple design partitioning allows for incremental compile and reduction in recompile time by up to 70%.
Power Analysis and Programmability	The Quartus II Power Analyzer provides trusted power estimates with unbiased consistency (8% mean error).
	Quartus II software is the first PLD design software to give the designer control over FPGA dynamic power.
Large Selection of Signal Processing and Serial Interface IP	Scalable, reversible fast Fourier transform (FFT)\inverse FFT (IFFT) with bit-exact C models
	Floating-point math support and compiler

In addition to the savings-by-design of Quartus II software, options for decreasing compile times include 64-bit Windows OS support, multiple processor support, and incremental compile. These features allow designers to segment large projects at inception into smaller, more easily compiled sections that can be integrated together in system integration with a streamlined compile flow. Figure 10 shows the resulting compilation time savings.

Figure 10. Compile Times of Stratix III vs. Virtex-5 FPGAs Using Identical Designs



Signal Integrity on Digital Interfaces

Signal integrity is an important performance issue for FPGAs, as well as all other signal propagation devices in a military sensor system. Very small differences in signal error can have highly magnified effects when propagated through array processing algorithms. Therefore, reliable, all-temperature, low error-rate performance is needed to take advantage of the extensive engineering efforts that make up modern sensor systems.

Signal integrity in Altera FPGAs (see Table 4) is by design—both in silicon and in FPGA packaging. On-chip termination improves power performance as well controlling stray voltage, improving signal integrity. Output delay control, on-die capacitors, and slew rate controls likewise improve stray electromagnetic effects that cause signal imbalances. Altera packaging is also designed for enhanced signal reliability by using on-package capacitors and optimized pin geometries.

Table 4. Significant Signal Integrity Advantages of Stratix Series FPGAs

	Significant Features	Benefits
Silicon	Adjustable slew rate control (4 settings)	Reduce $\partial i / \partial t$
	Advanced on-chip termination	Proper termination
	Staggered output delay control	Reduces SSN
	On-die capacitors	Improves PDN quality
Package	On-package decoupling capacitors	Reducing loop inductance reduces SSN
	8:1:1 I/O:GND:PWR ratio (Maximum distance between I/O and GND = 1)	Improves PDN quality

Conclusion

Designers of military radar and advanced sensors are among the most sophisticated and demanding in the field of programmable logic. They have the most design constraints, the longest design cycles, and the largest design management needs because of large engineering and verification teams. The Altera Stratix series of FPGAs and Quartus II design flow offer real solutions to each of these design problems and constraints. From speed and latency, heat dissipation, parts availability, FPGA-to-ASIC design flow, to lean compile times, Altera products offer advantages that are too great to ignore during architectural design.

Further Information

- Altera's Military Radar web page:
  www.altera.com/end-markets/military-aerospace/radar/radar
- *Designing and Using FPGAs for Double-Precision Floating-Point Math*:
  www.altera.com/literature/wp/wp-01028.pdf

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