White Paper

Reduce Total System Cost in Portable Applications Using Zero-Power CPLDs

Introduction

Traditionally, portable system designers have used ASICs and ASSPs to implement memory interfaces, I/O expansion, power-on sequencing, discrete logic functions, display, and other functions in portable systems. Cost limitations, power and cooling restrictions, and board space requirements often limit the use of programmable logic devices in these applications. Today, however, innovations in CPLDs in power reduction, cost optimization, and small form-factor packaging allow programmable logic devices to replace or augment ASICs, ASSPs, and discrete devices in portable applications.

Owing to their look-up table (LUT)-based architecture and innovative approaches to cost and power optimization, the latest zero-power CPLDs offer features and capabilities not found in older, macrocell-based predecessors, including:

- Highest logic density per board area
- Highest I/O count per board area
- On-chip voltage regulator and oscillator
- Auto power-down and auto power-up

Due to their very low cost and differentiating features, these CPLDs offer portable system designers, on average, 50 percent lower cost and power than older CPLD solutions. As a result, they are being adopted by product developers to deliver the time-to-market and flexibility benefits that ASICs and ASSPs cannot deliver.

Portable System Challenges

Portable applications are proliferating as demand increases for small, inexpensive products that support high levels of functionality with extended battery life. Table 1 lists some end markets and products for portable applications.

Table 1. Portable Markets and Applications

Markets	Applications
Consumer and Automotive	• Mobile communication handsets • Educational toys • Portable media players • Mobile GPS and navigation • E-paper readers • Digital cameras • Mobile computing • Automotive dashboard connectivity • Conditional access cards
Industrial	• Barcode scanners • Industrial PDAs • Camera modules • Point-of-sale terminals • Remote/wireless metering • I/O modules
Medical	• Handheld diagnostics • Patient monitoring and treatment
Test and Measurement	• Handheld testers • Multimeters
Communications	• Customer premises equipment (CPE) • Wireless network • Optical modules

The drive to support higher levels of functionality in portable systems is on the rise, even as the demand to reduce the size and cost of these systems increases, thus posing a significant challenge for system designers. Many of the most common functions required by portable applications are implemented using discrete components, which drives up board space, cost, and power consumption. These components and functions include:

- Power up and down sequencing
- Clock distribution
- Discrete logic devices for voltage level translation
- I/O expansion
- Battery monitoring/charging
- Display control
- Keyboard/keypad interface
- Protocol bridging and translation
- Memory management
- Touch-screen decoding

Zero-Power CPLDs Reduce Total System Cost and Board Space

In portable applications, the functions listed above are often implemented using ASICs, ASSPs, and other discrete devices. However, all of these functions can be integrated into zero-power CPLDs. The latest zero-power CPLDs offer very high logic capability in ultra-small form-factor packages, making them ideal for functions that require high I/O count per board area, such as interfacing with an LCD display, keypad, flash, touch screen, or memory in portable applications. In addition, they also provide a high logic-to-board area ratio, which is needed for integration of discrete components to minimize PCB space.

For example, Altera® MAX® IIZ CPLDs are offered in four low-cost Micro FineLine BGA (MBGA) (0.5-mm pitch) packages. Ideal for portable applications, the small form-factor 68-pin, 100-pin, 144-pin, and 256-pin 0.5-mm MBGA packages enable the system designer to pack more functionality into less board space so as to develop smaller products without sacrificing device functionality. Figure 1 shows the footprints of these packages.

Figure 1. 0.5-mm MBGA Package Footprints

These small form-factor packages offer the compact size of a 0.5-mm BGA with the easy breakout of a partially populated array. The 68-pin, 100-pin, and 256-pin packages are designed so that all pins and power connections can be broken out with only two layers of the PCB using Micro Via PCM layout rules. (The 144-pin package requires four layers.)

Besides saving board space, ultra-small form-factor packages lower total system cost by enabling system designers to integrate more user I/Os and logic density per board area (mm^2). Table 2 shows a comparison of the I/Os per mm^2 and macrocells per mm^2 of some CPLD families. The small form-factor packages on MAX II CPLDs offer up to three times more I/Os per board area (mm^2) and over seven times more logic density per board area (mm^2) than comparable macrocell-based packages.

Table 2. I/O per mm² and Logic Density per mm² Comparison of CPLD Families

Vendor	CPLD Family	Device	Package	Size (mm)	I/Os	Equivalent Macrocells	I/Os per mm²	Macrocells per mm²
Altera	**MAX IIZ**	**EPM240Z**	**M68**	**5x5**	**68**	**192**	**2.72**	**7.68**
Altera	**MAX IIZ**	**EPM240Z**	**M100**	**6x6**	**80**	**192**	**2.22**	**5.33**
Xilinx	CoolRunner-II	XC2C64	CP56	6x6	45	64	1.25	1.78
Lattice	ispMACH 4000Z	4064Z	CS56	6x6	32	64	0.89	1.78
Lattice	ispMACH 4000Z	4064Z	CS132	8x8	64	64	1.00	1.00
Altera	**MAX IIZ**	**EPM240Z**	**M68**	**5x5**	**68**	**192**	**2.72**	**7.68**
Altera	**MAX IIZ**	**EPM240Z**	**M100**	**6x6**	**80**	**192**	**2.22**	**5.33**
Xilinx	CoolRunner-II	XC2C128	CP132	8x8	100	128	1.56	2.00
Lattice	ispMACH 4000Z	4128Z	CS132	8x8	96	128	1.50	2.00
Altera	**MAX IIZ**	**EPM570Z**	**M100**	**6x6**	**76**	**440**	**2.22**	**12.22**
Altera	**MAX IIZ**	**EPM570Z**	**M144**	**7x7**	**116**	**440**	**2.37**	**8.98**
Xilinx	CoolRunner-II	XC2C256	CP132	8x8	106	256	1.66	4.00
Lattice	ispMACH 4000Z	4256Z	CS132	8x8	96	256	1.50	4.00

The high logic density of the MAX IIZ devices allows designers to reduce the total number of board components, which also reduces total system cost. MAX II devices also support a low-frequency internal oscillator that can eliminate the need for external clock sources for power-up sequencing or event timers and keyboard encoders.

Table 3 shows a comparison of the costs and benefits of some ASSP, discrete device, and CPLD solutions used in typical portable applications. MAX II CPLDs reduce the total solution cost of the portable system, as they offer programmable logic resources that integrate other board functions, reducing board space and system complexity. Also, MAX II CPLDs are a better alternative to ASSPs and discrete devices as they are not prone to obsolescence.

Table 3. Comparison of Altera MAX II CPLD-Based and Discrete-Based Functions in Portable Systems

Solution	CPLD Density (MCs)	Voltage Regulator	Frequency Oscillator	BOM Flexibility *(2)*	Obsolescence	Approximate Solution Price *(3)*
Altera MAX II EPM240M100C5	192	✔	✔	✔	✔	$4.80
Microchip PIC16F883-I/SP + TI TPS79118DBVR (LDO) + TI SN74AHC1G00DBVR (voltage translator) + TI PAL16R4 (I/O expander)		✔	✔			$4.45
FTDI 245RL (ASSP) + TI TPS79118DBVR (LDO) + TI PAL16R4 (I/O expander)		✔				$4.76
Non-Altera CPLD *(1)* + TI TPS79118DBVR (LDO) + Microchip PIC12F683-E/SN-ND (power-up sequence controller)	128-256	✔	✔	✔	✔	$8.00-$16.50

Notes:

(1) An example of a non-Altera CPLD is the Xilinx XC2C128CP132-7C (priced at $7.31 for 1000 units)

(2) BOM flexibility is the ability to work with multiple/different suppliers (e.g., display, flash, or A/D converter suppliers)

(3) Pricing based on 1000-unit list price

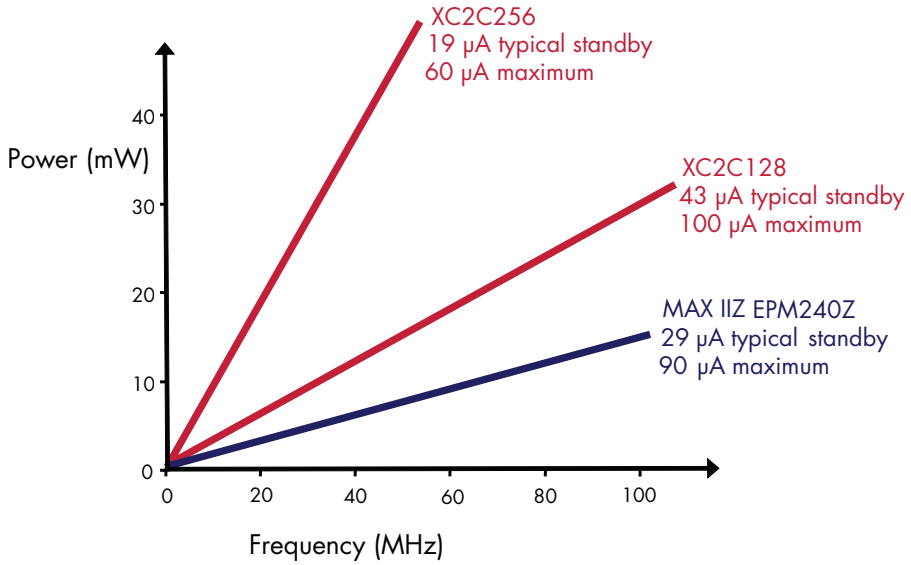
Reduced Power Consumption Lowers Costs

Power consumption is another challenge that portable design engineers face. Consumers demand smaller products with more features, but also want extended battery life to meet their mobile lifestyles. Power dissipation consists of dynamic and static components, and reducing both of these can extend the battery life. Reduced power consumption

improves overall product costs by requiring lower-cost batteries and/or power supplies to achieve the desired operating time.

MAX II devices have many power system characteristics that are beneficial for portable applications. MAX II devices deliver the lowest dynamic power in the CPLD industry and offer a power-down capability that conserves battery life. The typical standby current draw of MAX IIZ devices is only in the tens of microAmps, the lowest power consumption per macrocell or per I/O of any CPLD. Figure 2 shows the system power curves for the MAX IIZ device compared to those of two CoolRunner-II devices. The red line for the CoolRunner-II devices represents their power consumption across operating frequency, and the blue line represents the power consumption of a comparable MAX IIZ device. Also shown are the typical and maximum standby current draw for each of the devices.

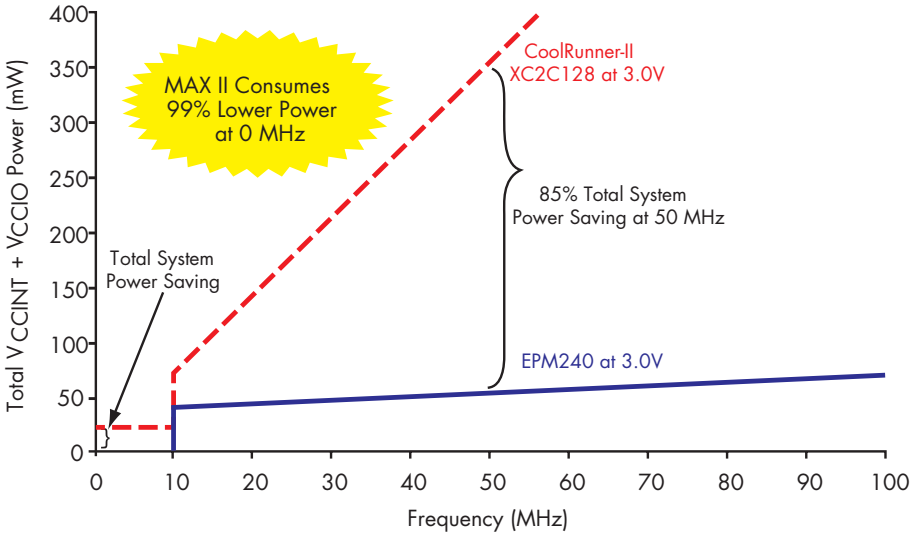
Figure 2. MAX IIZ vs. CoolRunner-II: Dynamic and Static Power Consumption



In addition to offering the lowest standby power, MAX IIZ CPLDs feature an easy-to-use power-down capability that enables portable system designers to achieve zero power at 0 MHz. Unlike competing CPLDs, the superior power system characteristics of MAX II CPLDs—such as hot-socketing support—enable them to be completely powered down without any power-sequence restrictions, thereby conserving battery power when the portable system is not in use.

Figure 3 shows the ability of the MAX II device to achieve zero power at 0 MHz when completely powered down. The application example assumes 50 percent of inputs are stuck at V_{CC} and 50 percent are at GND when the CPLD's V_{CCINT} and V_{CCIO} are powered down. As illustrated, the leakage current through the I/O pins on the CoolRunner-II device results in greater power dissipation when the device is "off" compared to when the MAX II device is "off." Multiple I/Os at V_{CC} or GND have very little or no effect on the MAX II device's power dissipation when it is turned "off." Older CPLD devices cannot be turned "off" to save power unless every input from all parts of the circuit is guaranteed to be "off," but MAX II devices have no such requirement.

Figure 3. MAX II vs. CoolRunner-II: Power Down Mode in Portable System



It is critical that a portable system with multiple power domains have a very flexible control mechanism and that each domain be very easy to power up and power down. Power transitions are also important, as a typical power management system is constantly transitioning from one power mode to another. Depending on the hot-socket characteristics of a device, it might consume more power parasitically in the "off" state than in the "on" state, due to poor hot-socket characteristics.

The main hot-socket concern is the I/O pin leakage when power is not applied to the PLD. Hot-socket leakage is the current leakage of an I/O pin at V_{CC} or GND when the device V_{CCIO} or V_{CCINT} is not applied. Hot-socket leakage can cause system power dissipation through an I/O pin even when the device is powered down. MAX II devices offer hot-socket support with very low static hot-socket leakage. The hot-socket feature removes some of the difficulty that designers face when using components on PCBs that have a mix of 3.3V, 2.5V, 1.8V, and 1.5V devices that are powered down in different modes. In a portable system, hot-socket support facilitates power-down of sections of the system without unwanted parasitic leakage paths through the CPLD I/O pins.

Conclusion

MAX II CPLDs offer several key benefits over ASIC, ASSP, discrete, and other CPLD devices. The ultra-small form-factor packages combined with the high-density, core voltage regulator, and internal frequency oscillator features, allow system designers to integrate existing discrete devices on a board, reducing total system cost and minimizing board space. In addition, MAX II CPLDs enable the system designer to not only reduce system power consumption, but also to simplify system power management in the end product. For most portable applications where ASICs, ASSPs, and discrete devices are traditionally used, MAX II CPLDs' low total solution cost provides a compelling argument for replacing or augmenting these devices.

Additional Resources

- More about MAX IIZ CPLDs:
  www.altera.com/MAXII
- MAX II Power-Down Design:
  www.altera.com/support/examples/max/exm-power-down.html
- Portable Applications Using MAX II Devices:
  www.altera.com/max2-portable
- *AN 422: Power Management in Portable Systems Using MAX II CPLDs:*
  www.altera.com/literature/an/an422.pdf
- *AN 114: Designing With High-Density BGA Packages for Altera Devices:*
  www.altera.com/literature/an/an114.pdf
- *Six Ways to Replace a Microcontroller With a CPLD:*
  www.altera.com/literature/wp/wp-01041-six-ways-to-replace-microcontroller-with-cpld.pdf
- *Using Zero-Power CPLDs to Substantially Lower Power Consumption in Portable Applications:*
  www.altera.com/literature/wp/wp-01042-using-zero-power-cplds-to-lower-power-in-portable.pdf
- *Using LEDs as Light-Level Sensors and Emitters:*
  www.altera.com/literature/wp/wp-01076-led-driver-reduces-power-adjusting-intensity-ambient-light.pdf

Acknowledgements

- Martin S. Won, Senior Member of Technical Staff, Customer Success Programs, Altera Corporation

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