White Paper

Signal Integrity Comparisons Between Stratix II and Virtex-4 FPGAs

Introduction

Signal integrity has become a critical issue in the design of high-speed systems. Poor signal integrity can mean increased engineering costs, delayed product releases, and even lost revenues. The opportunity cost of ignoring signal integrity can easily reach millions of dollars, given the importance of time-to-market in today's semiconductor marketplace. The onus on sound signal integrity inevitably falls on the choice of FPGA in high-speed systems.

This white paper describes competitive benchmarks between Stratix® II and Virtex-4 FPGAs demonstrating a 2X signal integrity advantage for Stratix II FPGAs. This paper also describes the Altera design process to deliver industry leading signal integrity and the resulting technology within Stratix II FPGAs that enable this significant advantage.

Poor signal integrity can arise due to issues at three design levels:

- Chip level - improper I/O buffer design, inadequate return current paths, etc.
- Package level - high package inductance, mismatched traces, improper routing, inadequate return current paths, etc.
- Board level - Crosstalk, reflections, signal attenuation, EMI/EMC, etc.

Chip level and package level signal integrity are entirely the result of the integrated circuit and package level design from the chip manufacturer. Board level signal integrity issues result from the combination of the quality of the chip and package as well as the customers board level design. The burden of board level design and the resulting system performance can be optimized through higher quality signal integrity within the chip and package.

Signal Integrity Benchmarks

Three sets of comparisons between Stratix II and Virtex-4 I/O signal integrity are described in this document, covering LVDS at 1Gbps and 1.3 Gbps and HSTL at 660 Mbps. In order to determine the relative signal integrity performance between Stratix II and Virtex-4 FPGAs, simulations using IBIS I/O models from each vendor were performed. In addition, simulations verifying the correlation of Altera's Stratix II IBIS models versus lab measurements are shown to validate the Altera simulation results. The Virtex-4 IBIS models were downloaded directly from the Xilinx web site and are assumed to be accurate. See Figure 1.

Figure 1: Simulation Setup for Measuring LVDS Eye Diagram for Stratix II and Virtex-4 FPGAs

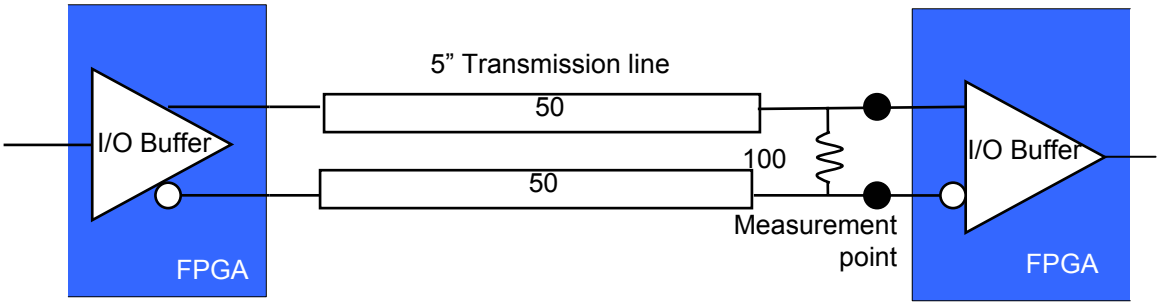


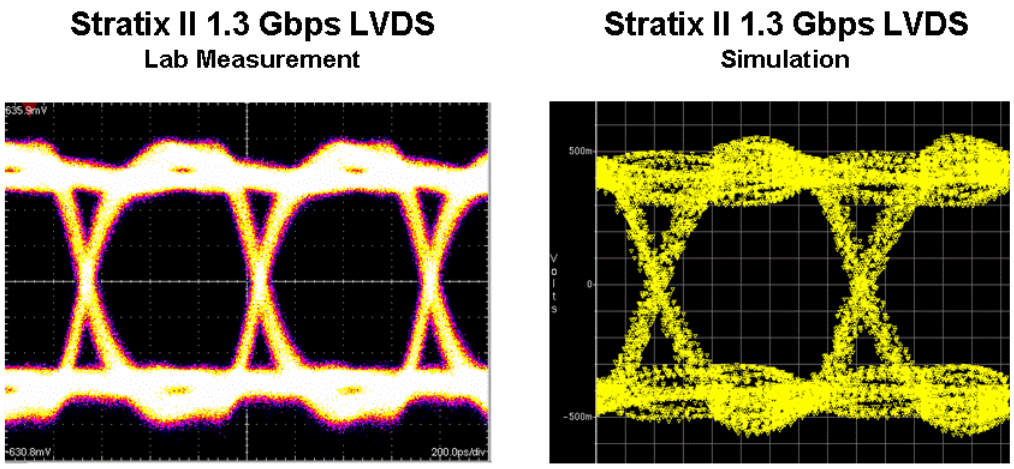
Table 1: Signal Integrity Test Set up for Stratix II and Virtex-4 I/Os

Test Setup Parameter	Virtex-4	Stratix II
IBIS Models	Downloaded from Xilinx Web Site, Rev 1.3 dated 1/21/2005	Downloaded from Altera Web Site, Rev 4.1 dated January, 2005
Software	IBIS Software version 3.2	IBIS Software version 3.2
Package	Virtex-4 IBIS Models do Not Have Package Information	F1020 Package
Voltage	Nominal	Nominal
Temperature	25^0C	25^0C

Results – LVDS Eye Diagram Measurements

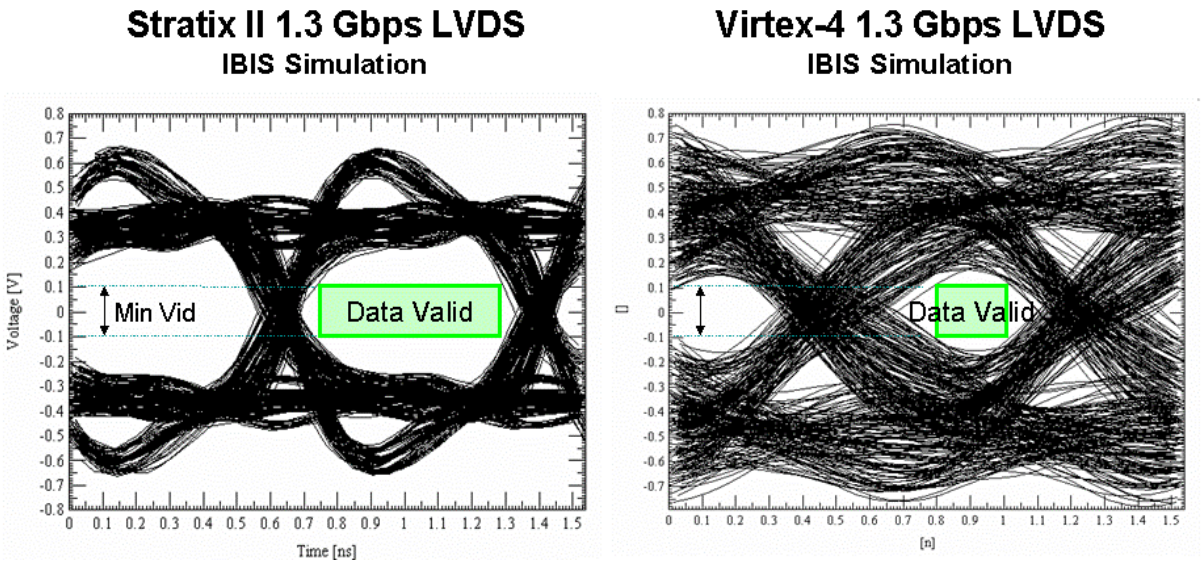
Figure 2 compares Stratix II 1.3 Gbps LVDS lab measurement results with simulation data. The scale on both the waveforms is the same. As can be seen, simulation results and lab data match very well.

Figure 2: 1.3 Gbps LVDS comparison of Stratix II measured and simulation eye-diagrams



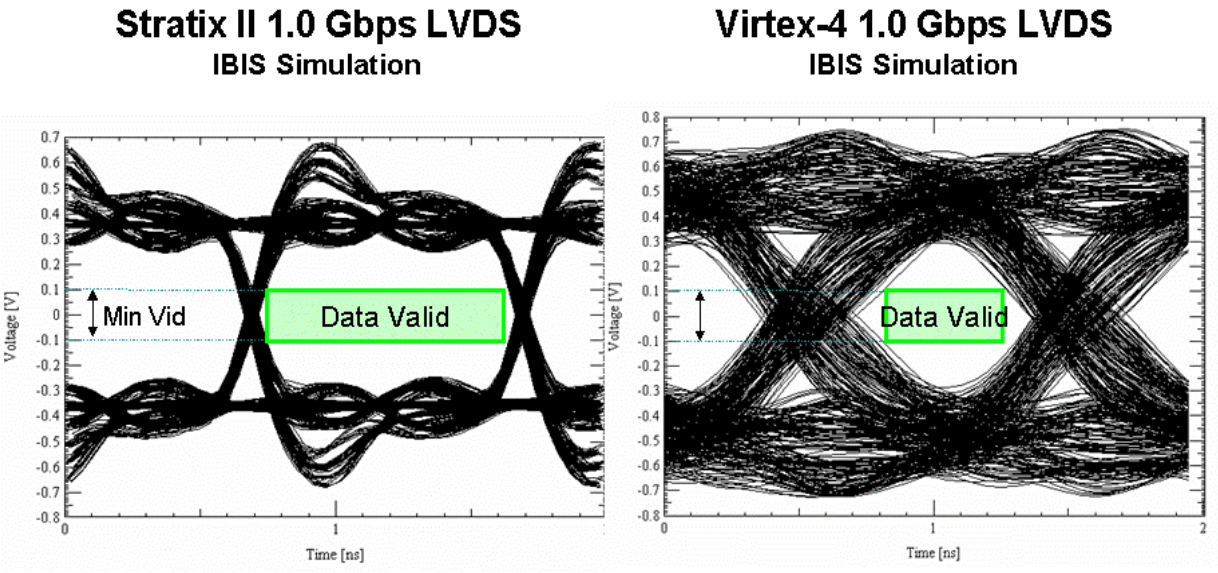
In Figure 3, Stratix II and Virtex-4 LVDS I/O signals are compared at 1.3 Gbps data rates. The Stratix II eye is significantly cleaner, with three times less edge noise, a three times faster edge rate, and a 2.3 times wider data valid window.

Figure 3: 1.3 Gbps LVDS IBIS simulation comparison of Stratix II and Virtex 4 eye-diagrams



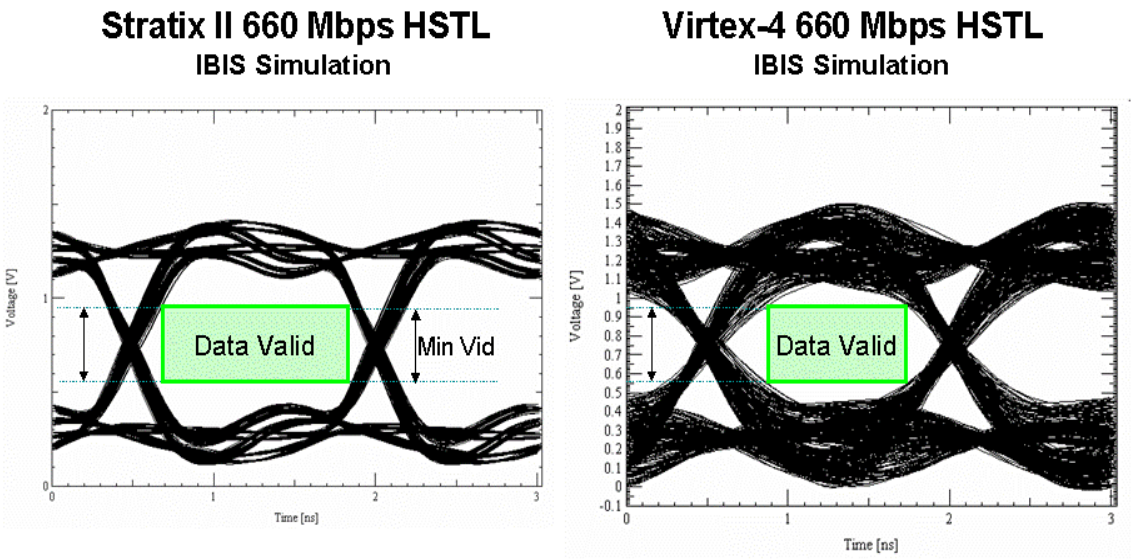
In Figure 4, Stratix II and Virtex-4 LVDS I/O signals are compared at 1.0Gbps data rates. The Stratix II eye is significantly cleaner, with 6.5 times less edge noise, a 3 times faster edge rate, and a 2.0 times wider data valid window.

Figure 4: 1.0 Gbps LVDS IBIS Simulation comparison of Stratix II and Virtex 4 eye-diagrams



In Figure 5, Stratix II and Virtex-4 HSTL I/O signals are compared at 660 Mbps data rates. The Stratix II eye is significantly cleaner, with a 1.8 times faster edge rate and a 1.3 times wider data valid window.

Figure 5: 660 Mbps HSTL IBIS Simulation comparison of Stratix II and Virtex 4 eye-diagrams



Pin Capacitance Measurements

The major difference between the Stratix II and Virtex-4 signal integrity is best explained by the relative difference in pin capacitance between the two FPGA products. The table below shows the pin capacitance values for different Stratix II and Virtex-4 I/Os. Stratix II I/O pin capacitance is at least 2 times lower than that of Virtex-4. Stratix II devices have the lowest pin capacitance in the FPGA industry. The pin capacitance numbers in this table were obtained from lab measurements.

Table 2: Pin Capacitance Comparison between Stratix II and Virtex-4 FPGAs

Pin Description	Stratix II	Virtex-4
User I/O – Vertical (1)	5.0pF	12.5pF
User I/O – Horizontal (2)	6.1pF	12.5pF
Configuration data pins	5.0pF	11.0pF
Clock pins –top/bottom CLK[4..7] and CLK[12..15]	6.0pF	11.0pF
Clock pins – left/right CLK0, CLK2, CLK8, CLK10	6.1pF	11.0pF
Clock pins – left/right CLK1, CLK3, CLK9, CLK11	3.3pF	11.0pF

Notes:

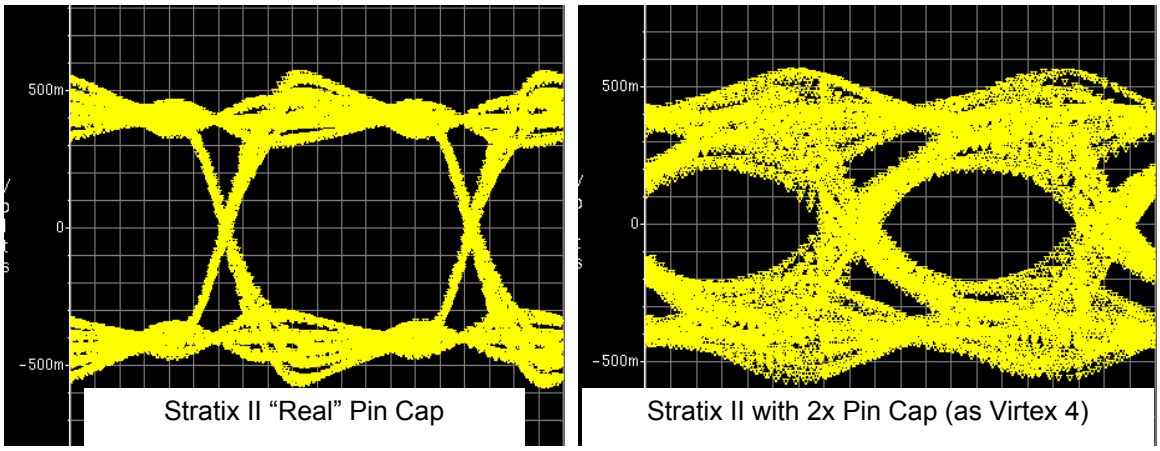
(1) *Vertical I/Os. I/O Standards Supported are LVTTL, LVCMOS, PCI, PCI-X, HSTL-1.5V Class I and II, HSTL-1.8V Class I and II, SSTL-18 Class I and II, SSTL-2 Class I and II.*

(2) *Horizontal I/Os. I/O Standards Supported are LVDS, HyperTransport, LVTTL, LVCMOS, SSTL-2, SSTL-18 Class I.*

Pin capacitance significantly impacts signal integrity. High pin capacitance affects signal integrity due to reflections. At high frequencies, capacitive loading at the far end acts as a resistor with low resistance. This causes impedance mismatch on the transmission line, which in turn cause reflections. In addition, pin capacitance slows down the edge rate of the signal, reducing the data valid window. On a separate note, higher pin capacitance can have an adverse effect of system power.

Figure 6 shows the impact of larger pin capacitance on signal integrity. The eye diagram on the left is a simulation of LVDS I/O pins at 1 Gbps with Stratix II pin capacitance. The diagram on right is a simulation of LVDS I/O pins with double the pin capacitance of Stratix II devices (same as Virtex-4 pin capacitance). Doubling the pin capacitance increased the edge noise, slowed down the edge rate, and reduced the data valid window.

Figure 6: 1.0 Gbps LVDS IBIS Simulation Comparison of Stratix II with "Real" Pin Capacitance and Stratix II with 2X Pin Capacitance (as Virtex 4)

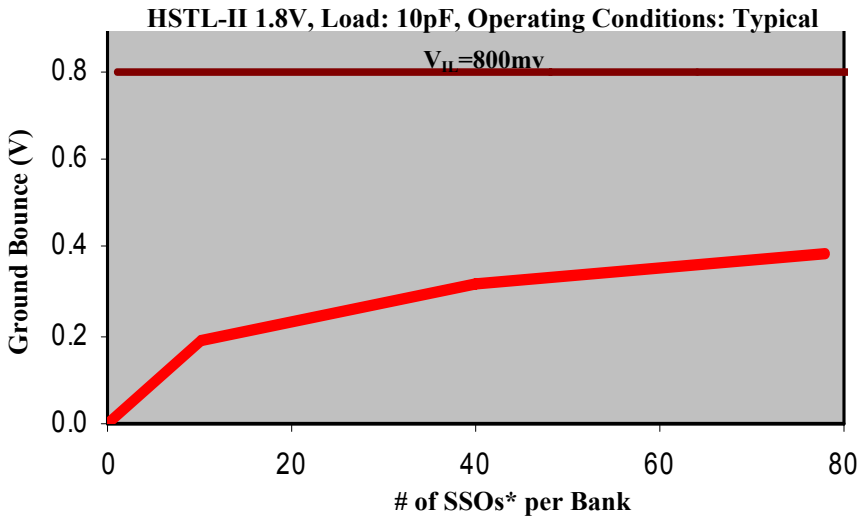


Simultaneous Switching Noise

A very important aspect of signal integrity is the impact of having many I/O pins toggling at the same time. This is called simultaneous switching noise (SSN). SSN is dependent on the quality of the chip and package power distribution network and I/O coupling.

SSN experiments were performed on Stratix II EP2S60F1020, HSTL-II 1.8V I/O pins with up to 100% of the bank toggling. Figure 6 shows the ground bounce voltage on the victim pin with different number of simultaneously switching outputs (SSOs) per bank. The maximum ground bounce voltage is only 0.4 V. The input low voltage (V_{IL}) for the HSTL-II 1.8 standard is 0.8V. As shown in Figure 7, ground bounce voltage is not violating the V_{IL} level, even with 100% of the bank toggling. This can be attributed to the low inductance and IR drop in Stratix II I/O buffers and packages.

Figure 7: Chart of Stratix II HSTL-II 1.8V I/O SSN Performance



Altera Silicon-Package Co-Design Methodology

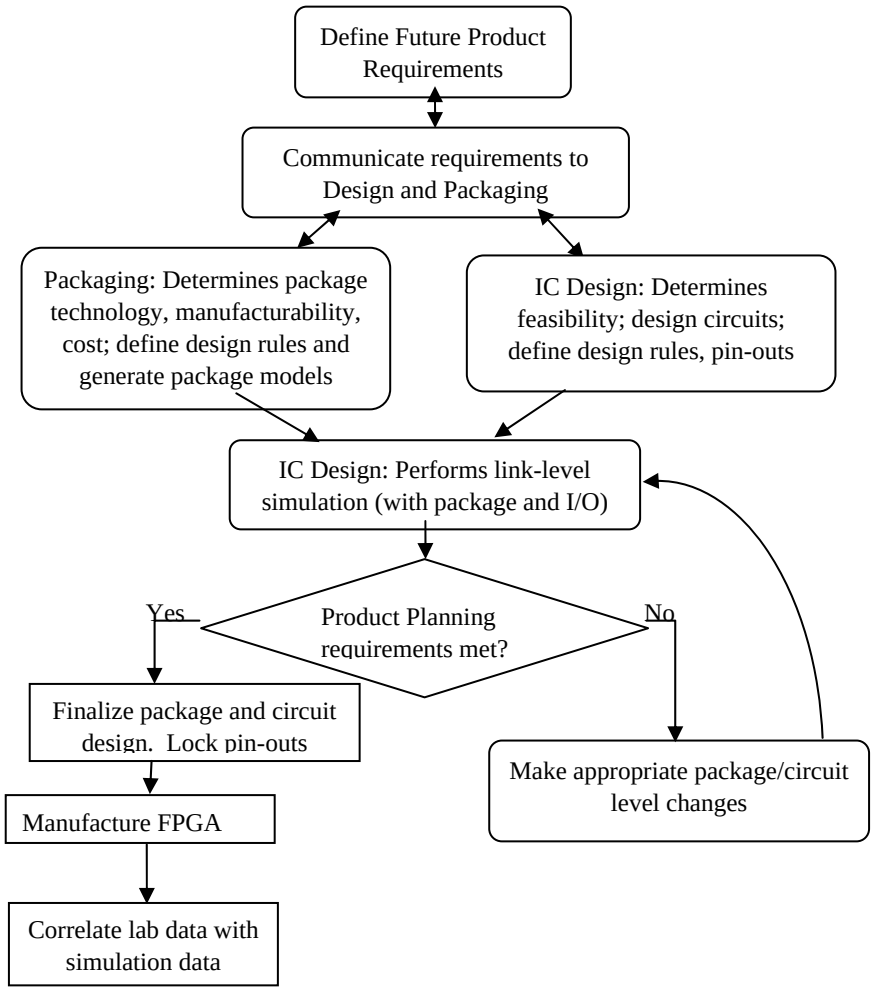
Altera achieved the excellent Stratix II signal integrity through an early focus on signal integrity in the design process, utilizing a silicon-package co-design methodology. Altera's silicon-package co-design methodology lays special emphasis on mitigating signal integrity issues at the chip and package level. Early in the product-development process, device requirements are established with a special emphasis on signal integrity.

Requirements that reduce signal integrity issues are then communicated to IC design and packaging engineers. These requirements are used by design engineers to define/improve design rules during circuit design. They also incorporate signal-integrity based requirements while determining circuit and pin layout and use them to generate I/O buffer models. Simultaneously, packaging engineers use the requirements to determine package technology and manufacturability. This feasibility analysis is then followed by steps to develop signal and power/ground routing, pin layout, etc. Package models are then generated.

Using both package and I/O buffer models, IC design engineers then perform link level simulations to ensure that performance and signal integrity requirements are met. Results from the link level simulations are used to refine the package and silicon design process. The entire package and silicon design process is now integrated and iterative, involving optimization between pin layout, chip layout, and cost/performance objectives. After silicon is available, simulated data is then correlated with lab experiments. A brief flow chart of the methodology is shown in Figure 8.

This design process was used during Stratix II product development. It enabled Altera's engineers to accurately predict the signal integrity behavior of the Stratix II device several months before actual silicon was available. Also, it ensured that Stratix II FPGAs met all the signal integrity requirements that were set during product definition.

Figure 8: Altera Silicon-Package Co-Design Methodology



Stratix II I/O Buffers

Stratix II I/O buffers are designed to minimize signal integrity issues that arise at the chip level. Improper I/O buffer design can cause a variety of signal integrity issues. For example, I/O buffers with high pin-capacitance cause reflections, inadequate return current paths cause SSN, and improper isolation to adjacent I/O circuitry causes signal crosstalk. These phenomena deteriorate signal quality, and limit system performance and reliability.

Several design features were incorporated into Stratix II I/O buffers to mitigate signal integrity failures. Table 3 lists some of these features and their impact on signal integrity.

Table 3: Features in Stratix II I/O Buffers that Reduce Signal Integrity Issues

Stratix II I/O Design Feature	Impact on Signal Integrity
On-chip decoupling capacitors	Reduces ground bounce and V_{CC} sag.
Improved transistor design, more compact and efficient layout	Low input pin capacitance to minimize reflections and signal noise.
V_{CCPD} power supply connected to 3.3V (power supply to the pre-driver to the output buffer)	V_{CCPD} is connected to of 3.3 V (as a comparison, Stratix V_{CCPD} was 1.5V), which increases the V_{GS} (gate voltage at the transistor) for HSTL I/O standards. As a result, the transistor size was reduced, lowering the I/O pin capacitance.
On-chip series and differential termination	Eliminates the need for external termination resistors on the board while minimizing reflections.
Output drive strength control	Allows designer to have control the amount of current. Compensates for signal attenuation and ISI so receiver can correctly capture data.
Output slew rate control	Gives designer flexibility to change the slew-rate of the output signals. This at times helps reduce SSN.
Programmable pre-emphasis and V_{OD} for differential buffers	Compensates for signal attenuation and ISI so receiver can correctly capture data. Programmable pre-emphasis controls the slew-rate and programmable V_{OD} controls the amount of current.

Stratix II Device Package

In high-speed systems, package performance is one of the major limiting factors of the overall system performance. This necessitates the fabrication of interconnects and packages that are capable of supporting very fast signals without degrading signal integrity to unacceptable levels.

Signal integrity was one of the most important factors that was considered during Stratix II package design. Table 4 lists Stratix II package characteristics that help minimize signal integrity issues at the package level.

Table 4: Stratix II Packaging Features that Minimize Signal Integrity Issues

Stratix II Package Characteristic	Impact on Signal Integrity
Dedicated power planes above package core	Reduces power supply inductance.
50Ω impedance for single-ended I/O pins and 100Ω for differential I/O pins	Minimizes impedance mismatch and reduces reflections.
Short traces and wide spaces between adjacent traces	Reduces cross talk between signals, minimizes package inductance.
Matched traces for critical signals	Reduces skew between signals.
Package traces designed as transmission line with 50Ω impedance	The traces reduce reflections from the package and significantly reduce package trace inductance and capacitance as they behave as transmission lines instead of lumped RLC discontinuities.

Virtex-4 has a higher power-to-I/O ratio than Stratix II FPGAs, but Stratix II signal integrity is much better than in Virtex-4. Measured and simulated comparisons clearly show Stratix II devices have better signal integrity and more I/O elements through superior packaging and I/O technologies.

Stratix II packages have dedicated power and ground planes below the package core (close to the balls). The impedance between the power and ground planes and the PCB is negligible, minimizing the need for larger numbers of power and ground pins on the package. The impedance between the power and ground planes in the package and the flip-chip mounting points is minimized using multiple parallel supply paths.

The Stratix II package power distribution network has been designed to minimize the overall power and ground impedance from the power and ground planes to the die to minimize SSN. SSN results show that even with 100% of the bank toggling, ground bounce voltage does not violate V_{IL} levels.

Altera's packaging and I/O technology deliver three significant benefits: excellent signal integrity, strong immunity to SSN, and up to 21% more I/O elements in equivalent pin density devices.

Virtex-4 packages do have similar power and ground planes below the package core. However, initial package analysis shows that Xilinx did not design the package to achieve the lowest power and ground impedance. For these reasons, Virtex-4 packages require more power/ground pins and still deliver reduced signal integrity.

Conclusion

Altera has successfully made signal integrity optimization a core factor in FPGA design flow. By placing a premium on effort in ensuring mitigation of signal integrity issues, Altera's silicon-package co-design methodology has ensured quality at the chip and package level. Stratix II devices provide significant signal integrity benefits over Virtex-4, as evidenced by the experiment results. In applications that require superior signal integrity and when the costs of poor signal integrity are high, Stratix II FPGAs are the clear choice.

References

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