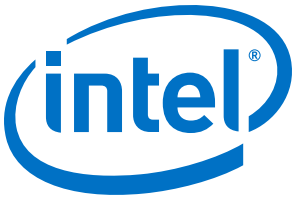

SDI Audio Intel FPGA IP User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.2**

IP Version: **19.1.0**

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Contents

1. SDI Audio Intel FPGA IP Overview

The SDI Audio Intel FPGA IP cores ease the development of video and image processing designs. The SDI Audio Embed IP core allows audio and video signals to be combined into one digital signal. The SDI Audio Extract IP core allows audio and video signals in one digital signal to be split into separate signals.

The SDI Audio Intel FPGA IP cores are part of the IP Catalog Library, which is distributed with the Intel® Quartus® Prime software.

Note: The SDI Audio Intel FPGA IP cores are available in the Intel Quartus Prime Pro Edition software from version 19.2 onwards for supported device families.

Note: The SDI Audio Intel FPGA IP cores are available in the Intel Quartus Prime Standard Edition software version 18.1 for supported device families. Refer to the user guide for the previous IP core version (18.0) for information.

You can use the following cores to embed, extract or convert audio:

- Audio Embed Intel FPGA IP
- Audio Extract Intel FPGA IP
- Clocked Audio Input Intel FPGA IP
- Clocked Audio Output Intel FPGA IP

You can instantiate the SDI Audio Intel FPGA IP cores with the SDI and SDI II Intel FPGA IP cores. You can configure each Audio IP core at run time using an Avalon-MM slave interface, provided the relevant parameters are enabled.

Related Information

- SDI Audio Intel FPGA IP User Guide Archives on page 33
  Provides a list of user guides for previous versions of the SDI Audio Intel FPGA IP cores.
- Serial Digital Interface (SDI) IP Core User Guide
  For information about SDI IP core.
- SDI II Intel FPGA IP User Guide
  For information about SDI II Intel FPGA IP core.

1.1. Release Information

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

The IP versioning scheme (X.Y.Z) number changes from one software version to another. A change in:

- X indicates a major revision of the IP. If you update your Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

Table 1. SDI Audio Intel FPGA IP Cores Current Release Information

Item	Description
IP Version	19.1.0
Intel Quartus Prime Version	19.2
Release Date	July 2019
Ordering Code	IP-SDI
Device Family	Intel Quartus Prime Pro Edition: Intel Arria® 10 GX, Intel Arria 10 GT, and Intel Arria 10 SX FPGA device families.

2. SDI Audio Intel FPGA IP Getting Started

The SDI Audio Intel FPGA IP cores are installed as part of the Intel Quartus Prime installation process.

You can select and parameterize any Intel FPGA IP from the library. Intel provides an integrated parameter editor that allows you to customize the SDI Audio Intel FPGA IP cores to support a wide variety of applications.

Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

2.1. Instantiating the SDI Audio Intel FPGA IP

You can instantiate the SDI Audio Embed and Audio Extract IP cores in the following ways:

- Instantiate through the IP Catalog using the IP parameter editor.
- Instantiate within Platform Designer with the audio inputs exposed outside Platform Designer.
- Instantiate within Platform Designer with the audio inputs exposed as Avalon-ST Audio within Platform Designer.
  As the SDI Audio Embed and Extract IP cores use an Avalon-MM slave interface to access the control registers, the most convenient way for you to instantiate the components are within Platform Designer. You are provided with the component declaration TCL files to support either the ordinary AES audio inputs or the Avalon-ST audio interface.

2.2. Simulating the Testbench

Intel provides a fixed testbench as an example to simulate the SDI Audio Intel FPGA IP cores. Use this testbench to simulate the SDI Audio Embed and the associated SDI Audio Extract IP cores, and the SDI Clocked Audio Input and the associated SDI Clocked Audio Output IP cores.

You can obtain the testbench from **ip/altera/audio_ip/simulation** directory.

To use the testbench with the ModelSim simulator, follow these steps:

The following table lists the SDI Audio Intel FPGA IP cores to generate with recommended parameter configurations and file names.

Table 2. SDI Audio IP Cores to Generate

IP Name	Number of Supported Audio Groups Parameter	Include Avalon-ST Interface Parameter	Include Avalon-MM Control Interface Parameter	IP Variant File Name
Audio Embed	4	Off	On	audio_embed_top.ip
Audio Embed	4	On	On	audio_embed_avalon_top.ip
Audio Extract	—	Off	On	audio_extract_top.ip
Audio Extract	—	On	On	audio_extract_avalon_top.ip
Clocked Audio Input	—	—	On	clocked_audio_input_top.ip
Clocked Audio Output	—	—	On	clocked_audio_output_top.ip

1. Open the Intel Quartus Prime software.
2. On the File menu, click the **New Project Wizard**.
3. Specify a sensible name for the project working directory, project name, and project top-level entity, and click **Next**.
4. Select **Empty Project** and click **Next**.
5. On the Add Files menu, leave everything empty and click **Next**.
6. Select the device family (for example, **Arria 10 (GX/SX/GT)**) and the desired FPGA device (for example, **10AS066N3F40E2SG**).
7. Click **Finish**.
8. Outside the Intel Quartus Prime software, copy the simulation folder including all simulation testbench files contained within this folder (for example, from **/tools/acds/19.2/57/linux64/ip/altera/audio_ip/simulation**) to your project working directory.
9. In the IP Catalog (**Tools > IP Catalog**), locate and double-click the IP under **Library > Interface Protocols > Audio & Video > *<IP Name e.g. Audio Embed>***.
   The New IP Variant prompt appears.
10. Save the IP variant according to the file name in the *SDI Audio IP Cores to Generate* table.
    The IP Parameter Editor appears.
11. Configure the IP according to the *SDI Audio IP Cores to Generate* table while leaving the rest of the parameters at default.
12. Click **Generate HDL**.
13. On the Generation menu, select **Create Simulation Model > Verilog** and click **Generate**.
14. Close the IP Parameter Editor after IP generation is complete.
15. Repeat steps 9 to 14 for all IPs listed in the *SDI Audio IP Cores to Generate* table.
16. Set the QUARTUS_ROOTDIR environment variable to point to your installation of the Intel Quartus Prime software though the Windows command prompt or Linux terminal.
    Command line examples:

```
windows64> setx QUARTUS_ROOTDIR “C:\intelFPGA_pro
\19.2\quartus”

linux-bash> export QUARTUS_ROOTDIR=“/tools/acds/19.2/57/
linux64/quartus”

linux-csh> setenv QUARTUS_ROOTDIR “/tools/acds/19.2/57/
linux64/quartus”
```

17. Start the ModelSim simulator.
18. Run **run.tcl** in your project working directory simulation folder. This file compiles the design.
    A selection of signals appears on the waveform viewer. The simulation runs automatically, providing a pass or fail indication upon completion.

Guidelines

When you use the testbench to simulate the IP cores, consider the following guidelines:

- Select the video standard for the video test source through the generic G_TEST_STD of the testbench entity. Set 0, 1, 2 or 3 to select SD-SDI, HD-SDI, 3G-SDI Level A, or 3G-SDI Level B.
- The audio test source uses the 48-kHz clock output from the SDI Audio Embed IP core. The audio test sample comprises an increasing count which allows the testbench to check the extracted audio at the far end of the processing chain.
- The SDI Audio Embed IP core accepts these video and audio test sources to create a video stream with embedded audio. The SDI Audio Extract IP core then receives the resulting stream to recover the embedded audio. Examine this audio sequence to ensure that the count pattern that was created is preserved.
- The synchronization requirements of the receive FIFO buffer in the SDI Audio Extract IP core allows you to repeat the occasional sample from the SDI Audio Extract IP core. Synchronization may take up to a field period of typically 16.7 ms to complete.
- Select G_INCLUDE_AVALON_ST = 1, if you want to instantiate another SDI Audio Embed IP core with Avalon-ST interface (with embedded clocked audio output component) and the associated SDI Audio Extract IP core with Avalon-ST interface (with embedded clocked audio input component) in this testbench.

3. SDI Audio Intel FPGA IP Functional Description

The following sections describe the block diagrams and components for the SDI Audio Intel FPGA IP cores.

3.1. SDI Audio Embed IP Core

The SDI Audio Embed Audio IP core embeds audio into the SD-, HD-, and 3G-SDI video standards.

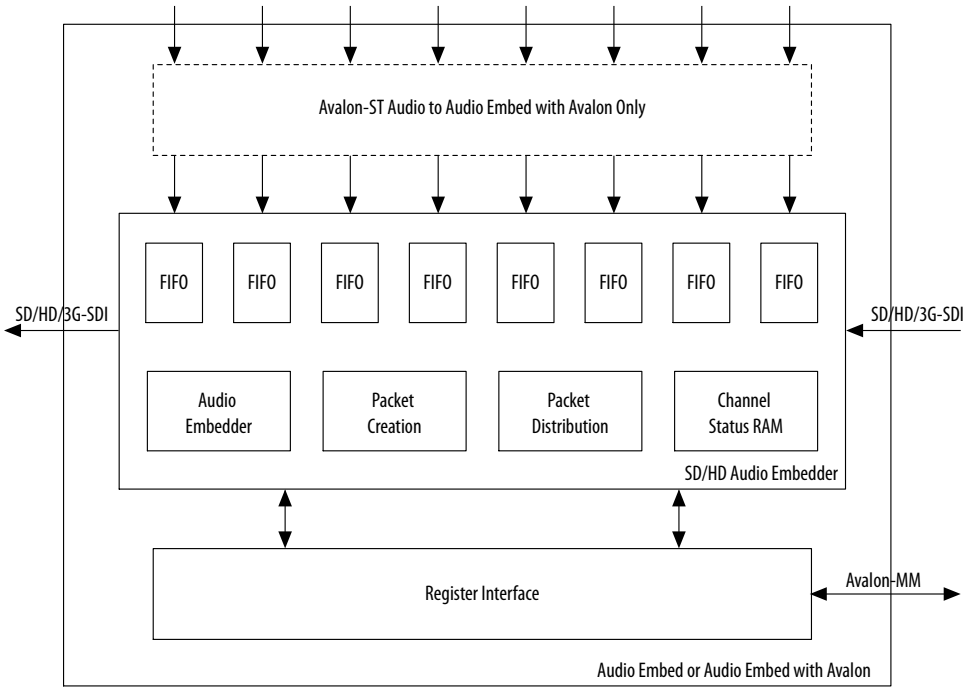
The format of the embedded audio is in accordance with the following standards:

- SMPTE272M-ABCD standard for SD-SDI
- SMPTE299M standard for HD-SDI
- SMPTE299M standard for 3G-SDI (provisional)

This IP core supports AES audio format for 48-kHz sampling rate

This figure shows a block diagram of the SDI Audio Embed IP core.

Figure 1. SDI Audio Embed IP Core Block Diagram



The SDI Audio Embed IP core embeds up to 16 channels or 8 channel pairs. The input audio can be any of the sample rates permitted by the SMPTE272M-ABCD and SMPTE299M standards; synchronous to the video. If you want to embed audio pairs together in a sample audio group, the audio pairs must be synchronous with each other.

The SDI Audio Embed IP core consists of the following components:

- An encrypted audio embedder core
- A register interface block that provides support for an Avalon-MM control bus

The audio embedder accepts the audio in AES format, and stores each channel pair in an input FIFO buffer. As the embedder places the audio sample in the FIFO buffer, it also records and stores the video clock phase information.

When accepting the audio in AES format, the SDI Audio Embed IP core does one of the following operations:

- maintains the channel-status details
- replaces the channel-status details with the default or the RAM versions

3.2. SDI Audio Extract IP Core

The SDI Audio Extract IP core accepts the SD-, HD-, and 3G-SDI from the SDI IP cores and extracts one channel pair of embedded audio.

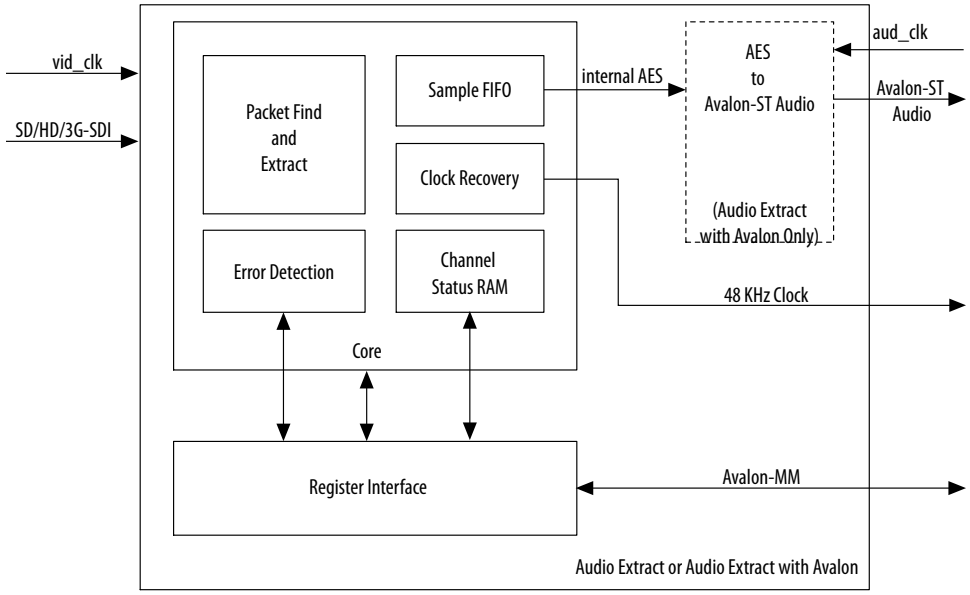
The format of the embedded audio is in accordance with the following standards:

- SMPTE272M-ABCD standard for SD-SDI
- SMPTE299M standard for HD-SDI
- SMPTE299M standard for 3G-SDI (provisional)

If you are extracting more than one channel pair, you must use multiple instances of the component. This IP core supports AES audio format for 48-kHz sampling rate.

This figure shows a block diagram of the SDI Audio Extract IP core.

Figure 2. SDI Audio Extract IP Core Block Diagram



The SDI Audio Extract IP core consists of the following components:

- An audio extraction core
- A register interface block that provides support for an Avalon-MM control bus

The clock recovery block recreates a 64 × sample rate clock, which you can use to clock the audio output logic. As the component recreates this clock from a 200-MHz reference clock, the created clock may have a higher jitter than is desirable.

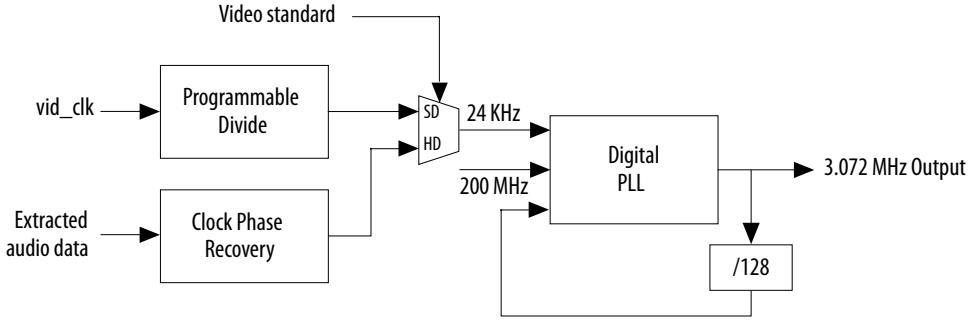
A digital PLL synchronizes this created clock to a 24-kHz reference source.

For the HD-SDI embedded audio, the 24-kHz reference source is the embedded clock phase information.

For the SD-SDI embedded audio, where the embedded clock phase data is not present, you can create the 24-kHz reference signal directly from the video clock.

This figure shows the clock recovery block diagram.

Figure 3. Clock Recovery Block Diagram



3.3. SDI Clocked Audio Input IP Core

The Clocked Audio Input IP core converts clocked audio in AES formats to Avalon-ST audio.

For a typical AES input, for each channel, the clocked audio input function does the following operations:

- Creates a 192-bit validity word, user word and channel status word
- Presents the words as a control packet after the audio data packet

3.4. SDI Clocked Audio Output IP Core

The SDI Clocked Audio Output IP core accepts clocked Avalon-ST audio and converts to audio in modified AES formats.

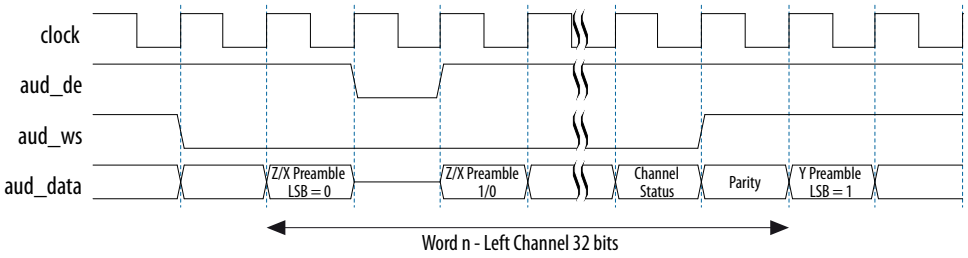
3.5. AES Format

The SDI cores use the AES standard. The Audio Engineering Society (AES), together with the European Broadcasting Union (EBU), created a digital audio transmission standard known as the AES/EBU standard. The AES standard is a digital audio standard for transporting digital audio signals serially between devices.

Using the AES format requires the entire 64-bit AES frame to be sent serially. As the AES defines the preambles as biphase mark codes, which cannot be directly decoded to 4 bits, you must replace the preambles with X = 0000b, Y = 0001b, and Z = 0010b. This internal AES format serializes the bit-parallel data words by sending the least significant bits (LSB) first, with the audio sample (up to 24 bits).

This figure shows the timing diagram of the internal AES format.

Figure 4. Internal AES Format Timing Diagram

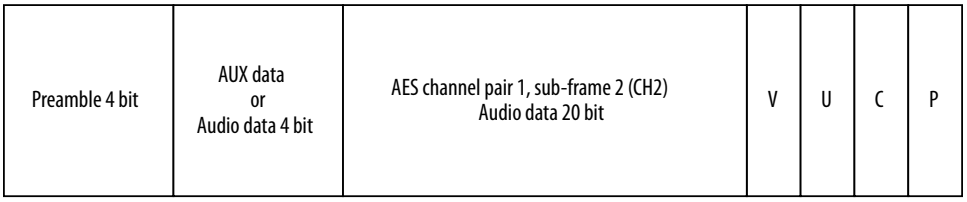


3.6. Avalon-ST Audio Interface

To allow the standard components inside Platform Designer (Standard) to interconnect, you must define the Avalon-ST audio interface. The Avalon-ST audio interface must carry audio to and from physical AES3 interfaces; which means to support the AES3 outputs, the interface must transport the extra V, U, and C bits. You may create the P bit.

Each audio block consists of 192 frames, and each frame has channels 1 and 2. Each frame has a combination of the bits shown in the following figure.

Figure 5. AES Format

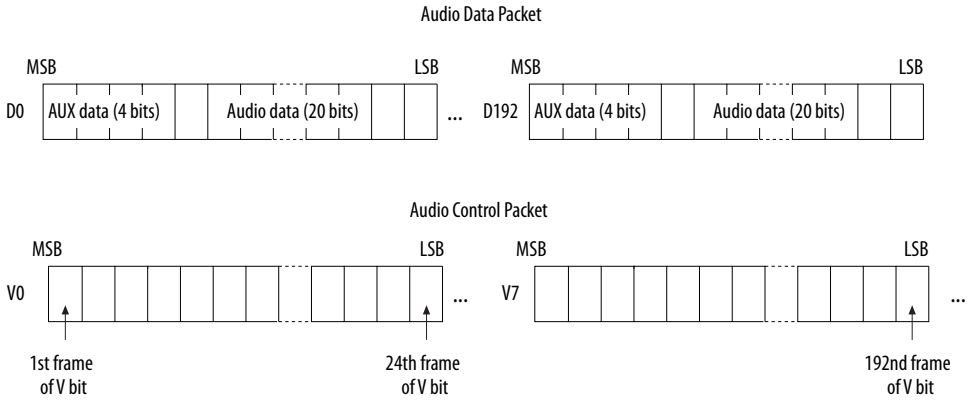


The Avalon-ST is a packet-based interface, which carries audio information as a sequence of data packets. The functions define the types of packets as audio data packets and audio control packets.

This figure shows the audio data and audio control packets for Avalon-ST audio interface.

Figure 6. Audio Data and Audio Control Packets for Avalon-ST Audio Interface

The sequence of audio control packets begins with V bit, U bit, and finally C bit. The audio control packets for U and C bits are similar to V bits.



The Avalon-ST audio protocol separates the audio data from the control or status data to facilitate audio data processing. The protocol defines that the data is packed LSB first, which matches the AES3 data. The audio data size is configurable at compile time and matches the audio data sample size. Including the aux, the audio data word is 24 bits.

In Avalon-ST audio, the data is packed as 24 bit symbols, typically with 1 symbol per beat [23:0]. The core transmits the audio control data as a packet after the audio data to meet the latency requirements.

The packet type identifier defines the packet type. The packet type identifier is the first value of any packet, when the start of packet signal is high. The audio data packet identifier is 0×A and the audio control data packet identifier is 0×E.

The table below lists the packet types.

Table 3. Avalon-ST Packet Types

Type Identifier	Description
0	Video data packet
1–8	User packet types

continued...

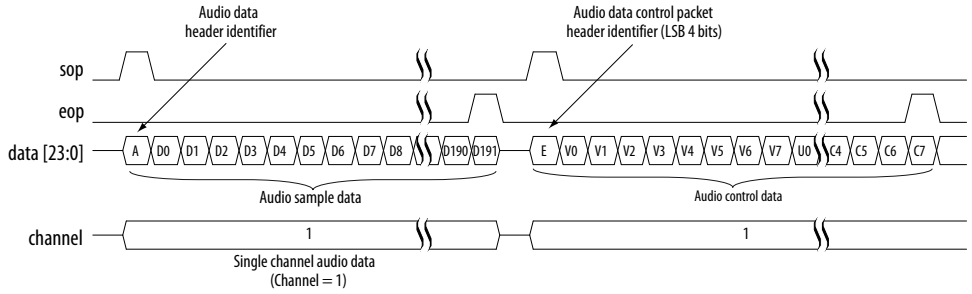
Type Identifier	Description
10	Audio data packet
14	Audio control data packet
15	Video control data packet
9–15	Reserved

The preamble data, XYZ from AES, describes whether the data is at the start of a block and which channel the audio refers to. In Avalon-ST audio protocol, you are not required to transport the preamble data because the information stored in the data is described by the start of packet, end of packet, and channel signals.

The start of packet, end of packet, and channel signals indicate the start of the audio sample data and the associated audio channel.

For a single audio channel, the channel signal indicates channel 1 for all valid samples. This figure shows an example of a single audio channel.

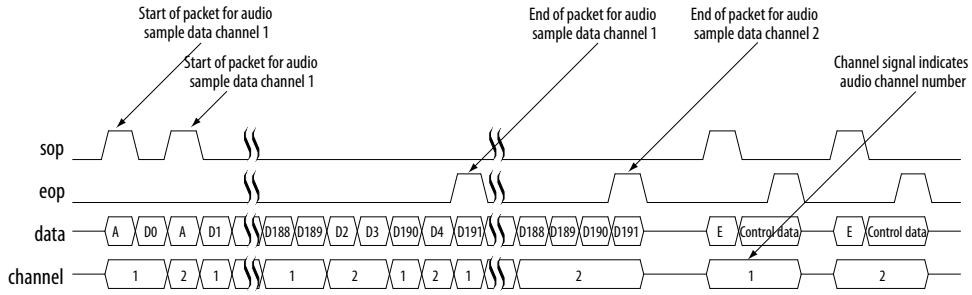
Figure 7. Single Audio Channel



For multiple channels, the Avalon-ST interface standard allows the packets to interleave across the channels. By interleaving, the interface allows multiple audio sources to be multiplexed and demultiplexed.

This figure shows an example of two audio channels, where the channel signal indicates either channel 1 or channel 2. Each channel has a start of packet and an end of packet signal, which allows the channel interleaving and de-interleaving.

Figure 8. Multiple Audio Channels



4. SDI Audio Intel FPGA IP Parameters

The following sections describe the parameters for the SDI Audio IP cores.

4.1. SDI Audio Embed Parameters

The following table lists the parameters for the SDI Audio Embed IP core.

Table 4. SDI Audio Embed Parameters

Parameter	Value	Description
Number of supported audio groups	1, 2, 3, 4	Specifies the maximum number of audio groups supported. Each audio group consists of 4 audio channels (2 channel pairs). You must specify all the four channels to the same sample frequencies.
Async Audio Interface	On or Off	Turn on to enable the Asynchronous input. This mode supports an audio clock equal to or higher than 64 × sample rate.
Parallel Audio Interface	On or Off	Turn on to send AES data in parallel mode with a 32-bit parallel interface. Requires **Async Audio Interface** to be turned on.
Frequency of fix_clk	0, 24.576, 25, 50, 100, 200	Sets the expected frequency of the `fix_clk` input; used as frequency reference when detecting the difference between video rate of 1/1.000 or 1/1.001. Setting this parameter to 0 drives `fix_clk` low. The Intel Quartus Prime Pro Edition software does not support this parameter.
Include SD-SDI 24-bit support	On or Off	Enables the embedding of SD-SDI Extended Data Packets (EDP) for each audio group.
Cleanly remove existing audio	0,1, 2	Enables the removal of existing embedded audio data. When set to 1, the system requires extra storage to delay the video and remove any existing audio from SD-SDI, HD-SDI, or 3G-SDI Level A standard. When set to 2, the system includes extra storage to remove the existing audio from 3G-SDI Level B standard. Select 0 to turn off this parameter. The Intel Quartus Prime Pro Edition software does not support this parameter.
Channel status RAM	0,1, 2	Enables storage of the custom channel status data. Select 1 to generate a single channel status RAM, or 2 to generate separate RAMs for each input audio pair. Select 0 to turn off this parameter.
Frequency sine wave generator	On or Off	Turn on to enable a four-frequency sine wave generator. You can use the four-frequency sine wave generator as a test source for the audio embedder.

continued...

Parameter	Value	Description
Include clock	On or Off	Turn on to enable a 48-kHz pulse generator synchronous to the video clock. You can use the 48-kHz pulse generator to request data from a sample rate converter. When you turn on the **Frequency Sine Wave Generator** parameter, the core automatically includes this pulse generator.
Include Avalon-ST interface	On or Off	Turn on to include the SDI Clocked Audio Output IP core. When you turn on this parameter, the Avalon-ST interface signals appear at the top level. Otherwise, the audio input signals appear at the top level.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

Related Information

SDI Audio Embed Signals on page 17

4.2. SDI Audio Extract Parameters

The following table lists the parameters for the SDI Audio Extract IP core.

Table 5. SDI Audio Extract Parameters

Parameter	Value	Description
Async Audio Interface	On or Off	Turn on to enable the Asynchronous output. This mode supports an audio clock equal to or higher than 64 × sample rate.
Parallel Audio Interface	On or Off	Turn on to send AES data in parallel mode with a 32-bit parallel interface. Requires **Async Audio Interface** to be turned on. The actual audio sample rate is specified for serial data transmission. The equivalent audio sample rate in parallel mode matches the actual audio sample rate.
Include SD-SDI 24-bit support	On or Off	Enables the extra logic to recover the EDP ancillary packets from SD-SDI inputs.
Channel status RAM	On or Off	Turn on to store the received channel status data.
Include error checking	On or Off	Turn on to enable extra error-checking logic to use the error status register.
Include status register	On or Off	Turn on to enable extra logic to report the audio FIFO status on the `fifo_status` port or register.
Include clock	On or Off	Turn on to enable the logic to recover both a sample rate clock and a 64 × sample rate clock. With HD-SDI inputs, the core generates the output by using the embedded clock phase information. With SD-SDI inputs, the core generates this output by using the counters running on the 27-MHz video clock. This generation limits the SD-SDI embedded audio to being synchronous to the video.
Include Avalon-ST interface	On or Off	Turn on to include the SDI Clocked Audio Input IP core. When you turn on this parameter, the Avalon-ST interface signals appear at the top level. Otherwise, the audio input signals appear at the top level.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

Related Information

SDI Audio Extract Signals on page 20

4.3. SDI Audio Clocked Audio Input Parameters

The following table lists the parameters for the SDI Clocked Audio Input IP cores.

Table 6. SDI Clocked Audio Input Parameters

Parameter	Value	Description
FIFO size	3–10	Defines the internal FIFO depth. For example, a value of 3 means $2^3 = 8$.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

4.4. SDI Audio Clocked Audio Output Parameters

The following table lists the parameters for the SDI Clocked Audio Output IP cores.

Table 7. SDI Clocked Audio Output Parameters

Parameter	Value	Description
FIFO size	3–10	Defines the internal FIFO depth. For example, a value of 3 means $2^3 = 8$.
Include Avalon-MM control interface	On or Off	Turn on to include the Avalon-MM control interface. When you turn on this parameter, the register interface signals appear at the top level. Otherwise, the direct control interface signals appear at the top level.

5. SDI Audio Intel FPGA IP Interface Signals

The following sections describe the interface signals for the SDI Audio IP cores.

5.1. SDI Audio Embed Signals

The following tables list the signals for the SDI Audio Embed IP cores.

This table lists the general input and output signals.

Table 8. SDI Audio Embed General Input and Output Signals

Signal	Width	Direction	Description
reset	[0:0]	Input	This signal resets the system.
fix_clk	[0:0]	Input	This signal provides the frequency reference used when detecting the difference between video standards using 1 and 1/1.001 clock rates. If its frequency is 0, the signal only detects either one of the clock rates. The core limits the possible frequencies for this signal to 24.576 MHz, 25 MHz, 50 MHz, 100 MHz, and 200 MHz. Set the required frequency using the **Frequency of fix_clk** parameter.
vid_std_rate	[0:0]	Input	If you set the **Frequency of fix_clk** parameter to 0, you must drive this signal high to detect a video frame rate of 1/1.001 and low to detect a video frame rate of 1. For other settings of the **Frequency of fix_clk** parameter, the core automatically detects these frame rates and drives this signal low.
vid_clk48	[0:0]	Output	The 48 kHz output clock that is synchronous to the video. This clock signal is only available when you turn on the **Frequency Sine Wave Generator** or **Include Clock** parameter.

This table lists the video input and output signals.

Table 9. SDI Audio Embed Video Input and Output Signals

Signal	Width	Direction	Description
vid_clk	[0:0]	Input	The video clock that is typically 27 MHz for SD-SDI, 74.25 MHz or 74.17 MHz for HD-SDI, or 148.5 MHz or 148.35 MHz for 3G-SDI standards. You can use higher clock rates with the vid_datavalid signal. Set exclusive clock group to aud_clk and vid_clk to prevent unstable or flickering image.
vid_std	[1:0]	Input	Indicates the received video standard. Applicable for 3G-SDI, dual standard, and triple standard modes only. Set this signal to indicate the following formats: • [00] for10-bit SD-SDI • [01] for 20-bit HD-SDI • [10] for 3G-SDI Level B • [11] for 3G-SDI Level A

continued...

Signal	Width	Direction	Description
vid_datavalid	[0:0]	Input	Assert this signal when the video data is valid.
vid_data	[19:0]	Input	Receiver protocol reset signal. This signal must be driven by the rx_rst_proto_out reset signal from the transceiver block. This signal carries luma and chroma information. SD-SDI: • [19:10] Unused • [9:0] Cb,Y, Cr, Y multiplex HD-SDI and 3G-SDI Level A: • [19:10] Y • [9:0] C 3G-SDI Level B: • [19:10] Cb,Y, Cr, Y multiplex (link A) • [9:0] Cb,Y, Cr, Y multiplex (link B)
vid_out_datavalid	[0:0]	Output	The core drives this signal high during valid output video clock cycles.
vid_out_trs	[0:0]	Output	The core drives this signal high during the first 3FF clock cycle of a video timing reference signal; the first two 3FF cycles for 3G-SDI Level B. This signal provides easy connection to the SDI IP cores.
vid_out_ln	[10:0]	Output	The video line signal that provides for easy connection to the SDI IP cores. To observe the correct video out line number, allow two-frame duration for the audio embed IP to correctly embed and show the line number.
vid_out_data	[19:0]	Output	The video output signal.

This table lists the audio input signals.

Table 10. SDI Audio Embed Audio Input Signals

N is the number of audio group.

Signal	Width	Direction	Description
aud_clk	[2N–1:0]	Input	Set this clock to 3.072 MHz that is synchronous to the extracted audio. In asynchronous mode, set this to any frequency above 3.072 MHz. Intel recommends that you set this clock to 50 MHz. For SD-SDI inputs, this mode of operation limits the core to embedding audio that is synchronous to the video. For HD-SDI inputs, this clock must either be generated from the optional 48 Hz output or the audio must be synchronous to the video. Set exclusive clock group to aud_clk and vid_clk to prevent unstable or flickering image.
aud_de	[2N–1:0]	Input	Assert this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core ignores this signal.
aud_ws	[2N–1:0]	Input	Assert this word select signal to provide framing for deserialization and to indicate left or right sample of channel pair.
aud_data	[2N–1:0]	Input	Internal AES data signal from the AES input module. In parallel mode, each audio pair is 32 bits wide. Total width in parallel mode is [(32*2N)–1:0].
	[(32*2N)–1:0]	Input	

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Embed IP core in Platform Designer (Standard).

Table 11. SDI Audio Embed Avalon-ST Audio Signals

n is the number of audio channels, the value starts from 0 to n-1.

Signal	Width	Direction	Description
aud(n)_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud(n)_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud(n)_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud(n)_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud(n)_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud(n)_channel	[7:0]	Input	Avalon-ST select signal. Use this signal to select a specific channel.
aud(n)_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

This table lists the register interface signals. The register interface is a standard 8-bit wide Avalon-MM slave.

Table 12. SDI Audio Embed Register Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the Avalon-MM register interface.
reg_reset	[0:0]	Input	Reset for the Avalon-MM register interface.
reg_base_addr	[5:0]	Input	Reset for the Avalon-MM register interface.
reg_burst_count	[5:0]	Input	Transfer size in bytes.
reg_waitrequest	[0:0]	Output	Wait request.
reg_write	[7:0]	Input	Write request.
reg_writedata	[0:0]	Input	Data to be written to target.
reg_read	[0:0]	Input	Read request.
reg_readdatavalid	[0:0]	Output	Requested read data valid after read latency.
reg_readdata	[7:0]	Output	Data read from target.

This table lists the direct control interface signals. These signals are exposed as ports if you turn off the **Include Avalon-MM Control Interface** parameter.

Table 13. SDI Audio Embed Direct Control Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the direct control interface.
audio_control	[7:0]	Input	Assert this 8-bit signal to enable the audio channels. Each bit controls one audio channel.
extended_control	[7:0]	Input	This signal does the same function as the extended control register.
video_status	[7:0]	Output	This signal does the same function as the video status register.
sd_edp_control	[7:0]	Output	This signal does the same function as the SD EDP control register.

continued...

Signal	Width	Direction	Description
audio_status	[7:0]	Output	This signal does the same function as the audio status register.
cs_control	[15:0]	Input	This signal does the same function as the channel status control register.
strip_control	[7:0]	Input	This signal does the same function as the strip control register. The Intel Quartus Prime Pro Edition software SDI Audio Intel FPGA IP does not support strip control.
strip_status	[7:0]	Output	This signal does the same function as the strip status register. The Intel Quartus Prime Pro Edition software SDI Audio Intel FPGA IP does not support strip status.
sine_freq_ch1	[7:0]	Input	This signal does the same function as the sine channel 1 frequency register.
sine_freq_ch2	[7:0]	Input	This signal does the same function as the sine channel 2 frequency register.
sine_freq_ch3	[7:0]	Input	This signal does the same function as the sine channel 3 frequency register.
sine_freq_ch4	[7:0]	Input	This signal does the same function as the sine channel 4 frequency register.
csram_addr	[5:0]	Input	Channel status RAM address.
csram_we	[0:0]	Input	Drive this signal high for a single cycle of reg_clk signal to load the value of the csram_data port into the channel status RAM at the address on the csram_addr port. If each input audio pair gets separate channel status RAMs, this signal addresses the RAM selected by the extended_control port.
csram_data	[7:0]	Input	Channel status data. This signal does the same function as the channel status RAM register in Table 4–9.

Related Information

- SDI Audio Embed Registers on page 26
- SDI Audio IP Register Interface Signals on page 25

5.2. SDI Audio Extract Signals

The following tables list the signals for the SDI Audio Extract IP core.

This table lists the clock recovery input and output signals.

Table 14. SDI Audio Extract Recovery Input and Output Signals

Signal	Width	Direction	Description
reset	[0:0]	Input	This signal resets the system.
fix_clk	[0:0]	Input	Assert this 200 MHz reference clock when you turn on the **Include Clock** parameter. If you do not turn on the **Include Clock** parameter, tie this signal low.
aud_clk_out	[0:0]	Output	The core asserts this 64 × sample rate clock (3.072 MHz audio clock) when you turn on the **Include Clock** parameter. You use this clock to clock the audio interface in synchronous mode.

continued...

Signal	Width	Direction	Description
			As the core creates this clock digitally, it is prone to higher levels of jitter.
aud_clk48_out	[0:0]	Output	The core asserts this sample rate clock when you turn on the **Include Clock** parameter.
aud_z	[0:0]	Output	The core asserts this signal to indicate the Z preamble.

This table lists the video input signals.

Table 15. SDI Audio Extract Video Input Signals

Signal	Width	Direction	Description
vid_clk	[0:0]	Input	The video clock that is typically 27 MHz for SD-SDI, 74.25 MHz or 74.17 MHz for HD-SDI, or 148.5 MHz or 148.35 MHz for 3G-SDI standards. You can use higher clock rates with the vid_datavalid signal.
vid_std	[1:0]	Input	Indicates the received video standard. Applicable for 3G-SDI, dual standard, and triple standard modes only. Set this signal to indicate the following formats: • 00b for 10-bit SD-SDI • 01b for 20-bit HD-SDI • 10b for 3G-SDI Level B • 11b for 3G-SDI Level A
vid_datavalid	[0:0]	Input	Assert this signal when the video data is valid.
vid_data	[19:0]	Input	This signal carries luma and chroma information. SD-SDI: • [19:10] Unused • [9:0] Cb,Y, Cr, Y multiplex HD-SDI and 3G-SDI Level A: • [19:10] Y • [9:0] C 3G-SDI Level B: • [19:10] Cb,Y, Cr, Y multiplex (link A) • [9:0] Cb,Y, Cr, Y multiplex (link B)
vid_locked	[0:0]	Input	Assert this signal when the video is locked.

This table lists the audio input and output signals.

Table 16. SDI Audio Extract Audio Input and Output Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Set this clock to 3.072 MHz that is synchronous to the extracted audio. For SD-SDI inputs, this mode of operation limits the core to extracting audio that is synchronous to the video. For HD-SDI inputs, you must generate this clock from the optional 48 kHz output or the audio must be synchronous to the video.
aud_ws_in	[0:0]	Input	Some audio receivers provide a word select output to align the serial outputs of several audio extract cores. In these circumstances, assert this signal to control the output timing of the audio extract externally, otherwise set it to 0. This signal must be a repeating cycle of high for 32 aud_clk cycles followed by low for 32 aud_clk cycles.

continued...

Signal	Width	Direction	Description
aud_de	[0:0]	Output	Assert this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core ignores this signal. The core asserts this data enable signal to indicate valid information on the aud_ws and aud_data signals. In synchronous mode, the core drives this signal high.
aud_ws	[0:0]	Output	The core asserts this word select signal to provide framing for deserialization and to indicate left or right sample of channel pair.
aud_data	[0:0]	Output	The core asserts this signal to extract the internal AES audio signal from the AES output module. In parallel mode, this signal is 32 bits wide.
	[31:0]	Output	

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Extract IP core in Platform Designer (Standard).

Table 17. SDI Audio Extract Avalon-ST Audio Signals

n is the number of audio channels, the value starts from 0 to n-1.

Signal	Width	Direction	Description
aud(n)_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud(n)_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud(n)_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud(n)_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud(n)_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud(n)_channel	[7:0]	Input	Avalon-ST select signal. Use this signal to select a specific channel.
aud(n)_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

This table lists the direct control interface signals. The direct control interface is internal to the SDI Audio Extract IP core.

Table 18. SDI Audio Extract Direct Control Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the direct control interface.
audio_control	[7:0]	Input	This signal does the same function as the audio control register.
audio_presence	[7:0]	Input	This signal does the same function as the audio presence register.
audio_status	[7:0]	Output	This signal does the same function as the audio status register.
sd_edp_presence	[7:0]	Output	This signal does the same function as the SD EDP presence register.
error_status	[7:0]	Output	This signal does the same function as the error status register.
error_reset	[15:0]	Input	Set any bit of this port high for a single cycle of reg_clk to clear the corresponding bit of the error_status signal.

continued...

Signal	Width	Direction	Description
			Setting any of bits [3:0] high for a clock cycle resets the entire 4-bit error counter.
fifo_status	[7:0]	Input	This signal does the same function as the FIFO status register.
fifo_reset	[7:0]	Input	Set high for a single cycle of reg_clk to clear the underflow or overflow field of the fifo_status signal.
clock_status	[7:0]	Input	This signal does the same function as the clock status register.
csram_addr	[5:0]	Input	Channel status RAM address. The contents of the selected address are valid on the csram_data signal after one cycle of reg_clk.
csram_data	[7:0]	Input	Channel status data. This signal does the same function as the channel status RAM.

Related Information

- SDI Audio Extract Registers on page 29
- SDI Audio IP Register Interface Signals on page 25

5.3. SDI Audio Clocked Input Signals

The following tables list the signals for the SDI Audio Clocked Input IP cores.

This table lists the input and output signals.

Table 19. SDI Audio Clocked Input Input and Output Signals

Signal	Width	Direction	Description
aes_clk	[0:0]	Input	Audio input clock.
aes_de	[0:0]	Input	Audio data enable.
aes_ws	[0:0]	Input	Audio word select.
aes_data	[0:0]	Input	Audio data input in internal AES format.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Clocked Input IP core in Platform Designer (Standard).

Table 20. SDI Audio Clocked Input Avalon-ST Audio Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud_ready	[0:0]	Input	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud_valid	[0:0]	Output	Avalon-ST valid signal. The core asserts this signal when it produces data.
aud_sop	[0:0]	Output	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud_eop	[0:0]	Output	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud_data	[23:0]	Output	Avalon-ST data bus. The core asserts this signal to transfer data.

This table lists the direct control interface signals. The direct control interface is internal to the audio extract component.

Table 21. SDI Audio Clocked Input Direct Control Interface Signals

Signal	Width	Direction	Description
channel0	[7:0]	Input	Indicates the channel number of audio channel 1.
channel1	[7:0]	Input	Indicates the channel number of audio channel 2.
fifo_status	[7:0]	Input	Drive bit 7 high to reset the clocked audio input FIFO buffer.
fifo_reset	[0:0]	Output	Assert this signal when the clocked audio input FIFO buffer overflows.

Related Information

SDI Audio IP Register Interface Signals on page 25

5.4. SDI Audio Clocked Output Signals

The following tables list the signals for the SDI Audio Clocked Output IP cores.

This table lists the input and output signals.

Table 22. SDI Audio Clocked Output Input and Output Signals

Signal	Width	Direction	Description
aes_clk	[0:0]	Input	Audio input clock.
aes_de	[0:0]	Output	Audio data enable.
aes_ws	[0:0]	Output	Audio word select.
aes_data	[0:0]	Output	Audio data input in internal AES format.

This table lists the Avalon-ST audio signals when you instantiate the SDI Audio Clocked Output IP core in Platform Designer (Standard).

Table 23. SDI Audio Clocked Output Avalon-ST Audio Signals

Signal	Width	Direction	Description
aud_clk	[0:0]	Input	Clocked audio clock. All the audio input signals are synchronous to this clock.
aud_ready	[0:0]	Output	Avalon-ST ready signal. Assert this signal when the device is able to receive data.
aud_valid	[0:0]	Input	Avalon-ST valid signal. The core asserts this signal when it receives data.
aud_sop	[0:0]	Input	Avalon-ST start of packet signal. The core asserts this signal when it is starting a new frame.
aud_eop	[0:0]	Input	Avalon-ST end of packet signal. The core asserts this signal when it is ending a frame.
aud_data	[23:0]	Input	Avalon-ST data bus. This bus transfers data.

Related Information

SDI Audio IP Register Interface Signals on page 25

5.5. SDI Audio IP Register Interface Signals

All SDI Audio IP cores use the same register interface signals.

The register interface is a standard 8-bit wide Avalon-MM slave.

Table 24. SDI Audio IP Register Interface Signals

Signal	Width	Direction	Description
reg_clk	[0:0]	Input	Clock for the Avalon-MM register interface.
reg_reset	[0:0]	Input	Reset for the Avalon-MM register interface.
reg_base_addr	[5:0]	Input	Reset for the Avalon-MM register interface.
reg_burst_count	[5:0]	Input	Transfer size in bytes.
reg_waitrequest	[0:0]	Output	Wait request.
reg_write	[7:0]	Input	Write request.
reg_writedata	[0:0]	Input	Data to be written to target.
reg_read	[0:0]	Input	Read request.
reg_readdatavalid	[0:0]	Output	Requested read data valid after read latency.
reg_readdata	[7:0]	Output	Data read from target.

6. SDI Audio Intel FPGA IP Registers

The following sections describe the registers for the SDI Audio IP cores.

6.1. SDI Audio Embed Registers

The following tables list the registers for the SDI Audio Embed IP core.

Table 25. SDI Audio Embed Register Map

Bytes Offset	Name
00h	Audio Control Register
01h	Extended Control Register
02h	Video Status Register
03h	SD EDP Control Register
04h	Channel Status Control Registers (3:0)
05h	Channel Status Control Registers (7:4)
06h	Strip Control Register(1)
07h	Strip Status Register(1)
08h	Sine Channel 1 Frequency
09h	Sine Channel 2 Frequency
0Ah	Sine Channel 3 Frequency
0Bh	Sine Channel 4 Frequency
0Ch	Audio Status Register
0Dh-0Fh	Reserved
10h-3Fh	Channel Status RAM (0×00), (0×01), ... (0×2F)

Table 26. SDI Audio Embed Registers

Bit	Name	Access	Description
Audio Control Register			
7:0	Audio group enable	RW	Enables the embedding of each audio group. When working with HD-SDI or 3G-SDI video, this register also enables the embedding of the audio control packet when one or more audio groups are enabled.

(1) The Intel Quartus Prime Pro Edition software SDI Audio Intel FPGA IP does not support strip control and strip status.

Bit	Name	Access	Description
Audio Control Register			
			The following bits correspond to the number of audio groups you specify: • Bit [1:0] = Audio group 1 • Bit [3:2] = Audio group 2 • Bit [5:4] = Audio group 3 • Bit [7:6] = Audio group 4

Extended Control Register			
2:0	Channel status RAM select	RW	When you specify the **Channel Status RAM** parameter to 2, this field selects the channel pair for the RAM written to by registers 10h to 3Fh. If you specify the **Channel Status RAM** parameter to 0 or 1, ignore this signal.
3	Unused	—	Reserved for future use.
4	Test sine generator enable	RW	When set to 1b, this bit ignores the audio inputs and uses the output of the sine generator as the data for each audio group.
6:5	Link AB Control	RW	This register applies only for 3G-SDI Level B standard. Controls which link the ancillary data is embedded in. • 00b = No data is embedded • 01b = Data is embedded only in Link B. • 10b = Data is embedded only in Link A (default value). • 11b = Data is embedded in Link A and Link B at the same time. When set to 11b, the IP core inserts new packets after any existing ancillary data on Link A and in the identical location on Link B. If the packet distribution of existing ancillary data on Link B differs, existing packets may be corrupted. In these circumstances, Intel recommends you use two separate instances of the ancillary embedder.
7	Unused	—	Reserved for future use.

Video Status Register			
7:0	Active channel	RO	Reports the detected video input standard. • Bits[7:5] = Picture structure code. Defined values for picture structure code are: — 001b = 486 or 576 line SD-SDI — 100b = 720 line HD-SDI — 101b = 1080 line HD-SDI — 010b = 1080 line 3G-SDI — 011b = 1080 line 3GA-SDI — 110b = 720 line 3GA-SDI — 111b = 720 line 3GB-SDI • Bit[4] = 0b—Interlace or segmented frame, 1b—Progressive. • Bits[3:0] = Frame rate code. Defined values for frame rate code (in Hz) are: — 0010b = 23.97 — 0011b = 24 — 0101b = 25 — 0110b = 29.97 — 0111b = 30 — 1001b = 50 — 1010b = 59.94 — 1011b = 60

SD EDP Control Register			
3:0	Enable SD EDP	RW	Enables the embedding of SD-SDI Extended Data Packets (EDP) for each audio group.
7:4	Enable SD ACP	RW	Enables the embedding of SD-SDI Audio Control Packets (ACP) for each audio group.

Channel Status Control Register			
7:0	CS mode select	RW	When set to 00b, the core keeps the existing channel status data. When set to 01b, the core replaces the channel status data with these default values: • Channel status byte 0: 0x8 • Channel status byte 1: 0x02 • Channel status byte 2–22: 0x00 • Channel status byte 23: 0xDD When set to 10b, the core replaces the data with the contents of the appropriate channel status RAM. The following bits correspond to the number of audio groups you specify: • Bit [1:0] = Audio group 1 • Bit [3:2] = Audio group 2 • Bit [5:4] = Audio group 3 • Bit [7:6] = Audio group 4

Strip Control Register			
3:0	Strip enable	RW	Enables the removal of both ACP and ADP (and any SD-SDI EDP) for each of the four audio groups.
7:4	Unused	—	Reserved for future use.

Strip Status Register			
3:0	Data packet present	RO 3:0	Reports which audio data groups are detected in the SDI stream. When in 3G-SDI Level B mode, this register reports the presence of audio on Link A (Link B should be a duplicate).
7:4	Control packet present	RO	Reports which audio control groups are detected in the SDI stream. When in 3G-SDI Level B mode, this register reports the presence of audio on Link A (Link B should be a duplicate).

Sine Channel *n* Frequency			
7:0	Sine channel frequency	RW	Defines the frequency of the generated audio.

Audio Status Register			
4	Frame lock	RO	Reports whether the video frame with the embedded audio is locked.

Channel Status RAM			
7:0	Channel status data	WO	Write accesses within the address range 10h to 3Fh to the channel status RAM. This field returns the 24 bytes of channel status for X channels starting at address 10h to 27h, and the 24 bytes of channel status for Y channels starting at address 28h to 3Fh.

Related Information

SDI Audio Embed Signals on page 17

6.2. SDI Audio Extract Registers

The following tables list the registers for the SDI Audio Extract IP core.

Table 27. SDI Audio Extract Register Map

Bytes Offset	Name
00h	Audio Control Register
01h	Audio Presence Register
02h	Audio Status Register
03h	SD EDP Presence Register
04h	Error Status Register
05h	Reserved
06h	FIFO Status Register
07h	Clock Status Register
08h-09h	Reserved
10h-3Fh	Channel Status RAM (0×00), (0×01), ... (0×2F)

Table 28. SDI Audio Extract Registers

Bit	Name	Access	Description
Audio Control Register			
0	Enable	RW	Enables the audio extraction component and internal AES output.
3:1	Extract pair	RW	Defines the audio pair that the component extracts. For example: • [000] = Extract the first channel pair of audio signal • [111] = Extract the eighth channel pair of audio signal
4	Extract pair MSB	RW	For 3G-SDI Level A standard, this field extends the extract pair field to allow for future implementations with 32 embedded audio channels. For 3G-SDI Level B standard, this field selects the active video half of the 3G multiplex.
5	Mute	RW	Drive this register high to mute the audio output.
7:6	Unused	—	Reserved for future use.
Audio Presence Register			
3:0	Data packet present	RO	Reports which audio data groups are detected in the SDI stream. The following bits correspond to the number of audio groups detected: • Bit [0] = Audio group 1 • Bit [1] = Audio group 2 • Bit [2] = Audio group 3 • Bit [3] = Audio group 4
7:4	Control packet present	RO	Reports which audio control packets are detected in the SDI stream.
Audio Status Register			
3:0	Active channel	RO	Reflects the lower four bits of the active channel field of the audio control packet.
4	Asynchronous	RO	Reflects the asx bit (synchronous mode bit) of the RATE (sampling rate) field of the audio control packet.
6:5	Sample rate	RO	Reports the X1 and X0 bits of the sample rate code from the RATE field of the audio control packet.
7	Status valid	RO	Set to 1b when the audio control packet is present in the video stream.
SD EDP Presence Register			
3:0	EDP Present	RO	Reports which audio extended data groups are detected in the SD-SDI stream.
7:4	Unused	—	Reserved for future use.
Error Status Register			
3:0	Error counter	RW	Counts up to 15 errors since last reset. Write 1b to any bit of this field to reset the entire counter to zero.
4	Ancillary CS fail	RW	Indicates that an error has been detected in the ancillary packet checksum. This bit stays set until cleared by writing 1b to this register.

continued...

Error Status Register			
5	Ancillary parity fail	RW	Indicates that an error has been detected in at least one of the parity fields: • ancillary packet parity bit • audio sample parity bit (for SD-SDI) • AES sample parity bit (for HD-SDI This bit stays set until cleared by writing 1b to this register.
6	Channel status CRC fail	RW	Indicates that an error has been detected in the channel status CRC. This bit stays set until cleared by writing 1b to this register.
7	Audio packet ECRC fail	RW	Indicates that an error has been detected in the ECRC that forms part of the HD audio data packet. This bit stays set until cleared. To clear, write 1b to this register.

FIFO Status Register			
6:0	FIFO fill level	RO	Reports the amount of data in either the audio output FIFO or the Avalon-ST audio FIFO when the optional Avalon-ST Audio interface is used.
7	Overflow/underflow	RW	This register bit goes high if one of the following occurs (based on the output mode used): • underflow or overflow of the audio output FIFO • overflow of the Avalon-ST audio FIFO This register always goes high at the beginning, so you must clear the audio FIFO first for the register to indicate underflow or overflow.

Clock Status Register			
4:0	Offset	RO	Defines the frequency of the generated audio.
6:5	Unused	—	Reserved for future use.
7	74.17-MHz video clock	RO	To create a 48-kHz signal synchronous to the video clock, you must detect whether a 1 or 1/1.001 video clock rate is used. If you detect a 1/1.001 video clock rate, this field returns high.

Channel Status RAM			
7:0	Channel status data	WO	Read accesses within the address range 10h to 3Fh to the channel status RAM. This field returns the 24 bytes of channel status for X channel starting at address 10h, and the 24 bytes of channel status for Y channel starting at address 28h.

6.3. SDI Clocked Audio Input Registers

The following tables list the registers for the SDI Clocked Audio Input IP core.

Table 29. SDI Clocked Audio Input Register Map

Bytes Offset	Name
00h	Channel 0 Register
01h	Channel 1 Register
02h	FIFO Status Register
03h	FIFO Reset Register

Table 30. SDI Clocked Audio Input Registers

Bit	Name	Access	Description
Channel 0 Register			
7:0	Channel 0	RW	The user-defined channel number of audio channel 0.

Channel 1 Register			
7:0	Channel status RAM select	RW	The user-defined channel number of audio channel 1.

FIFO Status Register			
7:0	Active channel	RO	This sticky bit reports the overflow of the clocked audio input FIFO.

FIFO Reset Register			
6:0	Unused	WO	Reserved for future use.
7	FIFO reset	WO	Resets the clocked audio FIFO.

6.4. SDI Clocked Audio Output Registers

The following tables list the registers for the SDI Clocked Audio Output IP core.

Table 31. SDI Clocked Audio Output Register Map

Bytes Offset	Name
00h	Channel 0 Register
01h	Channel 1 Register
02h	FIFO Status Register
03h	FIFO Reset Register

Table 32. SDI Clocked Audio Output Registers

Bit	Name	Access	Description
Channel 0 Register			
7:0	Channel 0	RW	The user-defined channel number of audio channel 0.

Channel 1 Register			
7:0	Channel status RAM select	RW	The user-defined channel number of audio channel 1.

FIFO Status Register			
7:0	Active channel	RO	This sticky bit reports the overflow of the clocked audio output FIFO.

FIFO Reset Register			
6:0	Unused	WO	Reserved for future use.
7	FIFO reset	WO	Resets the clocked audio FIFO.

7. SDI Audio Intel FPGA IP User Guide Archives

IP versions are the same as the Intel Quartus Prime Design Suite software versions up to v19.1. From Intel Quartus Prime Design Suite software version 19.2 or later, IP cores have a new IP versioning scheme.

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.0	SDI Audio Intel FPGA IP User Guide
16.0	SDI Audio IP Cores User Guide
14.0	SDI Audio IP Cores User Guide

8. Document Revision History for the SDI Audio Intel FPGA IP User Guide

Document Version	Intel Quartus Prime Version	IP Version	Changes
2019.07.24	19.2	19.1.0	• Updated introductory description of SDI Audio Intel FPGA IP cores in *SDI Audio Intel FPGA IP Overview* chapter. • Added notes on availability of SDI Audio Intel FPGA IP cores in the Intel Quartus Prime Pro Edition software and Intel Quartus Prime Standard Edition software in the *SDI Audio Intel FPGA IP Overview* chapter. • Added *Release Information* section in the *SDI Audio Intel FPGA IP Overview* chapter. • Moved release information and device family support information into *Release Information* section. • Renamed item *Version* to *IP Version* and added item *Intel Quartus Prime Version* in Table: *SDI Audio Intel FPGA IP Cores Current Release Information*. • Added support information for Intel Arria 10 GX, Intel Arria 10 GT, and Intel Arria 10 SX device families in Table: *SDI Audio Intel FPGA IP Cores Current Release Information*. • Removed support information for Arria® II GX, Arria V, Cyclone IV GX, Cyclone V, Stratix IV GX, and Stratix V FPGA device families in Table: *SDI Audio Intel FPGA IP Cores Current Release Information*. • Removed references to "Standard" associated with Platform Designer, added note on instantiating IP through IP Catalog using the IP parameter editor, and removed notes on instantiating IP in RTL in the *Instantiating the SDI Audio Intel FPGA IP* section. • Added Table: *SDI Audio IP Cores to Generate* in *Simulating the Testbench* section. • Updated procedure in *Simulating the Testbench* section. • Updated description for parameter **Async Audio Interface** to indicate that this mode supports an audio clock equal to or higher than 64 × sample rate, added description that the parameters **Frequency of fix_clk** and **Cleanly remove existing audio** are not supported in the Intel Quartus Prime Pro Edition software, and added parameter **Parallel Audio Interface** in Table: *SDI Audio Embed Parameters*. • Added parameters **Async Audio Interface** and **Parallel Audio Interface** in Table: *SDI Audio Extract Parameters*. • Added parallel mode width and description for signal `aud_data` in Table: *SDI Audio Embed Audio Input Signals* and Table: *SDI Audio Extract Audio Input and Output Signals*.

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			• Added description to signals `strip_control` and `strip_status` that the Intel Quartus Prime Pro Edition software SDI Audio Intel FPGA IP does not support strip control and strip status in Table: *SDI Audio Embed Direct Control Interface Signals*. • Added note for the strip control register and strip status register that the Intel Quartus Prime Pro Edition software SDI Audio Intel FPGA IP does not support strip control and strip status in Table: *SDI Audio Embed Register Map*. • Removed *SDI Audio Intel FPGA IP Design Example* chapter. *Note:* Intel provides a design example with the SDI Audio Embed and Extract IP cores in the Intel Quartus Prime Standard Edition software only. Refer to the user guide for the previous IP core version (18.0) for information. • Added explanation on the new IP versioning scheme in the *SDI Audio Intel FPGA IP User Guide Archives* chapter.
2018.05.16	18.0	18.0	• Rebranded as Intel. • Edited the `vid_std` settings for SDI Audio Extract IP core. The correct settings should be 10b for 3G-SDI Level B and 11b for 3G-SDI Level A. • Removed Audio group presence register (bit 3:0). The register is no longer supported in the current IP code.

Date	Version	Changes
May 2016	2016.05.30	• Added a new signal for the SDI Audio Extract IP core: `aud_z[0:0]`. This signal indicates the Z preamble. • Added the default values that replace the channel status data when you set the CS mode select register to 01b. • Added link to an archived version of the *SDI Audio IP Cores User Guide*. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2014	2014.06.30	• Created a separate user guide for the SDI Audio IP cores. • Removed the SDI Audio IP section from the *SDI IP Core User Guide*. • Added new registers for the SDI Audio Embed IP core: SD EDP Control, Strip Control, and Strip Status. • Added new signals for the SDI Audio Embed IP core: `extended_control`, `strip_control`, and `strip_control`. • Added a new register for the SDI Audio Extract IP core: SD EDP Presence. • Added a new signal for the SDI Audio Extract IP core: `sd_edp_presence`.