Device-Specific Power Delivery Network (PDN) Tool
User Guide
Chapter 1. User Guide for the Device-Specific Power Delivery Network (PDN) Tool

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This user guide provides a brief overview of the various tabs in the device-specific PDN tool. You can quickly and accurately design a robust power delivery network by calculating an optimum number of capacitors that meet the target impedance requirements for a given power supply.

The PDN tool only supports Microsoft Excel 2007 and newer.

Overview

PCB designers must estimate the number, value, and type of decoupling capacitors needed to develop an efficient PCB decoupling strategy during the early design phase, without going through extensive pre-layout simulations. Altera’s Power Delivery Network (PDN) tool provides these critical pieces of information.

Because all device-specific PDN tools have a similar user interface, this document serves as the user guide to all Altera® device-specific PDN tools. The device families supported by the tool are shown at the top of the Release Notes tab; in this case, Stratix® V, Arria® V, Arria II GZ, Cyclone® V, and Cyclone IV devices.

For more information about Altera’s general purpose PDN tool with no device support, refer to the Power Delivery Network (PDN) Tool User Guide.

The PDN tool is a Microsoft Excel-based spreadsheet tool used to calculate an impedance profile based on user inputs. For a given power supply, the spreadsheet requires only basic design information, such as the board stackup, transient current information, and ripple specifications to calculate the impedance profile and the optimum number of capacitors to meet the desired impedance target (Z_{TARGET}). The tool also provides device- and power rail-specific PCB decoupling cut-off frequency (F_{EFFECTIVE}). The results obtained through the spreadsheet tool are intended only as a preliminary estimate and not as a specification. For an accurate impedance profile, Altera recommends a post-layout simulation approach using any of the available EDA tools, such as Sigrity PowerSI, Ansoft SIWave, Cadence Allegro PCB PI, etc.

Application of the Tool

The purpose of the PDN tool is to help the design of a robust power delivery network for the device in the targeted device family by determining an optimum number, type, and value of decoupling capacitors needed for selected device/power rail to meet the desired Z_{TARGET} up to F_{EFFECTIVE}. This spreadsheet tool is useful for exploring the various what-if scenarios during the early design phase, without extensive and time consuming pre-layout analysis.
**PDN Decoupling Methodology Review**

This section describes general PCB decoupling methodology and explains in detail the two parameters ($Z_{TARGET}$ and $F_{EFFECTIVE}$) provided by the PDN tool for guiding PCB decoupling design.

**PDN Circuit Topology**

The PDN tool is based on a lumped equivalent model representation of the power delivery network topology. Figure 1–1 shows a schematic representation of the circuit topology, modeled as part of the tool. The PDN impedance profile is the impedance-over-frequency looking from the device side.

*Figure 1–1. PDN Topology*

For first order analysis, the voltage regulator module (VRM) can be simply modeled as a series connected resistor and inductor, as shown in Figure 1–1. At low frequencies, up to approximately 50 KHz, the VRM has a very low impedance and is capable of responding to the instantaneous current requirements of the FPGA. The equivalent series resistance (ESR) and equivalent series inductance (ESL) values can be obtained from the VRM manufacturer. At higher frequency, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement. PCB decoupling capacitors are used for reducing the PDN impedance up to tens of MHz. The on-board discrete decoupling capacitors provides the required low impedance depending on the capacitor intrinsic parasitics ($R_{CN}$, $C_{CN}$, $L_{CN}$) and the capacitor mounting inductance ($L_{mntN}$). The inter-planar capacitance between the power-ground planes typically has lower inductance than the discrete decoupling capacitor network, making it more effective at higher frequencies (tens of MHz). As frequency increases (tens of MHz and above), the PCB decoupling capacitors become less effective. The limitation comes from the parasitic inductance seen with respect to the FPGA, which consists of capacitor mounting inductance, PCB spreading inductance, ball grid array (BGA) via inductance, and packaging parasitic inductance. All these parasitics are modeled in this PDN tool to capture the effect of the PCB decoupling capacitors accurately. To simplify the circuit topology, all parasitics are represented with lumped inductors and resistors despite the distributed nature of PCB spreading inductance.
Z\text{TARGET}

According to Ohm’s law, voltage drop across a circuit is proportional to the current flow through the circuit and impedance of the circuit. The transient component of PDN current gives rise to voltage fluctuation within the PDN, which may lead to logic and timing issues. You can reduce excessive voltage fluctuation by reducing PDN impedance. One design guideline is target impedance Z\text{TARGET}.

Z\text{TARGET} is defined using the maximum allowable voltage ripple and transient current and is calculated as follows:

**Equation 1–1.**

\[
Z_{\text{TARGET}} = \frac{\text{VoltageRail} \times (\%\text{Ripple})}{100} \cdot \frac{\text{MaxTransientCurrent}}{\text{MaxTotalCurrent}}
\]

For example, to reliably decouple a 3.3-volt power rail that allows 5% of AC ripple and a maximum 2 A current draw, 50% of which is transient current, the desired target impedance is:

**Equation 1–2.**

\[
Z_{\text{TARGET}} = \frac{(3.3)(0.05)}{2 \times 0.5} = 0.165\Omega
\]

To accurately calculate the Z\text{TARGET} for any power rail, the following information must be known:

- The maximum transient current requirements for all devices in the system that are powered by the power rail under consideration. You can obtain this information from manufacturers of the respective devices. You can calculate the maximum transient current of a device using the maximum total current and the transient current percentage.

- The percentage of transient current is signal-pattern dependent. It changes as the output signal pattern varies for drivers using the power rail. You need to choose the value that represents the worst-case scenario of the power rail. For information about recommended settings, refer to the table in the **Introduction** tab of the PDN tool. Table 1–1 on page 1–4 is from the PDN tool for a Stratix IV GX device. It lists the Stratix IV GX default power supply voltage, the recommended settings of the transient current percentage, and the allowable voltage ripple for power rails.

You can obtain accurate estimations on the maximum total current for Altera devices using the Altera PowerPlay Early Power Estimator (EPE) tool or the Quartus® II PowerPlay Power Analyzer tools. You can download the EPE tool for your target Altera device from the PowerPlay Early Power Estimator (EPE) and Power Analyzer.
The maximum allowable AC ripple on the power rail as a percentage of the supply voltage. The maximum allowable AC ripple varies for different power rails. For information about the recommended maximum allowable AC ripple for power rails, refer to the table in the Introduction tab of the PDN tool. Table 1–1 shows ripple information for the power rails of Stratix IV GX devices.

Table 1–1. Settings for the Stratix IV GX Device Power Rails (Note 1)

<table>
<thead>
<tr>
<th>Rail Name</th>
<th>Voltage (V)</th>
<th>Allowable Ripple Percentage (%)</th>
<th>Transient Current Percentage (%)</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>0.9 V</td>
<td>5%</td>
<td>50%</td>
<td>Core</td>
</tr>
<tr>
<td>VCCIO</td>
<td>1.2 V - 3.0 V</td>
<td>5%</td>
<td>50%</td>
<td>I/O Bank</td>
</tr>
<tr>
<td>VCCPD</td>
<td>2.5 V</td>
<td>5%</td>
<td>50%</td>
<td>I/O Pre-Driver</td>
</tr>
<tr>
<td>VCCA_PLL</td>
<td>2.5 V</td>
<td>3%</td>
<td>20%</td>
<td>PLL (Analog)</td>
</tr>
<tr>
<td>VCCD_PLL</td>
<td>0.9 V</td>
<td>3%</td>
<td>20%</td>
<td>PLL (Digital)</td>
</tr>
<tr>
<td>VCC_CLKIN</td>
<td>2.5 V</td>
<td>5%</td>
<td>50%</td>
<td>Diff Clock Input</td>
</tr>
<tr>
<td>VCCR</td>
<td>1.1 V</td>
<td>3%</td>
<td>30%</td>
<td>XCVR RX (Analog)</td>
</tr>
<tr>
<td>VCCT</td>
<td>1.1 V</td>
<td>3%</td>
<td>30%</td>
<td>XCVR TX (Analog)</td>
</tr>
<tr>
<td>VCCA</td>
<td>3.0 V</td>
<td>5%</td>
<td>10%</td>
<td>XCVR High Voltage Power</td>
</tr>
<tr>
<td>VCCH_GXB</td>
<td>1.5 V</td>
<td>3%</td>
<td>10%</td>
<td>XCVR I/O Buffer Block</td>
</tr>
<tr>
<td>VCCL_GXB</td>
<td>1.1 V</td>
<td>3%</td>
<td>20%</td>
<td>XCVR Clock Block</td>
</tr>
<tr>
<td>VCCHIP</td>
<td>0.9 V</td>
<td>5%</td>
<td>50%</td>
<td>PCIe Hard IP (Digital)</td>
</tr>
<tr>
<td>VCCPT</td>
<td>1.5 V</td>
<td>3%</td>
<td>20%</td>
<td>Programmable Power Tech</td>
</tr>
<tr>
<td>VCCAUX</td>
<td>2.5 V</td>
<td>3%</td>
<td>20%</td>
<td>Programmable Power Tech Aux</td>
</tr>
</tbody>
</table>

Note to Table 1–1:
(1) For more information about power rail functions, refer to the pin connection guidelines for the selected device family.

**F_{EFFECTIVE}**

As shown in Figure 1–1 on page 1–2, a capacitor reduces PDN impedance by providing a least-impedance route between power and ground. Impedance of a capacitor at high frequency is determined by its parasitics (ESL and ESR). For a PCB-mount capacitor, the parasitics include not only the parasitic from the capacitors themselves but also the parasitics associated with mounting, PCB spreading, and packaging. Therefore, PCB capacitor parasitics are generally higher than those of on-package decoupling capacitor and on-die-capacitance. Decoupling using PCB capacitors becomes ineffective at high frequency. Using PCB capacitors for PDN decoupling beyond their effective frequency range brings little improvement to PDN performance and raises the bill of materials (BOM) cost.

To help reduce over-design of PCB decoupling, this release of the PDN tool provides a suggested PCB decoupling design cut-off frequency \( F_{EFFECTIVE} \) as another guideline. It is calculated using the PCB, package, and die parasitics. You only need to design PCB decoupling that keeps \( Z_{EFF} \) under \( Z_{TARGET} \) up to \( F_{EFFECTIVE} \).
F_EFFECTIVE may not be enough when the Altera FPGA device shares a power rail with another device. The noise generated from other device propagates along the PDN and affects FPGA device performance. The frequency of the noise is determined by the transfer impedance between the noise source and the FPGA device, and can be higher than F_EFFECTIVE. Reducing PDN parasitic inductance and increasing the isolation between the FPGA device and noise source reduces this risk. You must perform a transfer impedance analysis to clearly identify any noise interference risk.

**Major Tabs of the PDN Tool**

Figure 1–2 shows the tabs of the PDN tool spreadsheet. Table 1–2 describes the PDN tool tabs.

You can input design-specific information in the various tabs to arrive at a very accurate PDN profile for a given power supply. The following sections describe the major tabs for the tool.

<table>
<thead>
<tr>
<th>Tab</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Release Notes</td>
<td>This tab provides the legal disclaimers, the revision history of the tool, and the user agreement.</td>
</tr>
<tr>
<td>Introduction</td>
<td>This tab shows the schematic representation of the circuit that is modeled as part of the PDN tool. The tab also provides related information, such as a quick start instruction, recommended settings for some power rails and a brief description of decoupling design procedures under different power supply connection schemes.</td>
</tr>
<tr>
<td>System Decap</td>
<td>This tab provides an interface to enter the user power sharing scheme for selected a FPGA device and derive the decoupling for the device, based on the input.</td>
</tr>
<tr>
<td>Stackup</td>
<td>This tab provides an interface to enter user stackup information into the PDN tool.</td>
</tr>
<tr>
<td>Decap Selection</td>
<td>This tab provides an interface to input the various parameters and observe the resultant impedance profile. This is the main user interface to the tool.</td>
</tr>
<tr>
<td>Library</td>
<td>This tab points to various libraries (capacitor, dielectric materials, and so on) that are called by other tabs. You can change the default values listed as part of these libraries.</td>
</tr>
<tr>
<td>BGA Via</td>
<td>This tab provides an interface to calculate the BGA mounting inductance based on design-specific via parameters and the number of vias.</td>
</tr>
<tr>
<td>Plane Cap</td>
<td>This tab provides an interface to calculate the plane capacitance based on design-specific parameters.</td>
</tr>
<tr>
<td>Cap Mount</td>
<td>This tab provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for two different capacitor orientations (Via on Side [VOS] and Via on End [VOE]).</td>
</tr>
<tr>
<td>X2Y Mount</td>
<td>This tab provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for X2Y type capacitors.</td>
</tr>
<tr>
<td>BOM</td>
<td>This tab provides a summary of the final capacitor count needed to meet the target impedance.</td>
</tr>
<tr>
<td>Enlarged_Graph</td>
<td>This tab provides an enlarged view of the Z-profile shown in Decap_Selection tab.</td>
</tr>
</tbody>
</table>

You can input design-specific information in the various tabs to arrive at a very accurate PDN profile for a given power supply. The following sections describe the major tabs for the tool.
**System Decap**

You can determine the decoupling of selected FPGA devices based on the power sharing scheme entered in the **System Decap** tab, shown in Figure 1–3.

The **System Decap** tab is divided into the following sections:

1. Family/Device/Power sharing scheme selection
2. Power rail data / power sharing configuration
3. Via length and number of via pair
4. Regulator data
5. Rail group summary
6. Decoupling selection
7. Result summary
8. Additional buttons

**Figure 1–3. System Decap Tab**

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**Family/Device/Power Sharing Scheme Selection**

Select the Family/Device/Power sharing scheme in this section using the pull-down list of a selected cell. The tool updates the list of the power rails and power sharing scheme in the power rail data/configuration section, based on your selection. The tool also updates contents in power rail/power sharing configuration section accordingly.
Power Rail Data and Power Sharing Scheme

Enter the power supply voltage, current consumption of each power rail, and setup device power sharing scheme in this section. This section is divided into two areas (Figure 1–4). Area 1 is for the device power rail information and Area 2 is for configuring the power sharing scheme.

### Figure 1–4. Power Rail Data and Power Sharing Scheme Section

<table>
<thead>
<tr>
<th>Group #</th>
<th>Regulator / Separator</th>
<th>Parent Group</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rail</td>
<td>Voltage</td>
<td>I_{max}</td>
<td>switcher</td>
<td>filter</td>
<td>switcher</td>
<td>filter</td>
</tr>
<tr>
<td>VCCINT</td>
<td>1.2</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD1</td>
<td>2.5</td>
<td></td>
<td>x/related</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD2</td>
<td>2.5</td>
<td></td>
<td>x/related</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD3</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD4</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD5</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD6</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD7</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD8</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCA1</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCA2</td>
<td>2.5</td>
<td></td>
<td>x</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD_PLL1</td>
<td>1.2</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCCD_PLL2</td>
<td>1.2</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Enter the power rail voltage and current consumption of every power rail listed in Area 1.

You must enter the total current consumption of related power rails before you can use the system decoupling function.

Each column in Area 2 represents a power group in your system. You add or remove a power group using the Add Group or Remove Group button. The first row of each group is the Regulator/Separator type. Set the source type for the power group and available options from the pull-down list as switcher, linear, filter.

The second row is the Parent Group type. The available options for this row are None and the number representing all listed power groups. You input power sharing hierarchy in this column. You set the power rail connection using the remaining rows.

The PDN tool defines the power sharing tree using the Parent/Child power group. A power group is a child power group if that power group attaches to another power group. The other power group is the parent group in this case. A parent group can have multiple child groups. However, a child group cannot have a child group. A parent power group number is required for the child group. The parent group number of a parent power group is assigned to None because the group has no parent group.

The available options are:

- " " — Device rail does not connect to the power group.
- x — Device rail connects to the power group.
- x/related — Device rail connects to the group, and its activity is related to other rails that connect to the same group for VCCIO and VCCPD rails. You must select x/related if that VCCIO/VCCPD power rail is related to other rails within the same power rail group.
Two IO rails are related if their output activities are in sync. For example, when two VCCIO rails are assigned to the same memory interface. The maximum current will usually be reached at the same time for these related rails. As the result, the total current of related rails equals the sum of current of all shared rails. The total current of unrelated rails is calculated using the root-mean-square (RMS) method.

The PDN tool sets the default power rail sharing configuration based on the selected Altera recommended power sharing scheme listed above. Make changes to better match your design.

**Power Via Length and Number**

You set the power Via length and number of Power/Ground Via pair for each power group in this section. Select the PCB layer where the power group is located and the tool calculates the Via length using the PCB stackup information from the **Stackup** tab.

An incorrect input may result in overly pessimistic or optimistic decoupling results. You must use the layer number of power rails that consumes most of the current if the power rails in the group are not located in the same layer.

**Regulator Data**

Enter the regulator parameters such as DC supply voltage at VRM input, switcher VRM efficiency, ambient temperature and $\theta_{JA}$ of linear VRM in this section. The tool calculates VRM input current and linear VRM junction temperature $T_J$. This section provides information that helps you select the VRM module. Data input in this section does not affect the decoupling.

**Rail Group Summary**

You find a list of calculated key parameters, such as voltage, total current, transient current percentage, allowed voltage ripple, $Z_{TARGET}$ and $F_{EFFECTIVE}$ of all power groups in this section.

**Decoupling Selections**

You let the tool to derive the decoupling for all power groups using the **Decouple all rails** button. You can also select the power group you want to decouple from a pull-down list and click the **Decouple only this group** button. The tool will derive the decoupling for a selected power group.

**Result Summary**

You can find the list of the number and type of capacitors used for each group, and the summary of all the capacitors used.

**Additional Buttons**

There are two buttons on this page, **Export** and **Restore Default**. Use the **Export** button to get a summary of system decouple resorts. Click the **Restore Default** button to update all entries within this tab to the system default.
Recommended Flow for Deriving Decoupling for FPGA System using the System_Decap Tab

To use the System_Decap tab, perform the following steps:

1. Set up the stack up information in the Stackup tab.
2. Select the Altera device family/device.
3. Select the decoupling scheme. The tool will update the power rail connection configuration to the scheme recommended in the PCG.
4. Ensure that default parameters, such as power rail configuration, relativity of power rails within the same power group, power group layer, number of power/ground Via pairs, DC voltage supply for VRM module, or the decoupling cap location match your system and make necessary changes.
5. Enter the projected current consumption of each power rail.
6. Click the Decouple All Groups button to generate a decoupling scheme for all power groups listed, or select the group to be decoupled from the drop-down menu of the Decouple only this group cell, and click the Decouple the Selected Group button.

You may see violations if you check the impedance profile of the decoupling scheme derived in the System_Decap tab, located in the Decap_Selection tab. This is because the protocol used in System_Decap tab has optimizations for power sharing scenario.

Stackup

Enter the PCB stackup information of your design in the Stackup tab, shown in Figure 1–5. This tab updates related data in the BGA_Via, Plane_Cap, Cap_Mount and the X2Y_Mount tabs. You also use the stackup information in this tab for the System_Decap tab. Brief instructions are provided at the beginning of the tab. Follow the instructions to fill in the content for this tab.

![Figure 1–5. Stackup Tab](image-url)
The Stackup tab consists of the following sections:

- Stackup Data
- Stackup Stub
- Full Stackup

Stackup Data

Enter board dimension data and other parameters, such as board dimension, board stackup settings, power via and dielectric material, in the Stackup Data section.

Stackup Stub

The content in this section is updated based on the settings in Stackup Configuration, in the Stackup Data section. Enter the thickness of the metal/dielectric material for each layer in this section. The stackup shown in this section is used as the basic unit to construct the complete PCB stackup.

Full Stackup

This section lists the complete stackup of your board. You can modify content in the section to better match your board design. The last column in the section is PWR plane types. In a single rail analysis case, assign the layer where the power rail is located as target, and the ground layer that the power rail refers to as reference.

The Stackup tab contains the following buttons:

- Construct Stackup
- Import Geometries
- Proceed to System Decap

Construct Stackup

Click the Construct Stackup button and the tool populates the Full Stackup section to the number of layers defined in the Stackup Data section, using the blocks listed in the Stackup Stub section.

Import Geometries

Click the Import Geometries button and the tool updates geometry parameters in the BGA_Via, Plane_Cap, Cap_Mount, and X2Y_Mount tabs using your input from the Stackup Data section. The tool also checks that the PWR plane column in the Full Stackup section has only one target layer, and provides a warning for this error.

Proceed to System Decap

After you click the Proceed to System Decap button, you will proceed to System_Decap tab.
BGA Via

The BGA_Via tab calculates the vertical via loop inductance under the BGA pin field. Figure 1–6 is a snapshot taken from the tool.

Figure 1–6. BGA_Via Tab

You enter the layout-specific information, such as the via drill diameters, via length, via pitch, and the number of power/ground via pairs under the BGA. The tool calculates the effective via loop inductance and resistance value. You can save the change made to the tab, restore the changes, and restore the tab back to the default settings.
Plane Cap

The Plane_Cap tab calculates the distributed plane capacitance in microfarads (µF) that is developed between the power/ground planes based on the parallel plate capacitor equation. Figure 1–7 shows the Plane_Cap tab.

You enter the design specific information, such as plane dimensions, plane configuration, and dielectric material used. The tool calculates a plane capacitance value. You can save custom values, restore custom values, and restore the default settings.
Cap Mount

The **Cap_Mount** tab, shown in Figure 1–8, calculates the capacitor mounting inductance seen by the decoupling capacitor.

**Figure 1–8. Cap_Mount Tab**

The capacitor mounting calculation is based on the assumption that the decoupling capacitor is a two-terminal device. The capacitor mounting calculation is applicable to any two-terminal capacitor with the following footprints: 0201, 0402, 0603, 0805, and 1206. You enter all the information relevant to your layout and the tool provides a mounting inductance for a capacitor mounted on either the top or bottom layer of the board. Depending on the layout, you can choose between VOE (Via on End) or VOS (Via on Side) to achieve an accurate capacitor mounting inductance value.

If you plan to use a footprint capacitor other than a regular two-terminal capacitor or X2Y capacitor for decoupling, you can skip the **Cap_Mount** tab and directly enter the capacitor parasitics and capacitor mounting inductance in the **Library** tab (under the **Custom** field in the **Decoupling Cap** section of the library). As with the other tabs, you can save the changes made to the tab, restore the changes, and restore the tab back to the default settings.
X2Y Mount

The X2Y_Mount tab, shown in Figure 1–9, calculates the capacitor mounting inductance seen by the X2Y decoupling capacitor.

Figure 1–9. X2Y_Mount Tab

You enter all the information relevant to your layout and the tool provides a mounting inductance for a X2Y capacitor mounted on either the top or bottom layer of the board. As with the other tabs, you can save the changes made to the tab, restore the changes, and restore the tab back to the default settings.
Library

The **Library** tab stores all the device parameters that are referred to in the other tabs. Figure 1–10 shows the **Library** tab.

![Library Tab](image)

This tab is divided into the following sections:

- Two-Terminal Decoupling Capacitors (High/Mid Frequency)
- X2Y Decoupling Capacitors (High/Mid frequency)
- Bulk Capacitors (Mid/Low Frequency)
- BGA Via and Plane Capacitance
- VRM Library
- Spreading R, L Parasitics
- Dielectric Material Library
- User Set $F_{\text{EFFECTIVE}}$
- Stackup

You can change each of the default values listed in the respective sections to meet the specific needs of your design.
Two-Terminal Decoupling Capacitors
The decoupling capacitors section contains the default ESR and ESL values for the various two-terminal capacitors in different footprints (0201, 0402, 0603, 0805, and 1206). You also have the option of either modifying the default values or entering your own commonly used custom values in the Custom field. If you are using a capacitor with a footprint that is not available in the tool, you must use the Custom field to enter the capacitor parasitics and the corresponding mounting inductance.

The decoupling capacitors section also provides the option for the user defined capacitors (such as User1,...,User4). You can define the ESR and ESL parasitics for the various footprints and enter the corresponding capacitor value in the Decap_Selection tab. Choose the corresponding footprint when defining the capacitor values.

Bulk Capacitors
The bulk capacitors section contains the commonly used capacitor values for decoupling the power supply at mid/low frequencies. You can change the default values to reflect the parameters specific to the design.

X2Y Decoupling Capacitors
The X2Y decoupling capacitors section contains the default ESR and ESL values for the various X2Y capacitors in different footprints (0603, 0805, 1206, and 1210). You also can replace the default ESR and ESL values with your own commonly used custom values.

BGA Via and Plane Capacitance
The BGA via and plane capacitance section provides an option to directly enter the values for effective via loop inductance under the BGA and plane capacitance during the pre-layout phase when no design-specific information is available.

If you have access to design-specific information, you can ignore this section and enter the design-specific information in the Plane_Cap and BGA_Via tabs that calculate the plane capacitance and the BGA via parasitics, respectively.

VRM Library
The VRM section lists the default values for both the linear and switcher regulators. You can change the VRM parasitics listed under the linear/switcher rows or add the custom parasitics for the VRM relevant to the design in the Custom field.

Spreading R, L Parasitics
The spreading R, L library provides various options for the default effective spreading inductance values that the decoupling capacitors see with respect to the FPGA based on the quality of the PDN design. You can choose a Low value of effective spreading inductance if you have optimally designed your PDN Network. Optimum PDN design involves implementing the following design rules:
■ PCB stackup that provides a wide solid power/ground sandwich for a given supply with a thin dielectric between the planes. This minimizes the current loop, which reduces the spreading inductance. The thickness of the dielectric material between the power/ground pair directly influences the amount of spreading/loop inductance that a decoupling cap can see with respect to the FPGA.

■ Placing the capacitors closer to the FPGA from an electrical standpoint.

■ Minimizing via perforations in the power/ground sandwich in the current path from the decoupling caps to the FPGA device.

Due to layout and design constraints, the PDN design may not be optimal. In this case, you can choose either a Medium or High value of spreading R and L. You also have the option of changing the default values or using the Custom field listed in the library specific to the design.

**Dielectric Material Library**

The dielectric materials section lists the dielectric constant values for the various commonly used dielectric materials. These values are used in the plane capacitance calculations listed under the Plane_Cap tab. You can change the values listed in this section.

If you change the default values listed in the various sections in the Library tab, you can save the changes by clicking Save Custom. You can restore the default library by clicking Restore Default located at the top right-hand corner of the Library page. You can also restore the saved custom library by clicking Restore Custom.

**User Set $F_{\text{EFFECTIVE}}$**

You must decouple to a $F_{\text{EFFECTIVE}}$ higher than what is calculated for the power rails of some Altera device families. In this case, you must set the $F_{\text{EFFECTIVE}}$ option to Override in the Decap_Selection tab, and the PDN tool will then use the $F_{\text{EFFECTIVE}}$ value entered here.
Decap Selection

The Decap_Selection tab, shown in Figure 1–11, is where you perform the analysis for the PCB decoupling design. The user interface shown here is from the PDN tool for the Stratix IV device family.

Figure 1–11. Decap_Selection Tab

This tab is divided into the following sections:

- Family/Device/Power Rail Information
- Component Parameters Setting
- Electric Parameters and Design Guidelines
- Decoupling Capacitor (High/Mid Frequency)
- Decoupling Capacitor (Bulk)
- ZEFF Plot
Family/Device/Power Rail Information

You select the Family/Device/Power rail to work in this field. A pull-down menu with the names of the available devices and power rails for the Altera device family selected by the tool is shown when you click the corresponding cell. The tool validates the selected device/power rail combination. A warning is shown beneath the field if an invalid combination is chosen (Figure 1–12).

![Figure 1–12. Device/Power Rail Information](image)

Component Parameters Setting

You can either enable or disable the following components of the PDN network shown in Figure 1–13.

![Figure 1–13. Parameter Settings for PDN Components](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VRM</td>
<td>To disable this component, select Ignore. To enable the VRM parasitics, select Linear, Switcher, or Custom.</td>
</tr>
<tr>
<td>Spreading</td>
<td>Based on the design, you can select either Low, Medium, High, or a Custom value for the effective spreading R, L values that the decoupling capacitors see with respect to the FPGA. You can also ignore the spreading inductance by selecting Ignore. Ignoring the spreading inductance leads to an optimistic result and is not an accurate representation of the impedance profile that the FPGA sees. The Ignore option helps you understand that the spreading inductance in combination with the BGA via inductance is the limiting factor from a PCB perspective to decouple the FPGA at high frequencies. Be careful when choosing the Ignore option while coming up with a final capacitor count.</td>
</tr>
<tr>
<td>BGA Via</td>
<td>Based on the design, you can choose to Ignore the BGA via component or to Calculate the effective via inductance based on the layout. If you are in the middle of layout, you can directly enter the effective loop R, L via parasitics in the Library tab and choose the Custom setting under BGA Via to include the via parasitics.</td>
</tr>
<tr>
<td>Plane Capacitance</td>
<td>Based on the design, you can either choose to Ignore the inter-planar capacitance between the power and ground plane, or Calculate the plane capacitance based on the layout. If you are in the middle of layout, you can directly enter the plane capacitance in the Library tab and choose the Custom setting under the Plane Cap to include the plane capacitance parasitics.</td>
</tr>
</tbody>
</table>

Table 1–3 describes the PDN components.
Electric Parameters and Design Guidelines

The PDN tool calculates $Z_{TARGET}$ based on the user inputs in this field. The PDN tool also displays $F_{EFFECTIVE}$ that is derived based on the PCB stack-up and power rail information (Figure 1–14). The details regarding the calculation procedure are described in “$Z_{TARGET}$” on page 1–3 and “$F_{EFFECTIVE}$” on page 1–4.

Figure 1–14. Electric Parameters and Design Guidelines

<table>
<thead>
<tr>
<th>Target Impedance</th>
<th>Units</th>
<th>Value</th>
<th>Legend</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (Min)</td>
<td>V</td>
<td>1.1</td>
<td>N/A</td>
</tr>
<tr>
<td>$I_{MAX}$</td>
<td>A</td>
<td>5.425</td>
<td>N/A</td>
</tr>
<tr>
<td>Transient Current (%)</td>
<td>%</td>
<td>50</td>
<td>N/A</td>
</tr>
<tr>
<td>Ripple (+/-)</td>
<td>%</td>
<td>5</td>
<td>N/A</td>
</tr>
<tr>
<td>$F_{EFFECTIVE}$</td>
<td>Calculate MHz</td>
<td>4.6</td>
<td>$F_{EFFECTIVE}$</td>
</tr>
<tr>
<td>$Z_{TARGET} = \Delta V / \Delta I$</td>
<td>$\Omega$</td>
<td>0.0203</td>
<td>$Z_{TARGET}$</td>
</tr>
</tbody>
</table>

You need to enter information for:

- Power Supply Voltage (min)
- $I_{MAX}$
- Transient Current (%)
- Allowable Voltage Ripple Percentage ($\pm$)
- $F_{EFFECTIVE}$ Option

The percentage of transient current is signal-pattern dependent. Use a calculation, simulation, or a measurement to obtain the transient current (dynamic current) values. You can use the Quartus II PowerPlay Power Analyzer (PPPA) to accurately estimate the transient current values when you import design specific activity test vectors for analysis. If none of these methods are routinely available, Altera recommends the values available in the Introduction tab in each Device-Specific PDN tool for your design.

You must set the $F_{EFFECTIVE}$ option to Calculate if you want the tool to decouple to the calculated $F_{EFFECTIVE}$. You need to set the option to override if you want the tool to decouple to the designated $F_{EFFECTIVE}$.

$F_{EFFECTIVE}$ will increase as the spreading inductance is reduced. For a good PCB layout there is less ESL for the PCB decoupling capacitors, and they are able to affect the PDN impedance at higher frequencies. For a less optimal PCB layout with high spreading inductance, there is more ESL for the PCB decoupling capacitors and they are less effective in affecting the PDN impedance at high frequencies. Therefore, $F_{EFFECTIVE}$ is lower when parasitic inductance, such as plane spreading inductance and mounting inductance, is high.

The tool then calculates $Z_{TARGET}$ based on the user input from related fields and displays the results in the column below. The tool calculates the effective frequency for the rail selected. You can also set $F_{EFFECTIVE}$ to a frequency you select. To do so, you must set the $F_{EFFECTIVE}$ option to Override and enter the frequency in the Library tab.
Decoupling Capacitor (High/Mid Frequency)
You can select the various decoupling capacitors, both two-terminal and X2Y types, based on footprint, layer, and orientation to meet the target impedance for the mid to high frequency. The capacitance value for the X2Y capacitor may be different from that of the two-terminal capacitor. A warning message of “Wrong Footprint” is displayed if you choose a wrong combination of capacitance and footprint. The VOE and VOS option do not affect the mounting inductance for X2Y type capacitors because their via locations are symmetric. You also have the option of defining custom capacitor values (User1, ..., User4) needed for high/mid frequency decoupling specific to the design. You cannot change the capacitor parasitics (ESR and ESL) in this tab. This can only be done in the Library tab.

Decoupling Capacitor (Bulk)
You can select the desired bulk capacitors based on the footprint for the low to mid frequency decoupling need. You can only change the parasitics of the bulk decoupling capacitors and define the mounting inductance specific to the design in the Library tab. You also have the option of defining custom capacitor values (User5 and User6) for low/mid frequency decoupling specific to the design.

$Z_{\text{EFF}}$ Plot
The effective impedance that the Altera device encounters is shown in (Figure 1–15). Other information, such as $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$ are also shown in the plot, along with the impedance profile of components such as capacitors, VRM, and BGA via, within the PDN system. The plot is updated automatically when related parameters are changed.

Figure 1–15. $Z_{\text{EFF}}$ Plot

As provided in other tabs, you can save and restore the final capacitor count and other settings for a specific set of assumptions. There is also flexibility to revert back to default settings.
**Auto Decouple**

You can use the **Auto Decouple** function to derive the desired decoupling network. To use this function, click **Auto Decouple** after entering all the required information, and the tool will automatically select decoupling capacitors to meet the $Z_{\text{TARGET}}$ set based on the information you provide.

**Verify Solution**

You can use the **Verify Solution** function to check if your design meets the decoupling requirement. The tool calculates PDN impedance $Z_{\text{EFF}}$ up to the $F_{\text{EFFECTIVE}}$ and warns you about any violations found.
BOM

Figure 1–16 shows the BOM tab.

Figure 1–16. BOM Tab

When the analysis is done, you can print out the final $Z_{\text{EFF}}$ profile and capacitor count to achieve the profile by clicking Print BOM on the top right corner. It defaults to the default printer assigned in the File/Print menu. You can also export the data as an .xls file by clicking Export Data.
Enlarged_Graph

In the Enlarged_Graph tab, you can view the enlarged Z-profile plot, shown in Figure 1–17. The PDN tool switches to this tab when you click on the Z-profile plot in the Decap_Selection tab. You can go back to the Decap_Selection tab by clicking on the Return button.

Design PCB Decoupling Using the PDN Tool

PCB decoupling keeps PDN $Z_{\text{EFF}}$ smaller than $Z_{\text{TARG}}$ with the properly chosen PCB capacitor combination up to the frequency where the capacitor on the package and die take over the PDN decoupling. This section describes the procedure of designing PCB decoupling using the PDN tool in different power rail configurations. This section also provides design examples using the Stratix IV device PDN tool.

Pre-Layout Instructions

The PDN tool provides an accurate estimate of the number and types of capacitors needed to design a robust power delivery network, regardless of where you are in the design phase. However, the accuracy of the results depends highly on the user inputs for the various parameters.

If you have finalized the board stack-up and have access to board database and layout information, you can step through the tabs and enter the required information to arrive at an accurate decoupling scheme.

In the pre-layout phase of the design cycle, when no specific information about the board stack-up and board layout is known, you can follow the instructions in the following sections to explore the solution space when finalizing key design parameters such as stack-up, plane size, capacitor count, capacitor orientation, and so on.
In the pre-layout phase, you can ignore the Plane_Cap and Cap_Mount tabs and go directly to the Library tab when you do not have the layout information. Figure 1–18 shows the fields in the Library tab that you will use to enter the various parameters. If available, enter the values shown in Figure 1–18 in the Library tab. To use the default values, go directly to the Decap_Selection tab to begin the analysis.

**Figure 1–18. Library Tab Fields**

Notes to Figure 1–18:
The numbers in the figure correspond to the following steps 1, 2, 3, 4, 5.

1. Enter the ESR, ESL, and Lmnt values for the capacitors under the Custom field.
2. Enter the effective BGA via (loop) parasitics for the power supply being decoupled.
3. Enter the plane capacitance seen by the power/ground plane pair on the board for the power supply under Plane Cap.
4. Enter the VRM parasitics, if available, under the Custom row.
5. Enter the effective spreading inductance seen by the decoupling capacitors in Custom row.

**Derive Decoupling in a Single-Rail Scenario**

A power supply connects to only one power rail on the FPGA device in a single-rail scenario. The PDN noise is created by the transient current of the single rail. You determine \( Z_{\text{TARGET}} \) and \( F_{\text{EFFECTIVE}} \) based on the parameters related to the selected rail only.

The PDN tool provides two ways to derive a decoupling network. You can set up the tool with the information needed and let the tool derive the PDN decoupling for your system. You can also manually enter the information and derive decoupling manually.
You must follow the steps below to derive the desired capacitor combination:

1. Select the device/power rail to work with.
2. Select the parameter setting for the PDN components.
3. Enter the electric parameters to set $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$.
4. Derive the PCB decoupling scheme.

The red numbers in Figure 1–19 show the field to work with in each of these steps. For more information on these fields, refer to “Decap Selection” on page 1–18.

**Figure 1–19. Decap Selection Tab in a Single-Rail Design**

In Step 2, the PDN tool uses the inductance and resistance value calculated in the BGA_Via tab if you choose the Calculate option for the BGA via. Incorrect parameters may negatively affect the derived decoupling design. These values are calculated using the parameters you entered in the BGA_Via tab. You must check the BGA_Via tab to ensure the numbers you entered—especially the number and length of the BGA power via pair—matches the settings of the power rail selected in Step 1.
In Step 3, you need to have a good estimate of the parameters entered to derive the proper decoupling guidelines ($Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$). Although you need to determine those guidelines based on the worst-case scenario, pessimistic settings result in hard-to-achieve guidelines and over design of your PCB decoupling. For the recommended settings of the percentage of transient current and maximum allowable voltage ripple for selected power rail, refer to Table 1–1 on page 1–4.

In Step 4, you must adjust the number and value of the PCB capacitors in the Decoupling Capacitor (Mid/High Frequency) and Decoupling Capacitor (Bulk) fields to keep the plotted $Z_{\text{EFF}}$ below $Z_{\text{TARGET}}$ until $F_{\text{EFFECTIVE}}$. You can derive the decoupling for the selected power rail manually. You can also select the Auto Decouple button and let the PDN tool derive the decoupling scheme. If you are not able to find a capacitor combination that meets your design goal, you can try to change the parameters at Step 2; for example, reducing the BGA via inductance used in the Calculate option by reducing the BGA via length in the BGA_VIA tab and using the low option for plane spreading. These changes reduce parasitic inductance and make it easier to achieve your decoupling goal. To achieve the low spreading setting, you must place the mid to high frequency PCB capacitors close to the FPGA device. You also must minimize the dielectric thickness between the power and ground plane.

If you are not able to meet the $Z_{\text{TARGET}}$ requirement with the above changes, the PDN in your design may have reached its physical limitation under the parameters entered in Step 3. Go back to Step 3 and re-examine these parameters to check if they are too pessimistic.

The design shown in Figure 1–20 is a decoupling example for S4GX230KF40 VCC power rail. Assume that the minimum voltage supply is 0.9 V, $I_{\text{MAX}}$ is 7 A, transient current is 50% of $I_{\text{MAX}}$, and the maximum allowable ripple is 3% of supply voltage. The $V_{\text{CC}}$ rail has 50 power BGA vias. The length of BGA via is assumed to be 60 mil.
The PDN tool calculated that $Z_{\text{TARGET}}$ is 0.0077 $\Omega$ and $F_{\text{EFFECTIVE}}$ is 24.91 MHz. Figure 1–20 shows one of the capacitor combinations that you can select to meet the design goal. Figure 1–20 is the enlarged view of the $Z_{\text{EFF}}$ plot. As shown in the plot, $Z_{\text{EFF}}$ remains under $Z_{\text{TARGET}}$ up to $F_{\text{EFFECTIVE}}$. There are many combinations, but the ideal solution is to minimize the quantity and the type of capacitors needed to achieve a flat impedance profile below $Z_{\text{TARGET}}$.

**Figure 1–20. Enlarged Plot of Z_{eff} Using the Figure 1-16 Design**

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**Derive Decoupling in the Power-Sharing Scenarios**

It is a common practice that several power rails in the FPGA device share the same power supply. For example, you can connect VCCIO, VCCPD, VCCPGM, and VCC_CLKIN rails that require the same supply voltage to the same PCB power plane. This can be required by the design, such as in the memory interface case. This can also come from the needs to reduce BOM cost. You can use the System_Decap tab to facilitate the decoupling design for the power sharing scenarios. Refer to “System Decap” on page 1–6 for details.

When deriving decoupling capacitors for multiple FPGAs sharing the same power plane, each FPGA should be analyzed separately using the PDN tool. For each FPGA design, combine the required power rails as described above and analyze the decoupling scheme as if the FPGA was the only device on the power rail. Repeat for each of the remaining FPGAs on the board.

High frequency decoupling capacitors are meant to provide the current needed for AC transitions and must be placed in a close proximity to the FPGA power pins. Thus, the PDN tool should be used to derive the required decoupling capacitors for the unique power requirements for each FPGA on the board.

The power regulators must be able to supply the total combined current requirements for each load on the supply, but the decoupling capacitor selections should be analyzed on a single FPGA basis.
This chapter provides additional information about the document and Altera.

**Document Revision History**

The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| February 2014  | 1.1     | ■ Added note to first page that the PDN tool only supports Excel 2007 and newer.  
■ Updated the “Overview” section. |
| December 2012  | 1.0     | ■ Updated for Stratix V, Arria V, Arria II GZ, Cyclone V, and Cyclone IV device use and published with new part number.  
■ Updated the “Feffective” section.  
■ Added the “User Set Feffective” section.  
■ Added the “System Decap” section.  
■ Added the “Stackup” section.  
■ Updated the “Family/Device/Power Rail Information” section.  
■ Updated the “Electric Parameters and Design Guidelines” section.  
■ Added the “Auto Decouple” section.  
■ Added the “Verify Solution” section.  
■ Added the “Enlarged_graph” section.  
■ Updated the “Derive Decoupling in a Single-Rail Scenario” section.  
■ Updated the “Derive Decoupling in the Power-Sharing Scenarios” section.  
■ Updated Figure 1–2, Figure 1–10, Figure 1–11, Figure 1–12, Figure 1–14, and Figure 1–18. |
| September 2012 | 1.1     | Updated the “Derive Decoupling in the Power-Sharing Scenarios” section.     |
| July 2009      | 1.0     | Initial release.                                                          |

**How to Contact Altera**

To locate the most up-to-date information about Altera products, refer to the following table.

<table>
<thead>
<tr>
<th>Contact (1)</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
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<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Product literature</td>
<td>Website</td>
<td><a href="http://www.altera.com/literature">www.altera.com/literature</a></td>
</tr>
</tbody>
</table>
## Typographic Conventions

The following table shows the typographic conventions this document uses.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, <strong>Save As</strong> dialog box. For GUI elements, capitalization matches the GUI.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, \qdesigns directory, <strong>D:</strong> drive, and <strong>chiptrip.gdf</strong> file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Indicate document titles. For example, <em>Stratix IV Design Guidelines</em>.</td>
</tr>
<tr>
<td><strong>italic type</strong></td>
<td>Indicates variables. For example, <strong>n + 1</strong>. Variable names are enclosed in angle brackets (<strong>&lt; &gt;</strong>). For example, <strong>&lt;file name&gt;</strong> and <strong>&lt;project name&gt;.pof</strong> file.</td>
</tr>
<tr>
<td>Initial Capital Letters</td>
<td>Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.</td>
</tr>
<tr>
<td>“Subheading Title”</td>
<td>Quotation marks indicate references to sections within a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”</td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, <strong>data1</strong>, <strong>tdi</strong>, and <strong>input</strong>. The suffix <strong>n</strong> denotes an active-low signal. For example, <strong>resetn</strong>. Indicates command line commands and anything that must be typed exactly as it appears. For example, c:\qdesigns\tutorial\chiptrip.gdf. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <strong>SUBDESIGN</strong>), and logic function names (for example, <strong>TRI</strong>).</td>
</tr>
<tr>
<td><strong>An angled arrow</strong></td>
<td>An angled arrow instructs you to press the Enter key.</td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., and so on</td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td><strong>Bullets</strong></td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td><strong>The hand</strong></td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td><strong>A question mark</strong></td>
<td>A question mark directs you to a software help system with related information.</td>
</tr>
<tr>
<td><strong>A caution</strong></td>
<td>The feet direct you to another document or website with related information.</td>
</tr>
<tr>
<td><strong>A warning</strong></td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td><strong>The envelope</strong></td>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
</tr>
</tbody>
</table>

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**Note to Table:**

(1) You can also contact your local Altera sales office or sales representative.