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1. Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide

This user guide provides a brief overview of the various tabs in the device-specific PDN tool 2.0. It provides conceptual information and is common for all devices. You can quickly and accurately design a robust power delivery network with the PDN tool 2.0. This is done by calculating an optimum number of capacitors that meet the target impedance requirements for a given power supply.

Note: The PDN tool 2.0 only supports Microsoft Excel 2007 and newer, and either US or UK English language.

Table 1. PDN Tool 2.0 Software Verification

<table>
<thead>
<tr>
<th>Operating System</th>
<th>Excel Versions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Windows 10 Professional (64-bit)</td>
<td>Office 2010 and 2016</td>
</tr>
<tr>
<td>Windows 8.1 Professional (64-bit)</td>
<td>Office 2010 and 2013</td>
</tr>
<tr>
<td>Windows 7 (64-bit)</td>
<td>Office 2010</td>
</tr>
</tbody>
</table>

1.1. Overview

Intel's PDN tool 2.0 helps PCB designers estimate the number, value, and type of decoupling capacitors needed to develop an efficient PCB decoupling strategy. It allows you to do this during the early design phase, without going through extensive pre-layout simulations.

The PDN tool 2.0 is a Microsoft Excel-based spreadsheet that calculates an impedance profile based on your input. For a given power supply, the spreadsheet only requires basic design information to calculate the impedance profile and the optimum number of capacitors to meet the desired impedance target ($Z_{TARGET}$). Basic design information includes the board stackup, transient current information, and ripple specifications, for example. The tool also provides the device- and power rail-specific PCB decoupling cut-off frequency ($F_{EFFECTIVE}$). The results obtained through the PDN tool 2.0 are intended only as a preliminary estimate and not as a specification. For an accurate impedance profile, Intel recommends a post-layout simulation approach using any available EDA tool, such as Cadence PowerSI, Ansys SIWave, and Cadence Allegro PCB PI.
There are two versions of the PDN tool 2.0. One version is for 20-nm devices (which also includes the 14-nm Intel® Stratix® 10 devices), and one version is for all other devices listed below. The device families supported by the Intel device-specific PDN tool 2.0 are shown at the top of the Release Notes tab and they include:

- **14-nm devices:**
  - Intel Stratix 10 GX, SX, MX, TX, DX, NX
- **20-nm devices:**
  - Intel Arria® 10
  - Intel Cyclone® 10 GX
- **28-nm devices:**
  - Arria V
  - Arria V GZ
  - Cyclone V
  - Stratix V
- **40-nm devices:**
  - Arria II GZ
- **55-nm devices:**
  - Intel MAX® 10
- **60-nm devices:**
  - Cyclone IV E and GX

**Related Information**
Power Distribution Network Tools

**1.2. PDN Decoupling Methodology Review**

The PDN tool 2.0 provides two parameters for guiding PCB decoupling design: $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$.

**1.2.1. PDN Circuit Topology**

The PDN tool 2.0 is based on a lumped equivalent model representation of the power delivery network topology.
For a first order analysis, the VRM can be simply modeled as a series-connected resistor and inductor as shown above. This is a result of the typical proportional, integral, derivative (PID) voltage regulation loop compensation configuration of many regulators. The VRM has a very low impedance and can respond to the instantaneous current requirements of the FPGA up to between 50 kHz and 150 kHz, depending on the voltage regulation loop crossover (0 dB) frequency.

The equivalent series resistance (ESR) and equivalent series inductance (ESL) values can be obtained from the VRM manufacturer. At higher frequencies, the VRM impedance is primarily inductive, making it incapable of meeting the transient current requirement.

PCB decoupling capacitors are used for reducing the PDN impedance up to 50-100 MHz. The on-board discrete decoupling capacitors provide the required low impedance. This depends on the capacitor-intrinsic parasitics ($R_{CN}$, $C_{CN}$, $L_{CN}$) and the capacitor mounting inductance ($L_{mntN}$). The inter-planar capacitance between the power-ground planes typically has lower inductance than the discrete decoupling capacitor network, making it more effective at higher frequencies up to 100 MHz. As frequency increases, the PCB decoupling capacitors become less effective. The limitation comes from the parasitic inductance seen with respect to the FPGA. FPGA parasitic inductance includes capacitor mounting inductance, PCB spreading inductance, ball grid array (BGA) via inductance, and packaging parasitic inductance. All of these parasitics are modeled in the PDN tool 2.0 to capture the effect of the PCB decoupling capacitors accurately. To simplify the circuit topology, all parasitics are represented with lumped inductors and resistors despite the distributed nature of PCB spreading inductance.

### 1.2.1.1. $Z_{\text{TARGET}}$

The change of dynamic component of PDN current gives rise to voltage fluctuation within the PDN, which may lead to logic and timing issues. You can reduce excessive voltage fluctuation by reducing PDN impedance. One design guideline is target impedance, $Z_{\text{TARGET}}$. In the frequency domain, voltage fluctuation across a circuit at a frequency is proportional to the current flow through the circuit, and the impedance of
the circuit at the frequency according to Ohm’s law. \( Z_{\text{TARGET}} \) is defined using the maximum allowable noise tolerance and dynamic current change, and is calculated as follows.

**Figure 2.** \( Z_{\text{TARGET}} \) Equation

\[
Z_{\text{TARGET}} = \frac{\text{Voltage Rail} \times \left( \frac{\text{Noise Tolerance}\%}{100} \right)}{\text{Maximum Dynamic Current Change}}
\]

For example, the dynamic current of a 1.8 V power rail is 2 A. The worst case dynamic current change is 50% of the dynamic current. The noise tolerance of the power rail is 5% of the nominal voltage. The desired PDN target impedance for decoupling design is calculated as follows:

**Figure 3.** \( Z_{\text{TARGET}} \) Example Equation

\[
Z_{\text{TARGET}} = \frac{1.8 \times 0.5}{2 \times 0.5} = 0.9 \Omega
\]

To accurately calculate the \( Z_{\text{TARGET}} \) for any power rail, you must know the following information:

- The maximum dynamic current change requirements for the FPGA that is powered by the power rail under consideration. You can obtain this information from respective device datasheet. You can calculate the maximum dynamic current change of a device using the maximum dynamic current and the dynamic current change percentage.

  *Note:* The dynamic current is intended to parameterize the high-frequency current draws required to provide the energy for CMOS transistors changing state. In the case of the core rail, the transients are generated by switching inside the FPGA core. Thus, a design which involves extensive logical switching generates higher % transients (dynamic current change) than a more static design. The dynamic current change magnitude can be higher if the dynamic current is higher. For information about default settings of the dynamic current change percentage for major FPGA rails, refer to the table in the **Introduction** tab of the PDN tool 2.0.

  *Note:* You can obtain accurate estimations on the maximum dynamic current for Intel FPGA devices using the Early Power Estimator (EPE) tool or the Intel Quartus® Prime software power Analyzer tools. When using the data from the EPE, be sure to use only the dynamic power for each section for the PDN calculation.

- The maximum allowable noise tolerance on the power rail is given as a percentage of the supply voltage.

Device switching activity leads to transient noise (high frequency spikes) seen on the power supply rails. This noise can cause functionality issues if they are too high. The noise must be damped within a range defined as a percentage of power supply voltage. The recommended values for the maximum allowable noise tolerance are listed in the respective device datasheet and in the **Introduction** tab of the PDN tool 2.0. Different rails have different specifications because of their sensitivity to the transient voltage noise as well as how much current is used by the power rail.

Refer to the **Introduction** tab of the PDN tool 2.0 for more information about \( Z_{\text{TARGET}} \).
### Table 2. Settings for the Intel Stratix 10 Device Power Rails

This information is from the PDN tool 2.0 for a Intel Stratix 10 device.

<table>
<thead>
<tr>
<th>Rail Name</th>
<th>Default Voltage (V)</th>
<th>Noise Tolerance (%)</th>
<th>Dynamic Current Change (%)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>0.8 - 0.94 (1)</td>
<td>5</td>
<td>30 - 50</td>
<td>Core (30% for high dynamic current; 50% for low dynamic current)</td>
</tr>
<tr>
<td>VCCERAM</td>
<td>0.9</td>
<td>5</td>
<td>50</td>
<td>Programmable Power Tech Aux</td>
</tr>
<tr>
<td>VCCR_GXB</td>
<td>1.03/1.12 (1)</td>
<td>3</td>
<td>30</td>
<td>L-Tile and H-Tile Transceiver RX Analog</td>
</tr>
<tr>
<td>VCCT_GXB</td>
<td>1.03/1.12 (1)</td>
<td>2</td>
<td>60</td>
<td>L-Tile and H-Tile Transceiver TX Analog</td>
</tr>
<tr>
<td>VCCRT_GXE</td>
<td>0.9</td>
<td>2</td>
<td>30</td>
<td>E-Tile Transceiver RX Analog</td>
</tr>
<tr>
<td>VCCRT_GXP</td>
<td>0.9</td>
<td>2</td>
<td>30</td>
<td>P-Tile Transceiver TX Analog</td>
</tr>
<tr>
<td>VCCPT</td>
<td>1.8</td>
<td>5</td>
<td>50</td>
<td>Programmable Power Tech</td>
</tr>
<tr>
<td>VCCA_PLL</td>
<td>1.8</td>
<td>5</td>
<td>10</td>
<td>PLL Analog</td>
</tr>
<tr>
<td>VCCH_GXB</td>
<td>1.8</td>
<td>3</td>
<td>15</td>
<td>L-Tile and H-Tile Transceiver I/O Buffer Block</td>
</tr>
<tr>
<td>VCCH_GXE</td>
<td>1.1</td>
<td>2</td>
<td>30</td>
<td>E-Tile Transceiver I/O Buffer Block</td>
</tr>
<tr>
<td>VCCH_GXP</td>
<td>1.8</td>
<td>2</td>
<td>30</td>
<td>P-Tile Transceiver I/O Buffer Block</td>
</tr>
<tr>
<td>VCCIO</td>
<td>1.2/1.25/1.35/1.5/1.8</td>
<td>5</td>
<td>100</td>
<td>I/O Banks</td>
</tr>
<tr>
<td>VCCP</td>
<td>0.8 - 0.94 (1)</td>
<td>5</td>
<td>33</td>
<td>Periphery Power Supply</td>
</tr>
<tr>
<td>VCCIO_UIB</td>
<td>1.2</td>
<td>2</td>
<td>100/71 (2)</td>
<td>Host Memory Buffer I/O Universal Interface Bus</td>
</tr>
<tr>
<td>VCCBAT</td>
<td>1.2/1.5/1.8</td>
<td>5</td>
<td>100</td>
<td>Battery Back-up Power Supply</td>
</tr>
</tbody>
</table>

### Related Information
- Early Power Estimator (EPE)
- Pin Connection Guidelines

(1) For more information about power rail functions, refer to the Pin Connection Guidelines for the selected device family.

(2) If each VCCIO_UIB (BL or TL) is individually designed, use 100% of the total dynamic current.
If both VCCIO_UIBs (BL and TL) are combined:
- If both HBM operations are coherent, use 100% of the total dynamic current.
- If both HBM operations are non-coherent, use 71% of the total dynamic current.
The \( F_{\text{EFFECTIVE}} \) for VCCIO_UIB at package level is 2 MHz to meet target impedance.
1.2.1.2. \( F_{\text{EFFECTIVE}} \)

As previously described, a capacitor reduces PDN impedance by providing a least-impedance route between power and ground for transient current. Impedance of a capacitor at high frequency is determined by its parasitics (ESL and ESR). For a PCB with capacitors mounted, the parasitics include not only the parasitic from the capacitors themselves but also those associated with mounting, PCB spreading, and packaging. Therefore, PCB capacitor parasitics are generally higher than on-die capacitor parasitics. As a result, decoupling using PCB capacitors becomes ineffective at higher frequencies. Using PCB capacitors for PDN decoupling beyond their effective frequency range brings no improvement to PDN performance and raises the bill of materials (BOM) cost.

To help reduce over-design of PCB decoupling, this release of the PDN tool provides a suggested PCB decoupling design cut-off frequency (\( F_{\text{EFFECTIVE}} \)) as another guideline. You only need to design PCB decoupling that keeps \( Z_{\text{EFF}} \) under \( Z_{\text{TARGET}} \) up to \( F_{\text{EFFECTIVE}} \). \( Z_{\text{EFF}} \) is the impedance profile of the PCB design and includes all PDN-related design parasitics, including:

- VRM R and L
- PCB spreading R and L
- Plane R and C
- Decoupling capacitors
- BGA via R and L

\( F_{\text{EFFECTIVE}} \) defines the effective frequency of on-board decoupling capacitors.

Refer to Troubleshooting \( Z_{\text{EFF}} \) if the \( Z_{\text{EFF}} \) is too high or the number of capacitors for decoupling becomes too high.

**Note:** \( F_{\text{EFFECTIVE}} \) may not be enough when the Intel FPGA device shares a power rail with another device. The noise generated from other devices propagates along the PDN and affects FPGA device performance. The frequency of the noise is determined by the transfer impedance between the noise source and the FPGA device, and can be higher than \( F_{\text{EFFECTIVE}} \). Reducing PDN parasitic inductance and increasing the isolation between the FPGA device and noise source reduces this risk. You must perform a transfer impedance analysis to clearly identify any noise interference risk.

**Related Information**

- Troubleshooting \( Z_{\text{EFF}} \) on page 33
- For more information about the PDN decoupling methodology behind the PDN design tool, refer to the Power Delivery Network Design Using Altera PDN Design Tools online course.

### 1.2.2. Major Tabs of the PDN Tool 2.0

The tabs at the bottom of the PDN tool 2.0 application help you calculate your impedance profile.
Table 3. PDN Tool 2.0 Tabs

<table>
<thead>
<tr>
<th>Tab</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Release_Notes</td>
<td>Provides legal disclaimers, the revision history of the tool, and the user agreement.</td>
</tr>
</tbody>
</table>
| Introduction   | Displays the schematic representation of the circuit that is modeled as part of the PDN tool 2.0. It also provides the following related information:  
• quick start instructions  
• recommended settings for some power rails  
• a brief description of decoupling design procedures under different power supply connection schemes |
| System_Decap   | The principal tab that allows you to decouple your system. It displays by default when you launch the application. This tab provides an interface to enter your power sharing scheme for a selected FPGA device and derive the decoupling based on the input. |
| Stackup        | Provides an interface to enter your stackup information into the PDN tool. |
| Library        | Points to various libraries (capacitor, dielectric materials, and so on) that are called by other tabs. You can change the default values listed as part of these libraries. |
| BGA_Via        | Provides an interface to calculate the BGA mounting inductance based on design-specific via parameters and the number of vias. |
| Plane_Cap      | Provides an interface to calculate the plane capacitance based on design-specific parameters. |
| Cap_Mount      | Provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for two different capacitor orientations (Via on Side [VOS] and Via on End [VOE]). |
| X2Y_Mount      | Provides an interface to input design-specific parameters for calculating the capacitor mounting inductance for X2Y type capacitors. |
| Enlarged_Graph | Provides an enlarged view of the Z-profile shown in the System_Decap tab. |

1.2.2.1. System_Decap

You can determine the decoupling of selected FPGA devices based on the power sharing scheme entered in the System_Decap tab.

The System_Decap tab is divided into the following sections:

• Device selection  
• Power rail data and configuration  
• VRM Data  
• Rail group summary  
• VRM impedance  
• BGA Via  
• Plane  
• Spreading  
• \( F_{\text{EFFECTIVE}} \)  
• Decoupling selection  
• Result summary

1.2.2.1.1. Device Selection Section

1. Select the Family/Device using the drop-down list.
In the 20-nm Pro version of the PDN tool, choose Intel Stratix 10, Intel Arria 10, or Intel Cyclone 10 GX devices. In the 20 nm Standard version of the tool, choose Intel MAX 10 devices. In the 28 nm PDN tool, choose all other devices.

2. Select your device and the package type from the **Available Devices** drop-down list.

3. Select your desired power rail configuration from the **Power Rail Configuration** drop-down list.

   The **Power Rail Configuration** list includes custom and pre-defined configurations. When you select a pre-defined configuration, the tool sets the suggested power rail grouping automatically.

   The drop-down selections are based on examples from the pin connection guidelines for the device. Select the one that most closely matches your design, and use it as a basis for entering your design data. Refer to the pin connection guidelines for your device.

   The tool updates the list of power rails and the contents in the power rail configuration sections based on your selections.

**Figure 4. Device Selection**

![Device Selection](image1)

**Figure 5. Power Rail Configuration Selection**

![Power Rail Configuration Selection](image2)

**Related Information**

Pin Connection Guidelines

**1.2.2.1.2. Power Rail Data and Configuration Section**

This section of the application is divided into two areas. Area 1 is for the device power rail information, and Area 2 is for the power rail configuration.

1. Enter the power supply voltage in the **Voltage** column for each power rail listed in Area 1 by selecting a value from the pull-down menu, or by manually entering your own value.

   *Note:* You must enter the total dynamic current consumption of related power rails before you can use the system decoupling function.

   You can optionally adjust the recommended number up or down slightly based on knowledge of the intended application.

2. Enter the current consumption in the **Imax (Maximum Dynamic Current)** column for each power rail.
The earliest data from the Early Power Estimator (EPE) can provide good values for the current entries. The EPE delivers bulk data for the transceiver channels. Each bank of transceiver channels should be assigned the total EPE value divided by the number of banks. Later in the design cycle, the Intel Quartus Prime software power analyzer can derive much better data for each bank rail.

3. Setup your device power sharing scheme in Area 2.

**Figure 6. Power Rail Data and Power Sharing Scheme Section**

This configuration is an example of how this section of the spreadsheet should look. Every design varies depending on the device chosen and the power rail configuration selected.

The current usage for each rail should be entered in the **Imax (Maximum Dynamic Current)** column in Area 1. Note that, for the VCC rail, only the dynamic current usage should be entered from the Early Power Estimator.

Each column in Area 2 represents a power group in your system. Add or remove a power group using the **Add Group** or **Remove Group** buttons. The first row of each group is the **Regulator/Separator** type. Set the source type for the power group and available options from the pull-down list as **switcher**, **linear**, or **filter**.
The second row is the **Parent Group** type. The available options for this row are **None** and the number representing all listed power groups. Input your power sharing hierarchy in this column, and set the power rail connection using the remaining rows.

**Note:** The PDN tool 2.0 defines the power rail configuration using the **Parent/Child** power group. A power group is a child power group if it attaches to another power group at its input. The other power group is the parent group in this case. A parent group can have multiple child groups. A parent power group number is required for the child group. The parent group number of a parent power group is assigned to **None** because the group has no parent group.

The available Area 2 rail options are:
- **blank** — Device rail does not connect to the power group.
- **x** — Device rail connects to the power group.
- **x/related** — Device rail connects to the group, and its activity is related to other rails that connect to the same group. You must select **x/related** if that VCCIO/VCCPT power rail is related to other rails within the same power rail group.

**Note:** Two I/O rails are related if their output activities are synchronous. For example, when two VCCIO rails are assigned to the same memory interface. The maximum current is usually reached at the same time for these related rails. As a result, the total current of related rails equals the sum of the current of all shared rails. The total current of unrelated rails is calculated using the root-sum-square (RSS) method.

The PDN tool 2.0 sets the default power rail sharing configuration based on the selected Intel-recommended power rail configuration listed above. Make changes to better match your design.
Note: In the rail connection matrix, you can change the voltage of a rail without disconnecting it from a regulator group. However, all other rails connected to the same group must be able to change to the new voltage.

Figure 7. Changing Voltage for All Rails in a Group

### Related Information

1.2.2.1.3. Meeting Target Impedance when Entering 0 A into the PDN Tool

You may not be able to meet the target impedance if you enter 0 A into the Intel Power Distribution Network (PDN) tool.

If you enter 0 A into some low current power supply pin types, such as $V_{CCBAT}$, the PDN tool calculates a high effective impedance. Other power supply pin types may also show this problem.

The minimum allowable non-zero current entry into the Intel PDN Tool is 0.001 A. If you enter 0 A for currents below 0.001 A, a divide-by-zero or multiply-by-zero problem can occur.

To avoid this problem, enter 0.001 A to calculate decoupling for currents less than 0.001 A. Entering 0.001 A does not significantly burden the decoupling solution.
### 1.2.2.1.4. Dealing with Multiple Shared Power Supply Pin Types

You cannot add currents from multiple shared power supply pin types and enter them into a single supply pin type using the Intel Power Distribution Network (PDN) tool. The PDN tool calculates effective impedance based on the number of pins and package parasitic information for the chosen device. Entering the sum of shared currents into a single power supply pin type causes the PDN tool to miscalculate the spreading inductance. You should always enter the correct current for each power supply pin type into the PDN tool.

**Example 1**

If a shared 1.2 V power supply consists of $V_{CCIO2A}$ and $V_{CCIO2B}$, each drawing 0.3 A for a total of 0.6 A, you should not enter 0.6 A for $V_{CCIO2A}$ and 0 A for $V_{CCIO2B}$.

Instead, you should enter 0.3 A for $V_{CCIO2A}$ and 0.3 A for $V_{CCIO2B}$.

**Example 2**

If a shared 1.03 V power supply consisting of $V_{CCR\_GXBL1C}$, $V_{CCR\_GXBL1D}$, $V_{CCT\_GXBL1C}$, and $V_{CCT\_GXBL1D}$ drawing 0.5 A, 0.5 A, 0.2 A, and 0.2 A respectively, you should not enter 1 A for $V_{CCR\_GXBL1C}$ and 0.4 A for $V_{CCT\_GXBL1C}$.

Instead, you should enter $V_{CCR\_GXBL1C} = 0.5$ A, $V_{CCR\_GXBL1D} = 0.5$ A, $V_{CCT\_GXBL1C} = 0.2$ A, and $V_{CCT\_GXBL1D} = 0.2$ A.

### 1.2.2.1.5. VRM Data Section

Enter the voltage regulator module (VRM) parameters for DC supply voltage, Switcher VRM Efficiency, and Switcher VRM Input Current.

**Note:** If you are using a VRM with a sense line, the system compensates for the IR drop automatically.

### 1.2.2.1.6. Rail Group Summary Section

In this section, you can find a list of the following calculated key parameters of all power groups:

- Voltage
- Total Current
- Dynamic Current Change
- Noise Tolerance
- Core Clock Frequency
- Current Ramp Up Period
- $Z_{TARGET}$

These options allow you to customize how the data is collected or analyzed.

The **Dynamic Current Change** parameter has a pull-down menu with the following options:

- Calculate
- Override
Dynamic current change percentage requires a lot of diligence. The EPE and power analyzer both deliver values for current usage that include:

- the maximum static current (does not vary)
- the maximum current usage by the active elements

This calculation yields both a very high total current and a fairly high dynamic current usage. Calculations for a value to insert into the **Dynamic Current Change** field can yield a value much lower than the auto-populated value, which represents a safe engineering value.

The **Noise Tolerance** parameter has a pull-down menu with the following options:

- Calculate
- Override

Some PDN tool variants allow you to add data for the **Core Clock Frequency** and **Current Ramp Up Period** parameters using the pull-down menus. These values tell the tool how to calculate the current ramp up period for transient events, sometimes reducing transient current changes. The values relate to how fast the clock for the section is running, and the length of the data pipeline. Given a transient change in the input data, there are clock cycles in the pipeline for the algorithm to deliver the results. If the input data change activates a broad yet short pipeline, the transient is abrupt. This results in a large current change for the number of logic elements being used. If the pipeline is narrow and long, the overall change in current usage is proportionately smaller.

You can set the **Core Clock Frequency** parameter to a **High**, **Medium**, **Low**, or **Custom** set of input frequencies. The **Custom** option allows you to enter a specific input frequency.

The **Current Ramp Up Period** parameter allows you to specify the number of clock cycles consumed by the pipeline. You can select a **Long**, **Medium**, **Short**, or **Custom** setting.

**Core Clock Frequency** and **Current Ramp Up Period** options are highly dependent upon the core utilization setup in Intel Quartus Prime. Thus, options in the PDN tool can be used as a reference.

### 1.2.2.1.7. VRM Impedance Section

Enter the VRM impedance values for the regulators. Use the pull-down menu to enter data for **VRM Resistance** and **VRM Inductance**.
There are three ways to change the voltage regulator module (VRM) parameters.
Depending on what you select in the **VRM Impedance** pull-down menu, you can:

- **Select Custom**, and set your desired $R_{vrm}$ and $L_{vrm}$ values.
- **Select Library**, and get the suggested typical $R_{vrm}$ and $L_{vrm}$ values. This depends on the type of regulator (for example, switching, linear, or filter) you have selected.
- **Select Ignore**, and $R_{vrm}$ and $L_{vrm}$ are not considered design parameters.
- For switching regulators, you can choose a specific Intel Enpirion® VRM (based on ordering code) directly in the pull-down menu.
  - Intel Enpirion models in the VRM library already include base required output capacitance for a base/default supported current. You must obtain the base/default output capacitors from the Intel Enpirion datasheet of the device you want to include into your PCB decoupling caps, if you select an Intel Enpirion device.

**Figure 8. VRM Model**

The $R_1$ and $L_1$ effect occurs at approximately 1 kHz to 50 kHz, which represents the regulator normal $RL$ circuit without the closed loop.

The $R_2$ and $L_2$ effect occurs at 50 kHz to 300 kHz and represents the effect of the closed loop.

The $C_{out}$ branch effect occurs between 300 kHz and 1 MHz.

The PDN tool can help you select the appropriate Intel Enpirion VRM module to use for each power supply in your system.

**1.2.2.1.8. BGA Via Section**

The **BGA Via** table shows the L and R values per via. You can set the tool to **Calculate, Custom, Default**, or **Ignore**. For a fully customized workflow in which each rail group can have different settings, set the total effective R and L values in the **BGA Via** section to match your system.
If you set the **BGA Via** table to **Calculate** or **Ignore**, the **System_Decap** tab uses the same global settings for all rail groups.

If you set the **BGA Via** table to **Default**, the PDN tool calculates the R and L values similarly to the **Calculate** option, however, the tool also calculates the number of power/ground via pairs based on the rails connected to the regulator group. You can input the layer number in the tool. The layer number should match the target layer in **Full Stackup**. Then, BGA via R and L is calculated corresponding to the layer number.

**Figure 9. Setting the Layer Number**

<table>
<thead>
<tr>
<th>BGA Via</th>
<th>Default</th>
<th>Default</th>
<th>Default</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of power/Ground Via Pairs</td>
<td>40</td>
<td>4</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>Layer Number</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>R(Ω)</td>
<td>8.6066E-06</td>
<td>0.00054577</td>
<td>0.00017578</td>
<td>0.000194677</td>
</tr>
<tr>
<td>L (nH)</td>
<td>0.010544105</td>
<td>0.127997208</td>
<td>0.021317888</td>
<td>0.127997208</td>
</tr>
</tbody>
</table>

**1.2.2.1.9. Plane Section**

In the **Plane** table, you can set the tool to **Calculate**, **Custom**, or **Ignore**. For a fully customized workflow in which each rail group can have different settings:

1. Select the **Plane_Cap** tab in the PDN tool 2.0.
2. Set the parameters to match your system, and notice that the **Total planar capacitance** and **Total sheet resistance** values are updated automatically.
3. In the **System_Decap** tab, select the **Custom** option for each group where a custom plane is required.
4. Enter the calculated **Ctotal** and **Rtotal** values into the **Plane** section of the **System_Decap** tab.

Setting the **Plane** table to **Calculate** or **Ignore** causes the **System_Decap** tab to use the same global settings for all rail groups.

**1.2.2.1.10. Spreading Section**

In the **Spreading** table, you can set the tool to one of the following options:

- **Ignore**
- **Low**
- **Medium**
- **High**
- **Custom**

For a fully customized workflow in which each rail group can have different settings:

1. Select the **Library** tab in the PDN tool 2.0.
2. Set the parameters in the **Spreading R and L** table to match your system.
3. Examine the range of spreading R and L values to determine if you need a custom R and L. If a custom R and L is warranted, select **Custom** in the **System_Decap** tab and set the R and L values directly.

Setting the **Spreading** table to **Low**, **Medium**, **High**, or **Ignore** causes the **System_Decap** tab to use the same global settings for all rail groups.
1.2.2.1.11. Implementing Split Planes

Each group of power rails shares the same regulator. Therefore, separate power rail groups have separate regulators. However, they might share the same power plane layer (but separate power islands with different dimensions). Alternatively, each power rail group can be located on a different power plane layer.

1. If the regulator groups share the same power plane, select the same **Layer Number** under **BGA Via** in the **System-Decap** tab.

**Figure 10. Set the Layer Number**

2. Perform these steps in the **Stackup** tab:
   a. Complete the **Stackup Data** table.
   b. Click **Import Geometries**.

**Figure 11. Complete the Stackup Data Table**

3. Perform these steps in the **Plane_Cap** tab:
   a. Specify the dimensions of the area allocated to each regulator group.
   b. Change the import target from **All** to the group ID.
   c. Click **Import Plane R&C**.
**1.2.2.1.12. F	extsubscript{EFFECTIVE} Section**

You can set \textbf{F	extsubscript{EFFECTIVE}} to \textbf{Calculate} or \textbf{Override}. Select the \textbf{Calculate} option to use the Intel-recommended cut off frequency based on package and die parasitics.

**1.2.2.1.13. Decoupling Section**

You can set \textbf{Decoupling} to \textbf{Manual} or \textbf{Auto}. If you select the \textbf{Auto} option, any change you make to the system is automatically reflected in the decoupling solution. You can also view the impedance chart per rail group or VRM.

Selecting the \textbf{Manual} option allows you to:

- Lock in calculated decoupling solutions from being further optimized by any changes made to the \textbf{System_Decap} tab.
- Add or remove the number and type of decoupling capacitors in the \textbf{Results Summary} section. You can see its immediate impact on the impedance profile curve.

**1.2.2.1.14. Results Summary Section**

You can find the list of the number and type of capacitors used for each group, and the summary of all the capacitors used. The values in each column indicate the number of capacitors needed of each value for each rail.

The results section may show a very large number of capacitors required to decouple some power rails. Changes in various worksheets that supply data to this worksheet have a substantial effect on the capacitors required.
To use the System_Decap tab, perform the following steps:

1. Select the appropriate device family or device.
2. Set up the stack up information in the Stackup tab.
3. Select the decoupling scheme. The tool updates the power rail connection configuration to the scheme recommended in the Pin Connection Guidelines.
4. Ensure that the following default parameters match your system, and make the necessary changes such as:
   - power rail configuration
   - relativity of power rails within the same power group
   - power group layer
   - number of power/ground Via pairs
   - DC voltage supply for VRM module
   - decoupling cap location
5. Enter the projected current consumption of each power rail. If you applied the Custom setting, refer to BGA Via Section on page 16, Plane Section on page 17, or Spreading Section on page 17 to enter your values.

### 1.2.2.2. Stackup

Enter the PCB stackup information of your design in the Stackup tab. This tab updates related data in the BGA_Via, Plane_Cap, Cap_Mount and the X2Y_Mount tabs. The stackup information in this tab is also used for the System_Decap tab. Follow the instructions provided at the beginning of the tab to fill in the content for this tab.
1.2.2.2.1. Stackup Data

The **Stackup Data** section is where you enter board dimension data and other parameters, such as board stackup settings, power via, and dielectric material.

1.2.2.2.2. Full Stackup

This section lists the complete stackup of your board. You can modify content in the section to better match your board design. The last column in the section is the **PWR plane** types. In a single rail analysis case, assign the layer where the power rail is located as **target**, and the ground layer that the power rail refers to as **reference**.

Table 4. **Full Stackup Buttons**

<table>
<thead>
<tr>
<th>Button Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Construct Stackup</td>
<td>Populates the <strong>Full Stackup</strong> section to the number of layers defined in the <strong>Stackup Data</strong> section.</td>
</tr>
<tr>
<td>Import Geometries</td>
<td>Updates geometry parameters in the <strong>BGA_Via</strong>, <strong>Plane_Cap</strong>, <strong>Cap_Mount</strong>, and <strong>X2Y_Mount</strong> tabs using your input from the <strong>Stackup Data</strong> section. The tool also checks that the <strong>PWR Planes</strong> column in the <strong>Full Stackup</strong> section has only one target layer, and provides a warning for this error.</td>
</tr>
<tr>
<td>Proceed to System Decap</td>
<td>Opens the <strong>System_Decap</strong> tab.</td>
</tr>
</tbody>
</table>

1.2.2.3. BGA_Via

The **BGA_Via** tab calculates the vertical via loop inductance under the **BGA pin** field.
Figure 15.  BGA_Via Tab

The values in the **Unit** column indicate a unit value per one pair.

<table>
<thead>
<tr>
<th>BGA Via Inductance</th>
<th>Symbol</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via drill outer diameter</td>
<td>OD</td>
<td>mils</td>
<td>10</td>
</tr>
<tr>
<td>Via drill inner diameter</td>
<td>ID</td>
<td>mils</td>
<td>8</td>
</tr>
<tr>
<td>Via pitch</td>
<td>B</td>
<td>mils</td>
<td>30</td>
</tr>
<tr>
<td>Via length</td>
<td>C</td>
<td>mils</td>
<td>10</td>
</tr>
<tr>
<td>Linear inductance</td>
<td>Llin</td>
<td>nH</td>
<td>0.0209</td>
</tr>
<tr>
<td>Via inductance</td>
<td>Lvia</td>
<td>nH</td>
<td>0.2982</td>
</tr>
<tr>
<td>Via resistance</td>
<td>Rvia</td>
<td>mΩ</td>
<td>10.6848</td>
</tr>
</tbody>
</table>

Enter the layout-specific information such as via drill diameters, via length, via pitch, and the number of power/ground via pairs under the BGA in the **BGA Via Inductance** table. The tool calculates the effective via loop inductance and resistance value. You can save the change made to the tab, restore the changes, or restore the tab back to the default settings.

**1.2.2.4. Plane_Cap**

The **Plane Cap** tab calculates the distributed plane capacitance in microfarads (µF) that is developed between the power/ground planes based on the parallel plate capacitor equation.
Enter the design specific information such as plane dimensions, plane configuration and the dielectric material used in the Planar Capacitance table. The tool calculates a plane capacitance value. You can save custom values, restore custom values, or restore the default settings.

The Import Plane R&C button inserts the data for the planar capacitance into the regulator group data.

1.2.2.5. Cap_Mount

The Cap Mount tab calculates the capacitor mounting inductance seen by the decoupling capacitor.

Note: Power rails on different layers have different mounting inductances. For the best results, run the PDN separately for each layer set.
The capacitor mounting calculation is based on the assumption that the decoupling capacitor is a two-terminal device. The capacitor mounting calculation is applicable to any two-terminal capacitor with the following footprints: 0201, 0402, 0603, 0805, and 1206. Enter all the information relevant to your layout, and the tool provides a mounting inductance for a capacitor mounted on either the top or bottom layer of the board. Depending on the layout, you can choose between VOE (Via on End) or VOS (Via on Side) to achieve an accurate capacitor mounting inductance value. Generally, VOS can have lower mounting inductance due to a smaller via pitch. Also, X2Y cap can be considered as a solution for a space-limited design.

If you plan to use a footprint capacitor other than a regular two-terminal capacitor or X2Y capacitor for decoupling, you can skip the Cap Mount tab. In this case, you can directly enter the capacitor parasitics and capacitor mounting inductance in the Library tab (under the Custom field in the Decoupling Cap section of the library). As with the other tabs, you can save the changes made to the tab, restore the changes, or restore the tab back to the default settings.

You must pay special attention to the via lengths for the capacitors. Via inductance comprises a substantial portion of the PDN impedance.

1.2.2.6. X2Y_Mount

The X2Y Mount tab calculates the capacitor mounting inductance seen by the X2Y decoupling capacitor.
Figure 18. **X2Y_Mount Tab**

Enter all the information relevant to your layout in the **X2Y CAP Mounting Inductance** table. The tool then provides a mounting inductance for an X2Y capacitor mounted on either the top or bottom layer of the board. You can save the changes made to the tab, restore the changes, or restore the tab back to the default settings.

### 1.2.2.7. Library

The **Library** tab stores all the device parameters that are referred to in the other tabs.
You can change each of the default values listed in the respective sections to meet the specific needs of your design.

1.2.2.7.1. Two-Terminal Decoupling Capacitors

The decoupling capacitors section contains the default ESR and ESL values for the various two-terminal capacitors in the following footprints:

- 0201
- 0402
- 0603
- 0805
- 1206

You also have the option to either modify the default values or enter your own commonly used custom values in the **Custom** field. If you are using a capacitor with a footprint that is not available in the tool, you must use the **Custom** field to enter the capacitor parasitics and the corresponding mounting inductance.
The decoupling capacitors section also provides the option for user-defined capacitors (such as User1 through User4). You can define the ESR and ESL parasitics for the various footprints and enter the corresponding capacitor value in the System_Decap tab. Choose the corresponding footprint when defining the capacitor values.

1.2.2.7.2. Bulk Capacitors

The bulk capacitors section contains the commonly used capacitor values for decoupling the power supply at mid and low frequencies. You can change the default values to reflect the parameters specific to the design.

1.2.2.7.3. X2Y Decoupling Capacitors

The X2Y decoupling capacitors section contains the default ESR and ESL values for the various X2Y capacitors in the 0603, 0805, 1206, and 1210 footprints. You also can replace the default ESR and ESL values with your own commonly used custom values.

1.2.2.7.4. BGA Via and Plane Capacitance

This section allows you to directly enter the values for effective via loop inductance under the BGA and plane capacitance during the pre-layout phase when no design-specific information is available.

If you have access to design-specific information, you can ignore this section and enter the design-specific information in the Plane Cap and BGA Via tabs that calculate the plane capacitance and the BGA via parasitics, respectively.

1.2.2.7.5. VRM Library

The VRM section lists the default values for both the linear and switcher regulators. In the Custom field, you can change the VRM parasitics listed under the linear/switcher rows or add the custom parasitics for the VRM relevant to the design.

1.2.2.7.6. Spreading R and L Parasitics

This library provides various options for the default effective spreading inductance values that the decoupling capacitors see with respect to the FPGA. These values are based on the quality of the PDN design. You can choose a Low value of effective spreading inductance if you have optimally designed your PDN Network. Optimum PDN design involves implementing the following design rules:

- PCB stackup that provides a wide solid power/ground sandwich for a given supply with a thin dielectric between the planes. The thickness of the dielectric material between the power/ground pair directly influences the amount of spreading/loop inductance that a decoupling cap can see with respect to the FPGA.
- Placing the capacitors closer to the FPGA from an electrical standpoint.
- Minimizing via perforations in the power/ground sandwich in the current path from the decoupling caps to the FPGA device.

Due to layout and design constraints, the PDN design may not be optimal. In this case, you can choose either a Medium or High value of spreading R and L. You can also change the default values or use the Custom field listed in the library specific to the design.
1.2.2.7.7. Dielectric Material Library

This library lists the dielectric constant values for the various commonly used dielectric materials. These values are used in the plane capacitance calculations listed under the Plane_Cap tab. You can change the values listed in this section.

If you change the default values listed in the various sections in the Library tab, you can save the changes by clicking Save Custom. You can restore the default library by clicking Restore Default located at the top right-hand corner of the Library page. You can also restore the saved custom library by clicking Restore Custom.

1.2.2.7.8. User Set F_EFFECTIVE

You must decouple to an F_EFFECTIVE higher than what is calculated for the power rails of some device families. In this case, you must set the F_EFFECTIVE option to Override in the System_Decap tab. The PDN tool 2.0 then uses the F_EFFECTIVE value entered here.

1.2.2.8. Enlarged_Graph

In the Enlarged_Graph tab, you can view the enlarged Z-profile plot. The PDN tool 2.0 switches to this tab when you click the Z-profile plot in the System_Decap tab. You can go back to the System_Decap tab when you click the Return button.

Figure 20. Enlarged_Graph Tab
1.2.3. Design PCB Decoupling Using the PDN Tool 2.0

PCB decoupling keeps the PDN $Z_{	ext{EFF}}$ smaller than $Z_{\text{TARGET}}$ with the properly chosen PCB capacitor combination up to the frequency where the capacitance on the package and die take over the PDN decoupling. This procedure uses the PDN tool 2.0 in different power rail configurations and provides design examples using the Intel Stratix 10 device PDN tool.

1.2.3.1. Pre-Layout Instructions

The PDN tool 2.0 provides an accurate estimate of the number and types of capacitors needed to design a robust power delivery network, regardless of where you are in the design phase. However, the accuracy of the results depends highly on your inputs for the various parameters.

If you have finalized the board stack-up and have access to board database and layout information, you can proceed through the tabs and enter the required information to arrive at an accurate decoupling scheme.

In the pre-layout phase of the design cycle when you do not have specific information about the board stack-up and board layout, you can follow these instructions to explore the solution space when finalizing key design parameters such as stackup, plane size, capacitor count, capacitor orientation, and so on.

In the pre-layout phase, ignore the Plane Cap and Cap Mount tabs and go directly to the Library tab when you do not have the layout information. If available, enter the values shown below in the Library tab. To use the default values, go directly to the System_Decap tab to begin the analysis.
1. Enter the ESR, ESL, and Lmnt values for the capacitors listed in the Custom field.
2. Enter the effective BGA via parasitics for the power supply being decoupled in the BGA Via & Plane Cap field.
3. Enter the plane capacitance seen by the power/ground plane pair on the board for the power supply in the BGA Via & Plane Cap field.
4. Enter the VRM parasitics, if available, in the Custom row of the VRM field.
5. Enter the effective spreading inductance seen by the decoupling capacitors in the Custom row of the Spreading R and L field.

1.2.3.2. Deriving Decoupling in a Single-Rail Scenario

A power supply connects to only one power rail on the FPGA device in a single-rail scenario. The PDN noise is created by the dynamic current change of the single rail. You determine $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$ based on the parameters related to the selected rail only.
The PDN tool 2.0 provides two ways to derive a decoupling network. You can set up the tool with the information needed and let the tool derive the PDN decoupling for your system. You can also manually enter the information and derive decoupling. To derive the desired capacitor combination:

1. Select the device/power rail to work with.
2. Select the parameter settings for the PDN components.
3. Enter the electric parameters to set $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$. You need to have a good estimate of the parameters entered to derive the proper decoupling guidelines ($Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$). Although you need to determine those guidelines based on the worst-case scenario, pessimistic settings result in hard-to-achieve guidelines and over design of your PCB decoupling.
4. Derive the PCB decoupling scheme.

You must adjust the number and value of the PCB capacitors in the Decoupling Capacitor (Mid/High Frequency) and Decoupling Capacitor (Bulk) fields to keep the plotted $Z_{\text{EFF}}$ below $Z_{\text{TARGET}}$ until $F_{\text{EFFECTIVE}}$. You can derive the decoupling for the selected power rail manually. You can also select the Auto Decouple button and let the PDN tool 2.0 automatically determine a decoupling solution. If you are not able to find a capacitor combination that meets your design goal, you can try to change the parameters at 2 on page 31. For example, you can reduce the BGA via inductance used in the Calculate option by reducing the BGA via length in the BGA_VIA tab and using the low option for plane spreading. These changes reduce parasitic inductance and make it easier to achieve your decoupling goal. To achieve the low spreading setting, you must place the mid to high frequency PCB capacitors close to the FPGA device. You also must minimize the dielectric thickness between the power and ground plane. Refer to Troubleshooting if the $Z_{\text{EFF}}$ is too high or the number of capacitors for decoupling becomes too high.

If you are not able to meet the $Z_{\text{TARGET}}$ requirement with the changes above, the PDN in your design may have reached its physical limitation under the electrical parameters you entered for $Z_{\text{TARGET}}$ and $F_{\text{EFFECTIVE}}$. You should re-examine these parameters to check if they are overly pessimistic.
Figure 22. **Enlarged Plot of Z\textsubscript{EFF}**

This sample impedance plot is for a 1SG280LU_F50 VCC power rail. Assume that the minimum voltage supply is 0.8 V, \(I_{\text{dynamic}}\) is 50 A, dynamic current change is 30\% of \(I_{\text{dynamic}}\), and the maximum allowable die noise tolerance is 5\% of supply voltage. The VCC rail has 169 power BGA vias. The length of BGA via is assumed to be 20 mil.

![Impedance Frequency Plot](image)

The PDN tool 2.0 calculated that \(Z_{\text{TARGET}}\) is 0.0027 \(\Omega\) and \(F_{\text{EFFECTIVE}}\) is 13.58 MHz. The figure above shows one of the capacitor combinations that you can select to meet the design goal. As shown in the plot, \(Z_{\text{EFF}}\) remains under \(Z_{\text{TARGET}}\) up to \(F_{\text{EFFECTIVE}}\). There are many combinations, but the ideal solution is to minimize the quantity and the type of capacitors needed to achieve a flat impedance profile below \(Z_{\text{TARGET}}\).

**Related Information**

Troubleshooting ZEFF on page 33

1.2.3.3. Deriving Decoupling in the Power-Sharing Scenarios

It is a common practice that several power rails in the FPGA device share the same power supply. For example, you can connect VCCPT, VCCA_PLL, and VCCA_FPLL rails that require the same supply voltage to the same PCB power plane. This can be required by the design, such as in the memory interface case. This can also come from the need to reduce bill of materials (BOM) cost. You can use the **System_Decap** tab to facilitate the decoupling design for the power sharing scenarios.

When deriving decoupling capacitors for multiple FPGAs sharing the same power plane, each FPGA should be analyzed separately using the PDN tool 2.0. For each FPGA design, combine the required power rails as described above and analyze the decoupling scheme as if the FPGA was the only device on the power rail, taking note of how the current is divided across the devices.

High frequency decoupling capacitors are meant to provide the current needed for AC transitions, and must be placed in a close proximity to the FPGA power pins. Thus, the PDN tool 2.0 should be used to derive the required decoupling capacitors for the unique power requirements for each FPGA on the board.
The power regulators must be able to supply the total combined current requirements for each load on the supply, but the decoupling capacitor selections should be analyzed on a single FPGA basis.

1.2.4. Troubleshooting $Z_{\text{EFF}}$

When the decoupling mode is set to Auto, this may result in a $Z_{\text{EFF}}$ value that is too high. This can happen when the PCB parameters you entered result in an inefficient PDN, and the current to be decoupled by the PCB are unrealistically high.

With difficult PCB and current parameters, auto decoupling continues to add decoupling capacitors until it determines they have little effect. This results in hundreds of capacitors. You can achieve decoupling schemes with similar performance manually using far fewer capacitors.

1.2.4.1. Strategies for Correcting a High $Z_{\text{EFF}}$

As well as decoupling manually, you can reduce the decoupling burden by accurately estimating your current requirements and making your PCB more efficient. You may be able to achieve reduced PCB current requirements in the following ways:

- Estimating realistic current requirements in the Early Power Estimator (EPE).
- Entering realistic toggle rate figures for the logic in the EPE. Unrealistically high toggle rates dramatically increases dynamic current requirements.
- Entering realistic logic requirements in the EPE.
- Entering realistic clock frequencies in the EPE.
- Using the Intel Quartus Prime software power analyzer and .vcd simulation entry for accurate current requirement estimation.
- Considering Root Sum Squared (RSS) averaging for shared power supply rails. Refer to the Introduction tab of the PDN tool for more information about this method.

You can make the PCB more efficient in the following ways:

- Increasing inter-plane capacitance of your Power (PWR) and Ground (GND) plane pair by reducing their dielectric thickness.
- Increasing inter-plane capacitance of your PWR and GND plane pair by increasing their surface area.
- Reducing loop inductance from the PWR and GND plane pair to the FPGA. You can do this by moving them closer to the surface of the PCB where the FPGA is mounted.
- Reducing loop inductance from the high frequency decoupling capacitors to the PWR and GND plane pair. You can do this by placing them on the surface of the PCB that is closest to the planes.
- Using Via On Side (VOS) instead of Via On End (VOE) capacitor mounting topologies to help at high frequencies.
- Using ultra-low Effective Series Inductance (ESL) mounting capacitors to help at high frequencies, for example, X2Y package style.
- Using ultra-low Effective Series Resistance (ESR) bulk capacitors to help at low frequencies.
- Considering larger vias with less ESL.
Realistic tool entry can make decoupling easier to achieve. The following factors affect the calculation of $Z_{\text{TARGET}}$:

- An increase in dynamic current reduces $Z_{\text{TARGET}}$ and makes decoupling difficult to achieve. See the guidelines above.
- Enter realistic noise or ripple figures into the PDN tool. Use the noise figure listed in the device and rail specific table in the Introduction tab of the PDN Tool. Unrealistic ripple requirements reduce $Z_{\text{TARGET}}$ and make decoupling difficult.
- Enter realistic transient % figures into the PDN tool. Use the transient % figure listed in the device and rail specific table in the Introduction tab of the PDN Tool. Unrealistic transient % requirements reduce $Z_{\text{TARGET}}$ and make decoupling difficult.

The PDN Tool 2.0 includes the following new pessimism removal features to make decoupling the large core current manageable:

- Core clock frequency
- Current ramp up period

*Note:* These features are available only for the core rail.

### 1.3. PDN Tool Setup and Result Optimization

*Note:* If your PDN tool does not update automatically, ensure that you set the Microsoft Excel® Calculation option as follows: Formulas ➤ Calculation Options ➤ Automatic.

#### 1.3.1. Setting Up a PCB Stackup

This step-by-step guide helps you get optimal PDN decoupling estimation using Intel's PDN tool. This example is common for all product families supported by the PDN tool.

##### 1.3.1.1. Selecting Your Device

1. Click the System_Decap tab.
2. Select your Device and click Yes in the confirmation dialog box.

##### 1.3.1.2. Inputting Stackup Data

1. Click the Stackup tab.
2. Input your stackup values for the following parameters:
   - Number of Layers
   - Drill Size
   - BGA Via pitch
   - Foil Thickness
3. Select a dielectric material from the Dielectric Material drop-down menu.

*Note:* If you are using a custom dielectric material, skip this step and proceed to the Using a Custom Dielectric Material section.
4. Click **Construct Stackup**, then click **Yes** in the **Construct Stackup** confirmation dialog box. The **Full Stackup** section updates based on your inputs.

5. Enter the **Thickness** values for each layer in the **Full Stackup** table, then click **Import Geometries**.

**Figure 23. Full Stackup Table**

![Full Stackup Table]

6. Save your data to prevent data loss.

**Related Information**

Using a Custom Dielectric Material on page 35

**1.3.1.2.1. Using a Custom Dielectric Material**

1. Click the **Library** tab, then enter the **Er** value for **Custom 1** or **Custom 2** as necessary.
2. Click the **Stackup** tab, then select either **Custom 1** or **Custom 2** from the drop-down menu.

3. Click **Construct Stackup**, then click **Yes** in the confirmation dialog box.

### 1.3.2. Setting up a Power Group

#### 1.3.2.1. Selecting the Rails

1. Click the **System_Decap** tab.

2. Select a regulator type from the **Regulator/Separator** drop-down menu for **Group #1**.

3. Select either **x** or **x/related** for each selected power rail.

   *Note:* One power group can have one or more power rails depending on your power configuration. Refer to the **Introduction** tab in the PDN tool for a complete description of the tool options.

4. Obtain the dynamic current estimations from the **Report** tab of the Early Power Estimator (EPE) tool.

5. Enter these values in the **Imax (Maximum Dynamic Current)** column of the **System_Decap** tab in the PDN tool.

   *Note:* You can always add your own additional engineering margin on top of the EPE estimation based on your system design experience and the Power Model Accuracy in the EPE tool.

### Related Information

**Early Power Estimator (EPE)**
1.3.2.2. Rail Group Summary

The PDN tool automatically calculates the target impedance \( Z_{\text{TARGET}} \) based on the recommended Dynamic Current Change\% and Noise Tolerance\%.

**Figure 25. Rail Group Summary**

Boxes shaded in light blue are drop-down menus with different options to select. Core Clock Frequency and Current Ramp Up Period options vary depending on your design.

With these options enabled, the \( Z_{\text{TARGET}} \) curve relaxes from certain frequencies based on the inputs.

**Figure 26. Flat versus Curved \( Z_{\text{TARGET}} \)**

1.3.2.3. VRM Impedance

The PDN tool has default Library R and L models for **VRM Impedance**.

If a VRM model is available from the vendor, you can select the **Custom** option to replace the default values by directly overriding the new values.
Figure 27. **VRM Impedance**

![VRM Impedance](image)

**Note:** The single R and L assumption in the tool is for 1-phase single VRM. For multi-phase VRM usage, the simplest method for rough estimation is to divide the default numbers by the number of phases. For example, if the default values for a single switcher and four-phase VRM are $R = 1 \, \text{mΩ}$ and $L = 20 \, \text{nH}$, then you can estimate the final values as $R = 0.25 \, \text{mΩ}$ and $L = 5 \, \text{nH}$. Make note of how many phases of VRM you use in each PDN design. The tool may recommend bulk cap solutions that are significantly different.

### 1.3.2.4. BGA Via

Once you select a power rail, the PDN tool automatically updates the number of Power/GND Via pairs. Every device has a different number.

The tool automatically calculates the parasitics when you enter your expected layer number in the **Layer Number** field by overriding for power rail location in the stackup.

Figure 28. **BGA Via**

The **Layer Number** field also has the Ignore, Custom, and Calculate options.

![BGA Via](image)

**Note:** You can use the BGA_Via tab as a stand-alone tool for custom via parasitic calculation.

### 1.3.2.5. Calculating Plane

Based on your layer location assumption, the tool automatically calculates the plane R and C.

1. Click the **Stackup** tab.
2. Enter your expected plane length and width values in the **Plane Length** and **Plane Width** fields, respectively.

This is the best method for estimating if the layout design is already in progress (see the following figure).
3. Select which layers you want to use as target (power) and reference (ground, two layers maximum) in the **Full Stackup** table.

4. Click **Import Geometries** on the left side of the **Full Stackup** table.

5. Click the **Plane_Cap** tab.
   The tool automatically updates the plane parasitics.

6. Change the regulator group number in the **Import the calculated Plane R & Plane C to regulator Group** field, then click **Import Plane R&C**.

7. Click the System_Decap tab and verify that the tool has updated the parasitic.

   **Note:** The PDN tool does not support the multi-layered design for a single power. However, you can repeat 1 on page 38 through 6 on page 39 for each power layer, keeping the estimated parasitic numbers of each and combining capacitances of each power for final capacitance and calculating resistances of each power in parallel to get the final resistance. For example, if both layers nine and 10 of roughly the same size plane have one power rail, the tool calculates the parasitics based on one power and one reference layer in the **Full Stackup** table as shown in the figure below. Then, the final capacitance can be $0.0016 \times 2 = 0.0032 \, \mu F$ and the final resistance can be $0.001 \, / \, 2 = 0.0005 \, \Omega$. 
1.3.2.6. Plane Spreading Parasitics

For plane spreading parasitics, you can use pre-defined Library values, Custom, or Ignore options.

The default spreading setting is Low. Depending on the location of your decaps, you may also select Medium or High.

1.3.2.7. $F_{\text{EFFECTIVE}}$ and Decoupling Result Summary

The following figure shows final decoupling recommendations based on the inputs in the tool. However, even though $Z_{\text{PDN}}$ meets the $Z_{\text{TARGET}}$ up to $F_{\text{EFFECTIVE}}$, the number of capacitors, 301, are not suitable for the real design. Refer to the Optimization Method section for details about optimizing your results.
1.3.3. Optimizing in Pre-Layout

1.3.3.1. Checking the Capacitor Model

Capacitors, especially bulk caps, can be replaced with capacitors with lower parasitics.

1. Click the **Library** tab.

2. If there are RLC models with lower parasitics, replace the existing capacitors with them.
   a. Replace bulky Tantal Polymer capacitors with Multi-layered Ceramic Capacitor (MLCC) caps with similar electrical/thermal characteristics. 100uF, 220uF, and 330uF caps with much lower ESR and ESL are available.

   Using the decap library effectively in the PDN tool results in a more accurate estimation.
   b. Use **User** and **Custom** options for additional capacitors.
1.3.3.2. Optimizing the Decap Count

Since the tool is a code-based spreadsheet, it keeps adding up the number of decoupling capacitors until $Z_{PDN}$ satisfies $Z_{TARGET}$ up to $F_{EFFECTIVE}$. The PDN tool has a 301ea maximum decap count.


There can be a ±5% variation on $Z_{EFF}$ impedance when doing decoupling caps optimization. This impedance variation can relate to fabrication tolerance.
2. Observing the impedance plot carefully, optimize the number of each capacitor.
Figure 36. Manual Decoupling Results Summary - Post-Optimization, Round 1

After optimizing manually, 301ea decaps are dramatically reduced to 124ea while maintaining a similar $Z_{PDN}$ profile (the red curve) under the same $Z_{TARGET}$. 
Figure 37. **Manual Decoupling Results Summary - Post-Optimization Results, Round 1**

A small amount of violation at different frequencies can reduce the number of decaps. Before and after results are shown below.

1.3.4. Further Optimizing for Better Accuracy

While the two methods described in *Optimizing in Pre-Layout* are mainly used in the pre-layout stage for a rough estimation of the decoupling solution, the method described here shows how to get a more accurate and optimized estimation.

While *Checking the Capacitor Model* updates the decoupling capacitor library with the actual models used and *Optimizing the Decap Count* controls the number of decaps in manual mode, this method shows how to exclude Spreading R and L from the estimation process. As shown in the figure below, there is no mechanical restriction in populating decaps on the other side of the FPGA and red boxes indicate 70ea of 0402in decaps which can be directly placed; the majority of the total 124ea decaps can be populated right under BGAs. Thus, the spreading option might be negligible in this case.
1. Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide

**Figure 38.** Populating Decaps on the Other Side of the FPGA

1. Change Feffective option from Calculate to Override.
2. Check whether or not the number remains the same.
3. If the number changes, write the recommended $F_{\text{EFFECTIVE}}$, 10.18 MHz in the example below, into the white blank.

**Figure 39.** $F_{\text{EFFECTIVE}}$ Override

<table>
<thead>
<tr>
<th>Feffective</th>
<th>MHz</th>
<th>Calculate</th>
<th>10.18</th>
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<tr>
<td>Feffective</td>
<td>MHz</td>
<td>Override</td>
<td>10.18</td>
</tr>
</tbody>
</table>

4. Change the Spreading option from Low to Ignore. Once the spreading option is ignored, the entire $Z_{\text{PDN}}$ is lowered a little, which means more margin.
5. Repeat the manual optimization for each cap as shown in Optimizing the Decap Count.
After the optimization process, only 48ea of 0402in capacitors (circled with a red box below) are estimated while the total allowable number of 0402in capacitors is 70ea. Also, the rest of the larger capacitors (circled with a blue box below) in this example can be populated in the BGA area. Final results are shown below. The total number of capacitors was decreased down to 77ea from the max limit of 301ea, including bulk capacitors, through round 1 and 2 of the optimization process.

**Note:** The PDN tool result already includes the bulk capacitor solution for VRM. However, Intel recommends checking with the VRM vendor about the required output capacitance to check if the PDN tool estimation can cover the requirement. Intel Enpirion models in the VRM library already include the required output capacitance. For the required capacitor combination, please refer to the datasheet of each VRM model.
1.3.5. Correlation

The following results show the correlation between the PDN tool and the post-layout system PDN impedance profile (lower right figure) for one of Intel’s development kit boards. In the post-layout analysis, the simple VRM model from the PDN tool was used. Since the PDN tool is already considering PKG and die parasitics, both results are well correlated.
**Note:** The PDN tool does not display the on-die capacitance in the result graph. Die capacitance is utilized for determining $F_{\text{EFFECTIVE}}$.

**Figure 42.** PDN Tool

### 1.4. Device-Specific PDN Tool 2.0 Known Issues and Their Solutions

#### Table 5. Device-Specific PDN Tool 2.0 Known Issues and Their Solutions

<table>
<thead>
<tr>
<th>Known Issue</th>
<th>Solution</th>
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</thead>
<tbody>
<tr>
<td>Why does the PDN tool suggest 0 bulk decoupling capacitors with low-current power supply rails?</td>
<td>Low-Current Power Supply Rail Knowledge Base Article</td>
</tr>
<tr>
<td>Should I enter $I_{\text{MAX}}$ or $I_{\text{DYNAMIC}}$ currents into the PDN tool?</td>
<td>Decoupling Current Knowledge Base Article</td>
</tr>
<tr>
<td>Why can I not meet the target impedance when entering 0 mA into the PDN tool?</td>
<td>Impedance with 0 mA Knowledge Base Article</td>
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</tr>
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<td>Can I sum currents from multiple shared power supply pin types and enter</td>
<td>Summing Power Supply Pin Types Knowledge Base Article</td>
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<tr>
<td>them into a single supply pin type using the PDN tool?</td>
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<tr>
<td>Can I connect multiple power or GND pins to their planes through a</td>
<td>Using a Single Via Knowledge Base Article</td>
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<td>single via with Intel devices?</td>
<td></td>
</tr>
<tr>
<td>Why might the PDN tool's Auto Decoupling mode result in a Z_{eff} that</td>
<td>Auto Decoupling Mode Knowledge Base Article</td>
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<td>is too high?</td>
<td></td>
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<tr>
<td>How do I use the PDN tool to optimize my PDN design?</td>
<td>AN 750: Using the PDN Tool to Optimize Your Power Delivery Network Design</td>
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**1.5. Document Revision History for the Device-Specific Power Delivery Network (PDN) Tool 2.0 User Guide**

<table>
<thead>
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<td>2021.08.24</td>
<td>Made the following change:</td>
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<td>• Modified the units used in the Meeting Target Impedance when Entering 0 A into the PDN Tool topic.</td>
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<tr>
<td>2020.10.06</td>
<td>Made the following changes:</td>
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<td>• Added Meeting Target Impedance when Entering 0 mA into the PDN Tool and Dealing with Multiple Shared Power Supply Pin Types topics.</td>
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<td>• Added note to PDN Tool Setup and Result Optimization topic.</td>
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<td>2020.08.11</td>
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<td></td>
<td>• Added supported Intel Stratix 10 FPGA devices.</td>
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<td>• Added VCCRT_GXE, VCCRT_GXP, VCCH_GXE, and VCCH_GXP to &quot;Settings for the Intel Stratix 10 Device Power Rails&quot; table.</td>
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<tr>
<td></td>
<td>• Added a reason for the Z_{eff} impedance ±5% variation.</td>
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<td>• Added Device-Specific PDN Tool 2.0 Known Issues and Their Solutions.</td>
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<td>Made the following change:</td>
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<td>• Added the &quot;VRM Model&quot; figure.</td>
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<td>2018.10.04</td>
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<td>• Changed the name of the GUI tab to \textit{Imax (Maximum Dynamic Current)} in the &quot;Power Rail Data and Configuration Section&quot; section.</td>
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<td></td>
<td>• Updated the &quot;Changing Voltage for All Rails in a Group&quot; figure.</td>
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<td>• Updated the &quot;Power Rail Data and Power Sharing Scheme Section&quot; figure.</td>
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<td></td>
<td>• Added further description for VRM in the &quot;VRM Impedance Section&quot; section.</td>
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<td>• Changed the name of the GUI tab to \textit{Imax (Maximum Dynamic Current)} in the &quot;Selecting the Rails&quot; section.</td>
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<td>2017.11.27</td>
<td>• Added Setting Up a PCB Stackup</td>
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<td>• Added Setting Up a Power Group</td>
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<td>• Added Optimizing in Pre-layout</td>
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<td>• Added Correlation</td>
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<td></td>
<td>• Merged the PCG links</td>
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<td>• Changed the operating systems and platforms in the &quot;PDN Tool 2.0 Software Verification&quot; table.</td>
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<td>• Added the Intel Cyclone 10 GX device to the list of supported devices in the &quot;Overview&quot; section.</td>
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<td>• Added links to the <em>Cyclone 10 GX Device Family Pin Connection Guidelines</em> in the &quot;ZTARGET&quot; section.</td>
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<td>• Added links to the <em>Cyclone 10 GX Device Family Pin Connection Guidelines</em> in the &quot;Device Selection Section&quot; section.</td>
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<td>• Removed a step from the &quot;BGA Via Section&quot; section.</td>
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<td>2016.12.09</td>
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<td>• Added Stratix 10 device information globally.</td>
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<td>• Changed &quot;Die Noise Tolerance&quot; to &quot;Noise Tolerance&quot; globally.</td>
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<td>• Changed the &quot;Settings for the Stratix 10 Device Power Rails&quot; table to display the Stratix 10 specifications.</td>
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<td>• Changed the &quot;Device Selection&quot; figure to show Stratix 10 selections.</td>
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<td>• Changed the &quot;Power Rail Configuration Scheme&quot; figure to show Stratix 10 configurations.</td>
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<td>• Added a cross-reference to the <em>Stratix 10 GX and SX Device Family Pin Connection Guidelines</em> to the &quot;Device Selection Section&quot; topic.</td>
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<td>• Changed &quot;Imax&quot; to &quot;Idynamic&quot; in the &quot;Power Rail Data and Configuration Section&quot; topic.</td>
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<td>• Changed the &quot;Power Rail Data and Power Sharing Scheme Section&quot; figure to show Stratix 10 configurations.</td>
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<td>• Changed &quot;root-mean-square&quot; to &quot;root-sum-square&quot; in the &quot;Power Rail Data and Configuration Section&quot; topic.</td>
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<td>• Changed the &quot;Changing Voltage for All Rails in a Group&quot; figure to show Stratix 10 voltages.</td>
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<td>• Changed the note in the &quot;VRM Data Section&quot; topic.</td>
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<td>• Updated the options for the Current Ramp Up Period in the &quot;Rail Group Summary Section&quot; topic.</td>
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<td>• Changed the &quot;Stackup Tab&quot; figure to show Stratix 10 stackup information.</td>
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<td>• Removed the &quot;Stackup Stub&quot; section.</td>
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<td>• Changed the description of the &quot;Enlarged Plot of $Z_{EFF}$&quot; figure.</td>
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<td>• Changed the PDN Tool 2.0 calculations in the &quot;Deriving Decoupling in a Single-Rail Scenario&quot; section.</td>
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<td>• Removed the following pessimism removal features from the &quot;Strategies for Correcting a High $Z_{EFF}$&quot; section:</td>
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<td>□ Dynamic current change</td>
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<td></td>
<td>□ Die noise tolerance</td>
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<td>• Added definition of $Z_{EFF}$ to the &quot;$F_{EFFECTIVE}$&quot; section.</td>
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<td>• Added the Ignore option in the &quot;VRM Impedance Section&quot; section.</td>
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<td>2016.10.31</td>
<td>Clarified the Family/Device, Available Devices, and Power Rail Configuration entry description.</td>
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<td>• Documented a new option to change a rail's voltage without disconnecting it from the regulator group.</td>
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<td>• Clarified the PDN tool's treatment of VRMs with sense lines.</td>
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<td>• Documented the Default option in the BGA Via table.</td>
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<td>• Described how to implement split planes.</td>
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<td>2016.06.15</td>
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<td>• Changed the description of how $F_{EFFECTIVE}$ is calculated in the &quot;$F_{EFFECTIVE}$&quot; section.</td>
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<td>2015.11.02</td>
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<td>• Changed the description in the &quot;Overview&quot; section.</td>
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<td>• Added a description for current usage of Imax in the &quot;Power Rail Data and Configuration Section&quot; section.</td>
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<td>• Changed the &quot;Results Summary Section of the System_Decap Tab&quot; figure.</td>
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<td>• Added description for the Import Plane R&amp;C button in the &quot;Plane_Cap&quot; section.</td>
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<td>• Added list of pessimism removal features in the &quot;Strategies for Correcting a High Z_{EFF}&quot; section.</td>
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<td>• Changed the voltage for VCCH_GXB in the &quot;Settings for the Intel Arria 10 Device Power Rails&quot; table.</td>
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<td>2015.03.06</td>
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<td>• Added MAX 10 to the list of supported devices in the Overview section.</td>
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<td>• Added new parameters and descriptions to the Rail Group Summary Section section.</td>
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<td>• Added a note to the Cap_Mount section.</td>
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<td>• Added the Troubleshooting Z_{EFF} and Strategies for Correcting High Z_{EFF} sections.</td>
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<td>2014.09.29</td>
<td>• Added notes to the &quot;PDN Topology Modeled as Part of the Tool&quot; figure.</td>
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<td>• Added detailed explanation of the options available in the VRM Impedance pull-down menu in the &quot;VRM Impedance Section.&quot;</td>
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<td>2014.09.12</td>
<td>Initial release.</td>
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