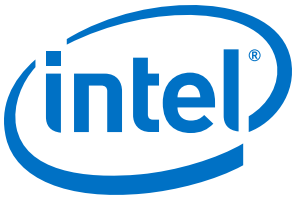

Intel® FPGA Temperature Sensor IP Core User Guide

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Contents

Intel® FPGA Temperature Sensor IP Core User Guide

The Intel® FPGA Temperature Sensor IP core configures the temperature sensing diode (TSD) block to utilize the temperature measurement feature in the FPGA.

Related Information

Introduction to Intel FPGA IP Cores
Provides general information about Intel FPGA IP cores.

Intel FPGA Temperature Sensor Features

The following table lists the Intel FPGA Temperature Sensor IP core features.

Table 1. Intel FPGA Temperature Sensor Features

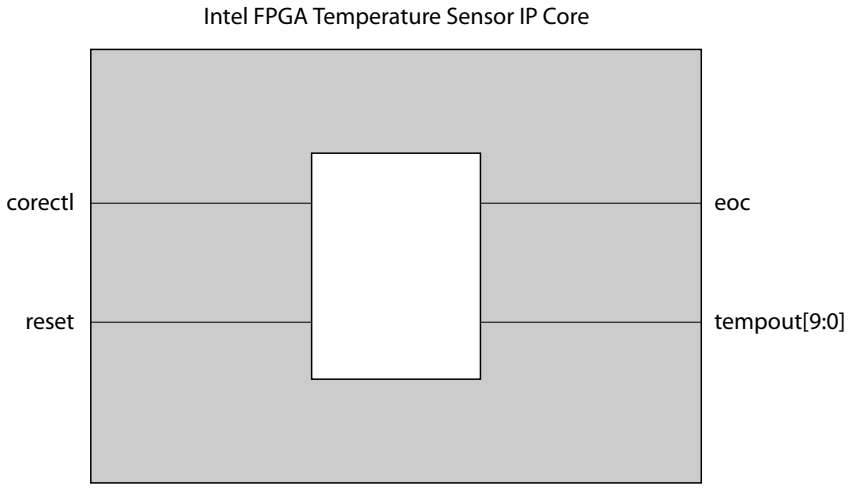
Device	Features
Stratix® V, Stratix IV, Arria® V, and Arria V GZ	• An internal TSD with built-in 8-bit analog-to-digital converter (ADC) circuitry to monitor die temperature • A clock divider to reduce the frequency of the clock signal to 1 MHz or less before clocking the ADC • An asynchronous clear signal to reset the TSD block
Intel Arria 10 and Intel Cyclone® 10 GX	• An internal TSD with built-in 10-bit ADC circuitry clocked by 1 MHz internal oscillator to monitor die temperature • Does not require external clock source • An asynchronous clear signal to reset the TSD block

Note: The Intel FPGA Temperature Sensor IP core does not have simulation model files and cannot be simulated.

Intel FPGA Temperature Sensor Functional Description

Temperature Sensing Operation for Intel Arria 10 and Intel Cyclone 10 GX Devices

Figure 1. Intel FPGA Temperature Sensor IP Core Top-Level Diagram for Intel Arria 10 and Intel Cyclone 10 GX Devices



The following lists the features for Intel FPGA Temperature Sensor IP core for Intel Arria 10 and Intel Cyclone 10 GX devices:

- For Intel Arria 10 and Intel Cyclone 10 GX devices, the Intel FPGA Temperature Sensor IP core supports the instantiation of temperature sensor block in your design from the IP Catalog.
- The Intel Arria 10 and Intel Cyclone 10 GX temperature sensor block runs at 1 MHz, where the clock signal is coming from the internal oscillator that is located in the temperature sensor block. Within the block, 10-bit ADC circuitry is included for converting sensor's reading to digital output.
- The `corectl` signal is used as an enable signal. When asserting the `corectl` signal, the ADC starts the conversion and 10-bit data is available at `tempout` after 1,024 clock cycles. The `corectl` signal must remain asserted until the completion of 1,024 clock cycles. The `eoc` signal goes high for one clock cycle of the 1-MHz internal oscillator clock, indicating end of conversion. You can latch the data on `tempout` at the falling edge of `eoc`. When the `corectl` signal is left asserted, the ADC starts another conversion cycle and provides a new temperature value at `tempout`. However, if the `corectl` signal is de-asserted, `tempout` maintains its current temperature value until the `corectl` signal re-asserts, or the `reset` signal is asserted.
- You can reset the temperature sensor anytime by asserting the `reset` signal.

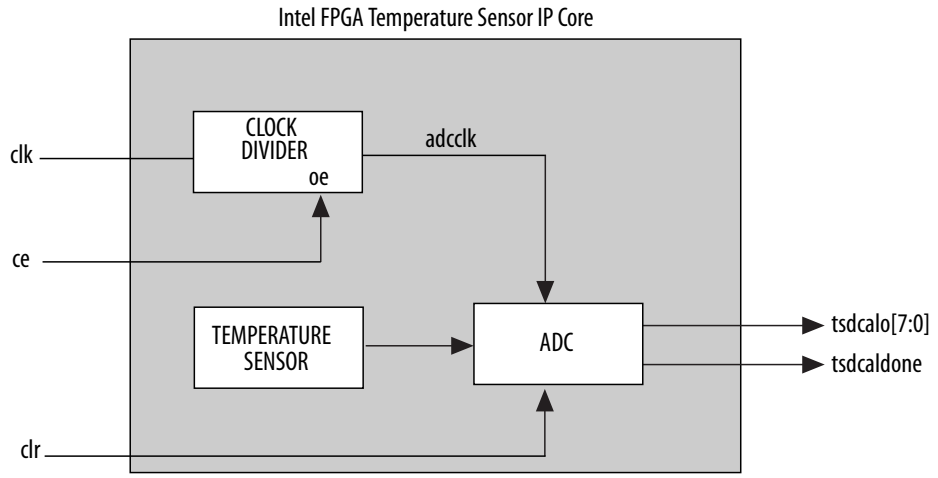
Related Information

Transfer Function for Internal TSD on page 10
Provides more information on how to calculate the temperature from the `tempout[9:0]` value.

Temperature Sensing Operation for Arria V, Arria V GZ, Stratix V, and Stratix IV Devices

Figure 2. Intel FPGA Temperature Sensor Block Diagram for Arria V, Arria V GZ, Stratix V, and Stratix IV Devices

This figure shows the top-level ports and the basic building blocks of the Intel FPGA Temperature Sensor IP core.



The Intel FPGA Temperature Sensor IP core runs at the frequency of the `clk` signal. The `clk` signal can run at a frequency of 80 MHz and below. The clock divider divides the `clk` signal to 1 MHz or less to feed the ADC. You can set the value of the clock divider using the Intel FPGA Temperature Sensor IP core parameter editor.

The `ce` signal connects to the output enable (`oe`) port of the clock divider block. Assert the `ce` signal to enable the Intel FPGA Temperature Sensor IP core. When you deassert the `ce` signal, the IP core disables the ADC, and maintains the previous values of the `tsdcalo[7..0]` and `tsdcaldone` signals unless you assert the `clr` signal, or reset the device. The `clr` signal is asynchronous, and you must assert the `clr` signal at least one clock cycle of the `adcclk` signal to clear the output ports.

Enabling the ADC allows you to measure the device temperature only once. To perform another temperature measurement, assert the `clr` signal, or reset the device. The `clr` signal is asynchronous, and you must assert the `clr` signal at least one clock cycle of the ADC `clk` signal to clear the output ports.

Note: When you choose not to create the `ce` port, the IP core connects the `ce` port to VCC. In this case, the ADC circuitry is always enabled. Intel recommends that you disable the ADC by deasserting the `ce` signal when the ADC is not in use to reduce power consumption.

During device power-up or when you assert the asynchronous `clr` signal, the Intel FPGA Temperature Sensor IP core sets the `tsdcaldone` port to `0` and the `tsdcalo[7:0]` signal to `11010101` or `0xD5`. After 10 clock cycles of the `adcclk` signal, the Intel FPGA Temperature Sensor IP core asserts the `tsdcaldone` signal to indicate that the temperature sensing operation is complete and that the value of the `tsdcalo[7:0]` signal is valid. The value of the `tsdcalo[7:0]` signal corresponds to the device temperature range. For more information about the value of

tsdcalo[7:0] signals, refer to the Related Information. To start another temperature sensing operation, assert the clr signal for at least one clock cycle of the adcclk signal, or reset the device.

Note: When you choose not to create the clr port , the Intel FPGA Temperature Sensor IP core connects the clr port to GND. In this case, you must reset the device to clear the output signals or start a temperature sensing operation. Intel recommends that you generate the clr port if you are planning to run the temperature sensing operation more than once.

If a derived PLL output clock is used to drive the Intel FPGA Temperature Sensor IP core, a minimum pulse violation might occur. When using the Intel FPGA Temperature Sensor IP core, you must ensure the clock applied must be less than or equal to 1 MHz. If you are using a higher frequency clock, the Intel FPGA Temperature Sensor IP core allows you use the 40 or 80 clock divider to reduce the clock frequency to be less than or equal to 1.0MHz.

Related Information

Intel FPGA Temperature Sensor IP Core Signals on page 10
Provides more information about the value of tsdcalo[7:0] that corresponds to the device temperature range.

Generating the Intel FPGA Temperature Sensor IP Core Example Design

To generate the Intel FPGA Temperature Sensor IP core, download the example design and follow these steps:

1. Open the **alttemp_sense_ex1.zip** file and extract **alttemp_sense_ex1.qar**.
2. In the Intel Quartus® Prime software, open the **alttemp_sense_ex1.qar** file and restore the archive file into your working directory.
3. On the IP Catalog window, search and click **Intel FPGA Temperature Sensor**.
4. In the **New IP Instance** dialog box, type tsd_s4 as your top-level file name.
5. In the Device family field, select Stratix IV.
6. Then, select your FPGA device family from the **Device Family** pull-down list. Click **OK**.
7. In the Parameter Editor, set the following parameter settings.

Table 2. Configuration Settings for the Intel FPGA Temperature Sensor IP Core

Option	Value
What is the input frequency?	**40** MHz
What is the clock divider value?	**80 MHz**
Create a clock enable port	Turned on
Create an asynchronous clear port	Turned on

8. Click **Finish**. The tsd_s4 module is built.

Related Information

Example Design

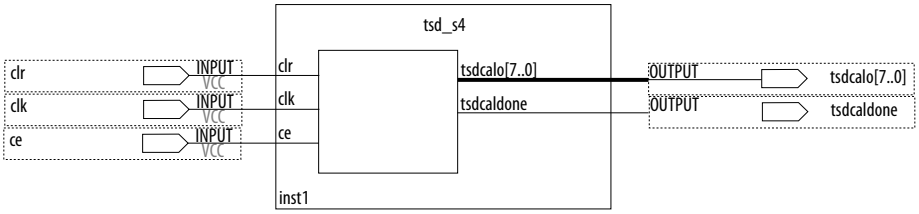
Compiling the Intel FPGA Temperature Sensor IP Core Example Design

To compile the Intel FPGA Temperature Sensor IP core in the Intel Quartus Prime software, follow these steps:

1. Open the top-level file **alttemp_sense_ex1.bdf** in the Intel Quartus Prime Block Editor software. This file contains the input and output assignments and a placeholder for the `tsd_s4` module.
2. To insert the `tsd_s4` module, double-click on the Block Editor window. The Symbol window appears.
3. Under **Name**, browse to the **tsd_s4.bsf** file.
4. Click **OK.**
5. Place the `tsd_s4` module onto the **INSERT TSD_S4 BLOCK HERE** placeholder so that the module aligns with the input and output ports.

Figure 3. Complete Design File

This figure shows the complete design file.



6. On the Processing menu, click **Start Compilation**.
7. When the **Full Compilation was successful** message box appears, click **OK**.

Using Clear Box Generator

You can use clear box generator, a command-line executable, to configure parameters that are in the Intel FPGA Temperature Sensor IP core parameter editor. The clear box generator creates or modifies custom IP core variations, which you can instantiate in a design file. The clear box generator generates IP core variation file in Verilog HDL or VHDL format.

Note: Intel Arria 10 and Intel Cyclone 10 GX Intel FPGA Temperature SensorIP core do not support clear box generation format.

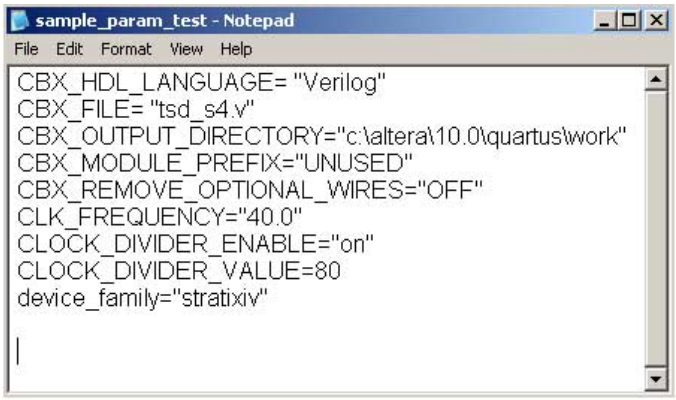
To generate the Intel FPGA Temperature Sensor IP core using the clear box generator, perform the following steps:

1. Create a text file (**.txt**) that contains your clear box ports and parameter settings in your working directory.

   For example,
   c:**altera****10.0****quartus****work****sample_param_test.txt**.

   This figure shows a sample text file to generate the Intel FPGA Temperature Sensor IP core.

Figure 4. Sample Text File for Clear Box Generator



Note: Ensure that you enclose String-type values with double-quotes.

2. Access the command prompt of your operating system, and change the current directory to your working directory by typing the following command:

   ```
   cd c:\altera\10.0\quartus\work\
   ```

   The clear box executable file name is **clearbox.exe**.

   Note: When you install the Intel Quartus Prime software, the %QUARTUS_ROOTDIR%\bin is added into your system's environment variables. Therefore, you can run the clear box command from any directory.

3. To view the available ports and parameters for this IP core, type the following command at the command prompt of your operating system:

   ```
   clearbox alttemp_sense -h
   ```

4. To generate the Intel FPGA Temperature Sensor IP core variation file based on the ports and parameter settings in the text file, type the following command:

   ```
   clearbox alttemp_sense -f *.txt
   ```

   For example, `clearbox alttemp_sense -f sample_param_test.txt`

5. After the clear box generator generates the IP core variation files, you can instantiate the IP core module in a HDL file or a block diagram file in the Intel Quartus Prime software.

6. To view the estimated hardware resources that the Intel FPGA Temperature Sensor IP core uses, type the following command:

   ```
   clearbox alttemp_sense -f sample_param_test.txt -resc_count
   ```

   Note: This command does not generate a HDL file.

Intel FPGA Temperature Sensor Device Support

The Intel FPGA Temperature Sensor IP core supports the following device family:

- Intel Arria 10
- Intel Cyclone 10 GX
- Stratix V

- Stratix IV
- Arria V
- Arria V GZ

Intel FPGA Temperature Sensor Parameters

The parameters are applicable for all supported devices except Intel Arria 10 and Intel Cyclone 10 GX devices. There are no available parameters for Intel Arria 10 and Intel Cyclone 10 GX devices.

You can parameterize the Intel FPGA Temperature Sensor IP core using the IP Catalog and parameter editor, or with the command-line interface (CLI). Use the parameter editor to quickly specify parameters in a GUI.

Expert users may choose to instantiate and parameterize the IP core through the command-line interface using the clear box generator command. This method requires you to have command-line scripting knowledge.

This table lists the parameter editor and CLI parameter settings for the Intel FPGA Temperature Sensor IP core.

Table 3. Intel FPGA Temperature Sensor IP Core Parameter Settings

Parameter		CLI Parameter		Description
Name	**Legal Values**	**Name**	**Legal Values**	
General Options Tab				
What is the input frequency?	**1.0** – **80.0 MHz**	clk_frequency	1.0 – 80.0	Specifies the input frequency of the `clk` signal. The input frequency value is type string, and the value must be less than or equal to the clock divider value. The default value is **1.0**
What is the clock divider value?	**40, 80**	clock_divider_value	`40, 80`	Specifies the clock divider value. The IP core divides the clock frequency value with the clock divider value before feeding the ADC. This option is only enabled when the `clk` signal frequency is more than 1 MHz. Intel recommends clocking the ADC with a 500 kHz signal. The CLI parameter is type integer. Ensure that you enable the clock divider by setting the `clock_divider_enable` parameter value to `on`. The default value is **40**.
Create a clock enable port	**On/Off**	`ce`	—	Specifies whether to turn on the asynchronous clock enable (`ce`) port. Turn on this option when you want to enable the Intel FPGA Temperature Sensor IP core. When you turn off this option, the clock enable port automatically connects to VCC.
Create an asynchronous clear port	**On/Off**	`clr`	—	Specifies whether to turn on the asynchronous clear (`clr`) port.

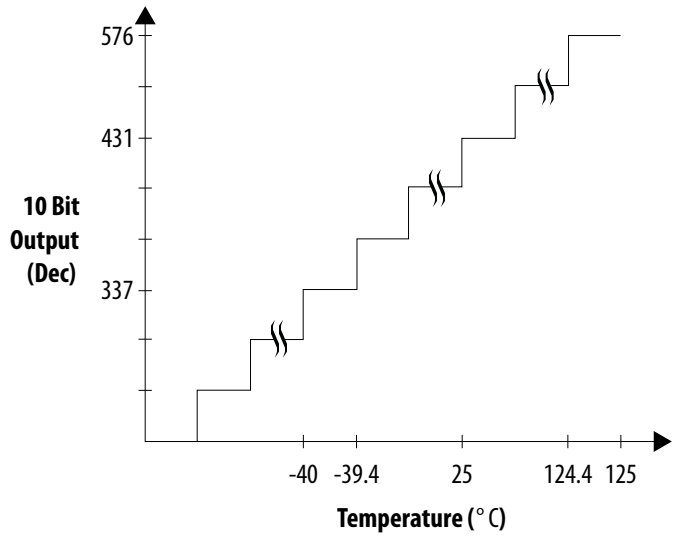
continued...

Parameter		CLI Parameter		Description
Name	Legal Values	Name	Legal Values	
				Turn on this option when you want to reset the Intel FPGA Temperature Sensor IP core. When you turn off this option, the clear port automatically connects to GND.

Transfer Function for Internal TSD

The following figure shows the transfer function for internal TSD.

Figure 5. ADC Transfer Function



You can calculate the temperature from `tempout[9:0]` value using this formula:

```
Temperature = {(AxC)÷1024} - B
```

Where:

- A = 693
- B = 265
- C = decimal value of `tempout[9..0]`

Intel FPGA Temperature Sensor IP Core Signals

The following tables list the Intel FPGA Temperature Sensor IP core signals.

Table 4. Intel FPGA Temperature Sensor IP Core Signals for Intel Arria 10 and Intel Cyclone 10 GX Devices

Signals	Direction	Width (Bit)	Description
corectl	Input	1	Enables the temperature sensing feature by the IP core.
reset	Input	1	Resets the temperature sensing block.
tempout[9:0]	Output	10	Resets the temperature sensing10-bit output data from internal ADC circuitry of temperature sensor block.
eoc	Output	1	Indicates end of internal ADC conversion. This signal goes high for one clock cycle of the 1-MHz internal oscillator clock and you can latch the data on tempout at the falling edge of eoc.

Table 5. Intel FPGA Temperature Sensor IP Core Signals for Arria V, Arria V GZ, Stratix V, and Stratix IV Devices

Signals	Direction	Width (Bit)	Description
clk	Input	1	Input clock signal that runs at a frequency of 80 MHz and below. The internal clock divider reduces the frequency of the clk signal to 1 MHz or less before clocking the ADC.
ce	Input	1	The asynchronous clock enable signal for the clk signal. This signal turns on/off the Intel FPGA Temperature Sensor IP core that implements the TSD block. This is an active-high signal. By default, this port connects to VCC.
clr	Input	1	The asynchronous clear signal. When you assert the clr signal, the IP core sets the tsdcalo[7:0] signal to 11010101 (0xD5) and the tsdcaldone signal to 0. This is an active-high signal. By default, this port connects to GND.
tsdcalo[7:0]	Output	8	8-bit output signal that contains the analog-to-digital-conversion temperature value. The 8-bit value maps to a unique temperature value. During device power-up or when you assert the clr signal, the IP core sets the tsdcalo[7:0] to 11010101 (0xD5).
tsdcaldone	Output	1	This signal indicates the completion of the temperature sensing process. The IP core asserts this signal when the process is complete. During device power-up or when you assert the clr signal, the IP core sets the tsdcaldone to 0.

Table 6. The Mapping of tsdcalo[7..0] Value to Arria V, Arria V GZ, Stratix V, and Stratix IV Devices Temperature

This table shows the value of tsdcalo[7:0] that corresponds to the device temperature range. The temperature specification ranges from -70° C to 127° C.

Value of tsdcalo[7:0] in Hexadecimal	Temperature in Degree Celsius (°C)
FF	127
...	...
E4	100
...	...
D5	85
...	...

continued...

Value of `tsdcalo[7:0]` in Hexadecimal	Temperature in Degree Celsius (°C)
D0	80
...	...
B2	50
...	...
9E	30
...	...
8A	10
...	...
80	0
...	...
76	-10
...	...
6C	-20
...	...
62	-30
...	...
4E	-50
...	...
3A	-70° C

Related Information

Transfer Function for Internal TSD on page 10
Provides more information on how to calculate the temperature from the `tempout[9:0]` value.

Intel FPGA Temperature Sensor Prototypes and Component Declarations

Verilog HDL Prototype

The Verilog HDL prototype is located in the `<Intel Quartus Prime installation directory>\eda\synthesis\altera_mf.v`

VHDL Component Declaration

The VHDL component declaration is located in the <Intel Quartus Prime installation directory>\libraries\vhdl\altera_mf\ directoryaltera_mf_components.vhd.

Document Revision History

This table lists the changes made to the document.

Document Version	Intel Quartus Prime Version	Changes
2018.05.30	17.1	Updated the description of the `reset` signal in the *Intel FPGA Temperature Sensor IP Core Signals for Intel Arria 10 and Intel Cyclone 10 GX Devices* table.

Date	Document Version	Changes Made
September 2017	2017.09.14	• Beginning from the Intel Quartus Prime software version 17.1, the name of this IP core has been changed from Altera Temperature Sensor IP Core to Intel FPGA Temperature Sensor IP Core. • Added Intel Cyclone 10 GX devices information. • Changed instances of Quartus II to Intel Quartus Prime. • Added the link to Intel FPGA Temperature Sensor IP core example design. • Added the Transfer Function for Internal TSD section. • Updated the Intel FPGA Temperature Sensor IP Core Top-Level Diagram for Intel Arria 10 and Intel Cyclone 10 GX Devices figure. • Updated the Temperature Sensing Operation for Intel Arria 10 and Intel Cyclone 10 GX Devices section. • Updated the `eoc` description in the Intel FPGA Temperature Sensor IP Core Signals for Intel Arria 10 and Intel Cyclone 10 GX Devices table.
May 2017	2017.05.08	Rebranded as Intel.
May 2015	2015.05.04	• Added a link on how to calculate the temperature from the `tempout[9:0]` value. • Editorial updates.
December 2014	2014.12.15	• Added Arria 10, Arria V, and Arria V GZ devices to the Device Support section. • Editorial changes to the warning message in Temperature Sensing Operation section. • Added Arria 10 devices information. • Updated template.
June 2013	3.1	• Updated the "Temperature Sensing Operation" on page 3–1 to clarify that enabling the ADC allows you to measure the temperature of the device only once and to include a warning about a minimum pulse violation when input clock derived from a PLL. • Updated "Features" on page 1–1 to notify that this IP core does not provide simulation feature.
September 2010	3.0	• Updated the Parameter Settings chapter. • Added the Prototypes and Component Declarations section. • Added the Clear Box Generator chapter.
February 2010	2.0	Updated the Temperature Sensing Operation section.
November 2009	1.0	Initial release.