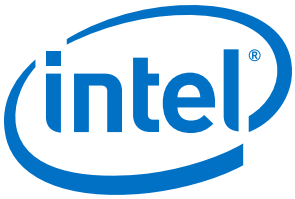

IOPLL Intel® FPGA IP Core User Guide

Updated for Intel® Quartus® Prime Design Suite: **18.1**

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Contents

IOPLL Intel® FPGA IP Core User Guide

The IOPLL Intel® FPGA IP core allows you to configure the settings of the Intel Arria® 10 and Intel Cyclone® 10 GX I/O PLL.

IOPLL IP core supports the following features:

- Supports six different clock feedback modes: direct, external feedback, normal, source synchronous, zero delay buffer, and LVDS mode.
- Generates up to nine clock output signals for the Intel Arria 10 and Intel Cyclone 10 GX devices.
- Switches between two reference input clocks.
- Supports adjacent PLL (`adjpllin`) input to connect with an upstream PLL in PLL cascading mode.
- Generates the Memory Initialization File (**.mif**) and allows PLL dynamic reconfiguration.
- Supports PLL dynamic phase shift.

Related Information

- Introduction to Intel FPGA IP Cores
  Provides more information about Intel FPGA IP cores and the parameter editor.
- Operation Modes on page 9
- Output Clocks on page 10
- Reference Clock Switchover on page 10
- PLL-to-PLL Cascading on page 11
- IOPLL Intel FPGA IP Core User Guide Archives on page 12
  Provides a list of user guides for previous versions of the IOPLL Intel FPGA IP core.

Device Family Support

The IOPLL IP core only supports the Intel Arria 10 and Intel Cyclone 10 GX device families.

IOPLL IP Core Parameters

The IOPLL IP core parameter editor appears in the PLL category of the IP Catalog.

IOPLL IP Core Parameters - PLL Tab

Table 1. IOPLL IP Core Parameters - PLL Tab

Parameter	Legal Value	Description
Device Family	**Intel Arria 10**, **Intel Cyclone 10 GX**	Specifies the device family.
Component	—	Specifies the targeted device.
Speed Grade	—	Specifies the speed grade for targeted device.
PLL Mode	**Integer-N PLL**	Specifies the mode used for the IOPLL IP core. The only legal selection is **Integer-N PLL**. If you need a fractional PLL, you must use the fPLL Intel Arria 10/Cyclone 10 FPGA IP core.
Reference Clock Frequency	—	Specifies the input frequency for the input clock, `refclk`, in MHz. The default value is **100.0 MHz**. The minimum and maximum value is dependent on the selected device.
Enable Locked Output Port	Turn on or Turn off	Turn on to enable the `locked` port.
Enable physical output clock parameters	Turn on or Turn off	Turn on to enter physical PLL counter parameters instead of specifying a desired output clock frequency.
Operation Mode	**direct**, **external feedback**, **normal**, **source synchronous**, **zero delay buffer**, or **lvds**	Specifies the operation of the PLL. The default operation is **direct** mode. • If you select the **direct** mode, the PLL minimizes the length of the feedback path to produce the smallest possible jitter at the PLL output.The internal-clock and external-clock outputs of the PLL are phase-shifted with respect to the PLL clock input. In this mode, the PLL does not compensate for any clock networks. • If you select the **normal** mode, the PLL compensates for the delay of the internal clock network used by the clock output. If the PLL is also used to drive an external clock output pin, a corresponding phase shift of the signal on the output pin occurs. • If you select the **source synchronous** mode, the clock delay from pin to I/O input register matches the data delay from pin to I/O input register. • If you select the **external feedback** mode, you must connect the `fbclk` input port to an input pin. A board-level connection must connect both the input pin and external clock output port, `fboutclk`. The `fbclk` port is aligned with the input clock. • If you select the **zero delay buffer** mode, the PLL must feed an external clock output pin and compensate for the delay introduced by that pin. The signal observed on the pin is synchronized to the input clock. The PLL clock output connects to the `altbidir` port and drives `zdbfbclk` as an output port. If the PLL also drives the internal clock network, a corresponding phase shift of that network occurs. • If you select the **lvds** mode, the same data and clock timing relationship of the pins at the internal SERDES capture register is maintained. The mode compensates for the delays in LVDS clock network, and between the data pin and clock input pin to the SERDES capture register paths.
Number of Clocks	**1**–**9**	Specifies the number of output clocks required for each device in the PLL design. The requested settings for output frequency, phase shift, and duty cycle are shown based on the number of clocks selected.
Specify VCO Frequency	Turn on or Turn off	Allows you to restrict the VCO frequency to the specified value. This is useful when creating a PLL for LVDS external mode, or if a specific dynamic phase shift step size is desired.

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Parameter	Legal Value	Description
VCO Frequency (1)	—	• When **Enable physical output clock parameters** is turned on—displays the VCO frequency based on the values for **Reference Clock Frequency**, **Multiply Factor (M-Counter)**, and **Divide Factor (N-Counter)**. • When **Enable physical output clock parameters** is turned off—allows you to specify the requested value for the VCO frequency. The default value is **600.0 MHz**.
Give clock global name	Turn on or Turn off	Allows you to rename the output clock name.
Clock Name	—	The user clock name for Synopsis Design Constraints (SDC).
Desired Frequency	—	Specifies the output clock frequency of the corresponding output clock port, `outclk[]`, in MHz. The default value is **100.0 MHz**. The minimum and maximum values depend on the device used. The PLL only reads the numerals in the first six decimal places.
Actual Frequency	—	Allows you to select the actual output clock frequency from a list of achievable frequencies. The default value is the closest achievable frequency to the desired frequency.
Phase Shift units	**ps** or **degrees**	Specifies the phase shift unit for the corresponding output clock port, `outclk[]`, in picoseconds (ps) or degrees.
Desired Phase Shift	—	Specifies the requested value for the phase shift. The default value is **0 ps**.
Actual Phase Shift	—	Allows you to select the actual phase shift from a list of achievable phase shift values. The default value is the closest achievable phase shift to the desired phase shift.
Desired Duty Cycle	**0.0–100.0**	Specifies the requested value for the duty cycle. The default value is **50.0%**.
Actual Duty Cycle	—	Allows you to select the actual duty cycle from a list of achievable duty cycle values. The default value is the closest achievable duty cycle to the desired duty cycle.
Multiply Factor (M-Counter) (2)	**4–511**	Specifies the multiply factor of `M`-counter. The legal range of the `M` counter is 4–511. However, restrictions on the minimum legal PFD frequency and maximum legal VCO frequency restrict the effective `M` counter range to 4–160.
Divide Factor (N-Counter) (2)	**1–511**	Specifies the divide factor of `N`-counter. The legal range of the `N` counter is 1–511. However, restrictions on the minimum legal PFD frequency restrict the effective range of the `N` counter to 1–80.
Divide Factor (C-Counter) (2)	**1-511**	Specifies the divide factor for the output clock (`C`-counter).

(1) This parameter is only available when **Enable physical output clock parameters** is turned off.

(2) This parameter is only available when **Enable physical output clock parameters** is turned on.

IOPLL IP Core Parameters - Settings Tab

Table 2. IOPLL IP Core Parameters - Settings Tab

Parameter	Legal Value	Description
PLL Bandwidth Preset	**Low**, **Medium**, or **High**	Specifies the PLL bandwidth preset setting. The default selection is **Low**.
PLL Auto Reset	Turn on or Turn off	Automatically self-resets the PLL on loss of lock.
Create a second input clk 'refclk1'	Turn on or Turn off	Turn on to provide a backup clock attached to your PLL that can switch with your original reference clock.
Second Reference Clock Frequency	—	Selects the frequency of the second input clock signal. The default value is **100.0 MHz**. The minimum and maximum value is dependent on the device used.
Create an 'active_clk' signal to indicate the input clock in use	Turn on or Turn off	Turn on to create the `activeclk` output. The `activeclk` output indicates the input clock which is in use by the PLL. Output signal low indicates `refclk` and output signal high indicates `refclk1`.
Create a 'clkbad' signal for each of the input clocks	Turn on or Turn off	Turn on to create two `clkbad` outputs, one for each input clock. Output signal low indicates the clock is working and output signal high indicates the clock is not working.
Switchover Mode	**Automatic Switchover**, **Manual Switchover**, or **Automatic Switchover with Manual Override**	Specifies the switchover mode for design application. The IP supports three switchover modes: • If you select the **Automatic Switchover** mode, the PLL circuitry monitors the selected reference clock. If one clock stops, the circuit automatically switches to the backup clock in a few clock cycles and updates the status signals, `clkbad` and `activeclk`. • If you select the **Manual Switchover** mode, when the control signal, `extswitch`, changes from logic high to logic low, and stays low for at least three clock cycles, the input clock switches to the other clock. The `extswitch` can be generated from FPGA core logic or input pin. • If you select **Automatic Switchover with Manual Override** mode, when the `extswitch` signal is low, it overrides the automatic switch function. As long as `extswitch` remains low, further switchover action is blocked. To select this mode, your two clock sources must be running and the frequency of the two clocks cannot differ by more than 20%. If both clocks are not on the same frequency, but their period difference is within 20%, the clock loss detection block will detect the lost clock. The PLL most likely drops out of lock after the PLL clock input switchover and needs time to lock again.
Switchover Delay	**0**–**7**	Adds a specific amount of cycle delay to the switchover process. The default value is 0.
Access to PLL LVDS_CLK/ LOADEN output port	**Disabled**, **Enable LVDS_CLK/ LOADEN 0**, or **Enable LVDS_CLK/ LOADEN 0 & 1**	Select **Enable LVDS_CLK/LOADEN 0** or **Enable LVDS_CLK/ LOADEN 0 & 1** to enable the PLL `lvds_clk` or `loaden` output port. Enables this parameter in case the PLL feeds an LVDS SERDES block with external PLL. When using the I/O PLL `outclk` ports with LVDS ports, `outclk[0..3]` are used for `lvds_clk[0,1]` and `loaden[0,1]` ports, `outclk4` can be used for `coreclk` ports.
Enable access to the PLL DPA output port	Turn on or Turn off	Turn on to enable the PLL DPA output port.

continued...

Parameter	Legal Value	Description
Enable access to PLL external clock output port	Turn on or Turn off	Turn on to enable the PLL external clock output port.
Specifies which outclk to be used as extclk_out[0] source	**C0** – **C8**	Specifies the `outclk` port to be used as `extclk_out[0]` source.
Specifies which outclk to be used as extclk_out[1] source	**C0** – **C8**	Specifies the `outclk` port to be used as `extclk_out[1]` source.

IOPLL IP Core Parameters - Cascading Tab

Table 3. IOPLL IP Core Parameters - Cascading Tab

Parameter	Legal Value	Description
Create a 'cascade out' signal to connect with a downstream PLL	Turn on or Turn off	Turn on to create the `cascade_out` port, which indicates that this PLL is a source and connects with a destination (downstream) PLL.
Specifies which outclk to be used as cascading source	**0**-**8**	Specifies the cascading source.
Create an adjpllin or cclk signal to connect with an upstream PLL	Turn on or Turn off	Turn on to create an input port, which indicates that this PLL is a destination and connects with a source (upstream) PLL.

IOPLL IP Core Parameters - Dynamic Reconfiguration Tab

Table 4. IOPLL IP Core Parameters - Dynamic Reconfiguration Tab

Parameter	Legal Value	Description
Enable dynamic reconfiguration of PLL	Turn on or Turn off	Turn on the enable the dynamic reconfiguration of this PLL (in conjunction with PLL Reconfig Intel FPGA IP core).
Enable access to dynamic phase shift ports	Turn on or Turn off	Turn on the enable the dynamic phase shift interface with the PLL.
MIF Generation Option (3)	**Generate New MIF File**, **Add Configuration to Existing MIF File**, and **Create MIF File during IP Generation**	Either create a new `.mif` file containing the current configuration of the I/O PLL, or add this configuration to an existing `.mif` file. You can use this `.mif` file during dynamic reconfiguration to reconfigure the I/O PLL to its current settings.
Path to New MIF file (4)	—	Enter the location and file name of the new `.mif` file to be created.
Path to Existing MIF file (5)	—	Enter the location and file name of the existing `.mif` file you intend to add to.

continued...

(3) This parameter is only available when **Enable dynamic reconfiguration of PLL** is turned on.

(4) This parameter is only available when **Generate New MIF File** is selected as MIF Generation Option.

(5) This parameter is only available when **Add Configuration to Existing MIF File** is selected as MIF Generation Option.

Parameter	Legal Value	Description
Enable Dynamic Phase Shift for MIF Streaming (3)	Turn on or Turn off	Turn on to store dynamic phase shift properties for PLL reconfiguration.
DPS Counter Selection (6)	**C0–C8**, **All C**, or **M**	Selects the counter to undergo dynamic phase shift. `M` is the feedback counter and `C` is the post-scale counters.
Number of Dynamic Phase Shifts (6)	**1–7**	Selects the number of phase shift increments. The size of a single phase shift increment is equal to 1/8 of the VCO period. The default value is **1**.
Dynamic Phase Shift Direction (6)	**Positive** or **Negative**	Determines the dynamic phase shift direction to store into the PLL MIF.

IOPLL IP Core Parameters - Advanced Parameters Tab

Table 5. IOPLL IP Core Parameters - Advanced Parameters Tab

Parameter	Legal Value	Description
Advanced Parameters	—	Displays a table of physical PLL settings that will be implemented based on your input.

Functional Description

An I/O PLL is a frequency-control system that generates an output clock by synchronizing itself to an input clock. The PLL compares the phase difference between the input signal and the output signal of a voltage-controlled oscillator (VCO) and then performs phase synchronization to maintain a constant phase angle (lock) on the frequency of the input or reference signal. The synchronization or negative feedback loop of the system forces the PLL to be phase-locked.

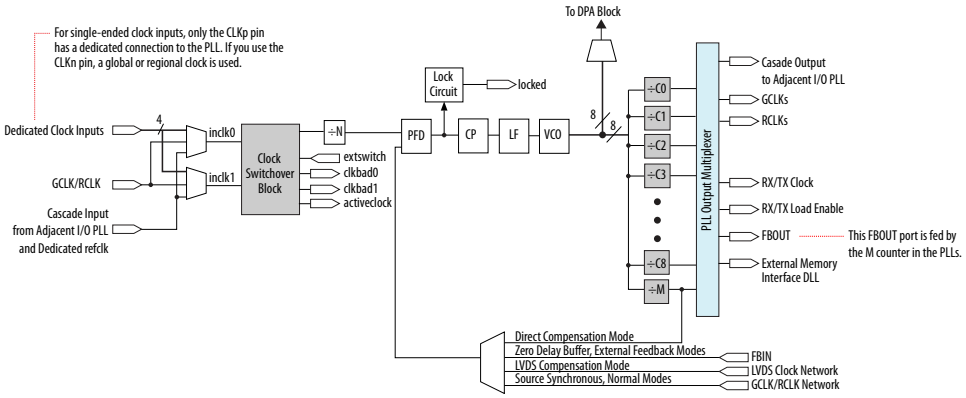
You can configure PLLs as frequency multipliers, dividers, demodulators, tracking generators, or clock recovery circuits. You can use PLLs to generate stable frequencies, recover signals from a noisy communication channel, or distribute clock signals throughout your design.

Building Blocks of a PLL

The main blocks of the I/O PLL are the phase frequency detector (PFD), charge pump, loop filter, VCO, and counters, such as a feedback counter (`M`), a pre-scale counter (`N`), and post-scale counters (`C`). The PLL architecture depends on the device you use in your design.

(6) This parameter is only available when **Enable Dynamic Phase Shift for MIF Streaming** is turned on.

Figure 1. Typical I/O PLL Architecture



The following terms are commonly used to describe the behavior of a PLL:

- PLL lock time—also known as the PLL acquisition time. PLL lock time is the time for the PLL to attain the target frequency and phase relationship after power-up, after a programmed output frequency change, or after a PLL reset.

  Note: Simulation software does not model a realistic PLL lock time. Simulation shows an unrealistically fast lock time. For the actual lock time specification, refer to the device datasheet.

- PLL resolution—the minimum frequency increment value of a PLL VCO. The number of bits in the M and N counters determine the PLL resolution value.
- PLL sample rate—the F_{REF} sampling frequency required to perform the phase and frequency correction in the PLL. The PLL sample rate is f_{REF} /N.

PLL Lock

The PLL lock is dependent on the two input signals in the phase frequency detector. The lock signal is an asynchronous output of the PLLs.

The number of cycles required to gate the lock signal depends on the PLL input clock which clocks the gated-lock circuitry. Divide the maximum lock time of the PLL by the period of the PLL input clock to calculate the number of clock cycles required to gate the lock signal.

Operation Modes

The IOPLL IP core supports six different clock feedback modes. Each mode allows clock multiplication and division, phase shifting, and duty-cycle programming.

The following list describes the operation modes for the IOPLL IP core:

- Direct mode—the PLL minimizes the feedback path length to produce the smallest possible jitter at the PLL output. In this mode, the PLL does not compensate for any clock networks.
- Normal mode—the PLL feedback path source is a global or regional clock network, minimizing clock delay from the input clock pin to the core registers through global or regional clock network.
- Source-Synchronous mode—the data and clock signals arrive at the input pins at the same time. In this mode, the signals have the same phase relationship at the clock and data ports of any Input Output Enable register.
- External Feedback mode—the PLL compensates for the `fbclk` feedback input to the PLL, thus minimizing the delay between the input clock pin and the feedback clock pin.
- Zero-Delay Buffer mode—the PLL feedback path is confined to the dedicated PLL external output pin. The clock port driven off-chip is phase aligned with the clock input for a minimal delay between the clock input and the external clock output.
- LVDS mode— maintains the same data and clock timing relationship of the pins at the internal SERDES capture register. This mode compensates for the LVDS clock network delay, plus any delay difference between the data pin and clock input pin to the SERDES capture register paths. The compensation mimic path mimics the clock and data delay of the receiver side.

Output Clocks

The IOPLL IP core can generate up to nine clock output signals. The generated clock output signals clock the core or the external blocks outside the core.

You can use the `reset` signal to reset the output clock value to 0 and disable the PLL output clocks.

Each output clock has a set of requested settings where you can specify the desired values for output frequency, phase shift, and duty cycle. The desired settings are the settings that you want to implement in your design.

The actual values for the frequency, phase shift, and duty cycle are the closest settings (best approximate of the desired settings) that can be implemented in the PLL circuit.

Reference Clock Switchover

The reference clock switchover feature allows the PLL to switch between two reference input clocks. Use this feature for clock redundancy, or for a dual clock domain application such as in a system. The system can turn on a redundant clock if the primary clock stops running.

Using the reference clock switchover feature, you can specify the frequency for the second input clock, and select the mode and delay for the switchover.

The clock loss detection and reference clock switchover block has the following functions:

- Monitors the reference clock status. If the reference clock fails, the clock automatically switches to a backup clock input source. The clock updates the status of the `clkbad` and `activeclk` signals to alert the event.
- Switches the reference clock back and forth between two different frequencies. Use the `extswitch` signal to manually control the switch action. After a switchover occurs, the PLL may lose lock temporarily and go through the reckoning process.

PLL-to-PLL Cascading

If you cascade PLLs in your design, the source (upstream) PLL must have a low-bandwidth setting, while the destination (downstream) PLL must have a high-bandwidth setting. During cascading, the output of source PLL serves as the reference clock (input) of the destination PLL. The bandwidth settings of cascaded PLLs must be different. If the bandwidth settings of the cascaded PLLs are the same, the cascaded PLLs may amplify phase noise at certain frequencies.

The `adjpllin` input clock source is used for inter-cascading between fracturable fractional PLLs.

Ports

Table 6. IOPLL IP Core Ports

Parameter	Type	Condition	Description
`refclk`	Input	Required	The reference clock source that drives the I/O PLL.
`rst`	Input	Required	The asynchronous reset port for the output clocks. Drive this port high to reset all output clocks to the value of 0. You must connect this port to the user control signal.
`fbclk`	Input	Optional	The external feedback input port for the I/O PLL. The IOPLL IP core creates this port when the I/O PLL is operating in external feedback mode or zero-delay buffer mode. To complete the feedback loop, a board-level connection must connect the `fbclk` port and the external clock output port of the I/O PLL.
`fboutclk`	Output	Optional	The port that feeds the `fbclk` port through the mimic circuitry. The `fboutclk` port is available only if the I/O PLL is in external feedback mode.
`zdbfbclk`	Bidirectional	Optional	The bidirectional port that connects to the mimic circuitry. This port must connect to a bidirectional pin that is placed on the positive feedback dedicated output pin of the I/O PLL. The `zdbfbclk` port is available only if the I/O PLL is in zero-delay buffer mode. To avoid signal reflection when using zero-delay buffer mode, do not place board traces on bidirectional I/O pin.
`locked`	Output	Optional	The IOPLL IP core drives this port high when the PLL acquires lock. The port remains high as long as the IOPLL is locked. The I/O PLL asserts the locked port when the phases and frequencies of the reference clock and feedback clock are the

continued...

Parameter	Type	Condition	Description
			same or within the lock circuit tolerance. When the difference between the two clock signals exceeds the lock circuit tolerance, the I/O PLL loses lock.
refclk1	Input	Optional	Second reference clock source that drives the I/O PLL for clock switchover feature.
extswitch	Input	Optional	Assert the extswitch signal low (1'b0) for at least 3 clock cycles to manually switch the clock.
activeclk	Output	Optional	Output signal to indicate which reference clock source is in used by I/O PLL.
clkbad	Output	Optional	Output signal that indicates the status of reference clock source is good or bad.
cascade_out	Output	Optional	Output signal that feeds into downstream I/O PLL.
adjpllin	Input	Optional	Input signal that feeds from upstream I/O PLL.
outclk_[]	Output	Optional	Output clock from I/O PLL.

IOPLL Intel FPGA IP Core User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
17.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
16.1	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
16.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide
15.0	Altera I/O Phase-Locked Loop (Altera IOPLL) IP Core User Guide

Document Revision History for the IOPLL Intel FPGA IP Core User Guide

Document Version	Intel Quartus® Prime Version	Changes
2019.01.03	18.1	• Updated the **Access to PLL LVDS_CLK/LOADEN output port** parameter in the *IOPLL IP Core Parameters - Settings Tab* table. • Updated the description for the zdbfbclk port in the *IOPLL IP Core Ports* table.
2018.09.28	18.1	• Corrected the description for extswitch in the *IOPLL IP Core Ports* table. • Renamed the following IP cores as per Intel rebranding: — Changed Altera IOPLL IP core to IOPLL Intel FPGA IP core. — Changed Altera PLL Reconfig IP core to PLL Reconfig Intel FPGA IP core. — Changed Arria 10 FPLL IP core to fPLL Intel Arria 10/Cyclone 10 FPGA IP core.

Date	Version	Changes
June 2017	2017.06.16	• Added support for Intel Cyclone 10 GX devices. • Rebranded as Intel.
December 2016	2016.12.05	Updated the description of the `rst` port of the IP core.
June 2016	2016.06.23	• Updated IP Core Parameters - Settings Tab table. — Updated the description for Manual Switchover and Automatic Switchover with Manual Override parameters. The clock switchover control signal is active low. — Updated the description for Switchover Delay parameter. • Defined `M` and `C` counters for DPS Counter Selection parameter in IP Core Parameters - Dynamic Reconfiguration Tab table. • Changed clock switchover port name from `clkswitch` to `extswitch` in Typical I/O PLL Architecture diagram.
May 2016	2016.05.02	Updated IP Core Parameters - Dynamic Reconfiguration Tab table.
May 2015	2015.05.04	Updated the description for `Enable access to PLL LVDS_CLK/LOADEN output port` parameter in IP Core Parameters - Settings Tab table. Added a link to the Signal Interface Between Altera IOPLL and Altera LVDS SERDES IP Cores table in the I/O and High Speed I/O in Arria 10 Devices chapter.
August 2014	2014.08.18	Initial release.