Ethernet Toolkit User Guide

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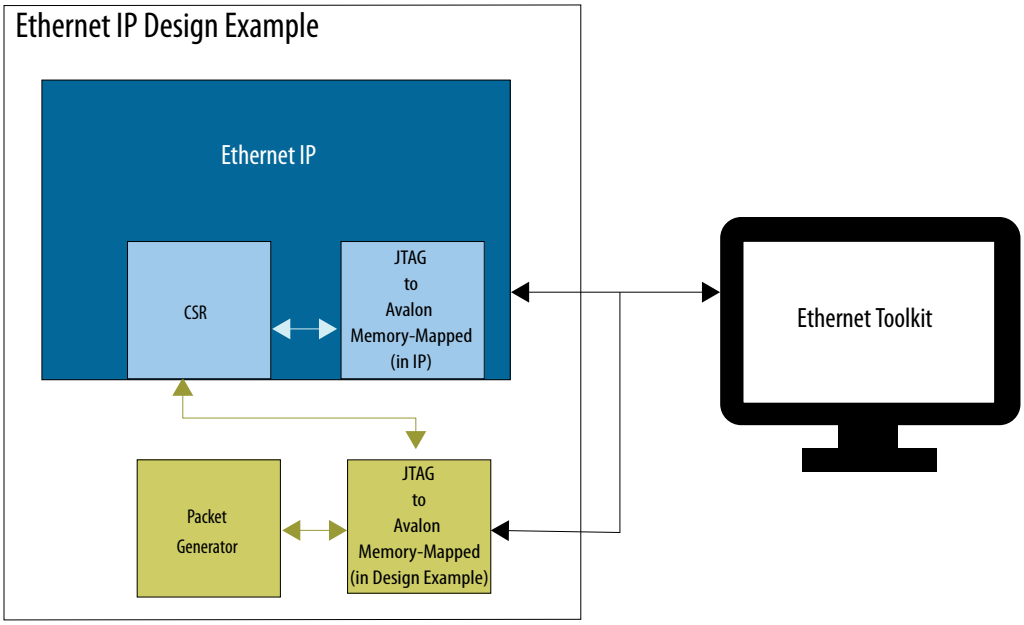
1. Ethernet Toolkit Overview

The Ethernet Toolkit is a TCL based debugging tool that allows you to interact with an Ethernet Intel FPGA IP in real time.

Figure 1. Block Diagram of the Ethernet Toolkit



You can use the Ethernet Toolkit with hardware design that has standalone Ethernet IP. You can also use the Ethernet Toolkit with an Intel® Quartus® Prime generated Ethernet IP design example.

1.1. Features

The Ethernet Toolkit offers the following features when used with hardware design that has standalone Ethernet IP as well as with an Intel Quartus Prime generated Ethernet IP design example:

- Verifies the status of the Ethernet link.
- Reads and writes to status and configuration registers of the IP.
- Displays the values of TX/RX status and statistics registers.
- Ability to assert and deassert IP resets.
- Verifies the IPs error correction capability.

The Ethernet Toolkit also offers some additional features when used with an Intel Quartus Prime generated Ethernet IP design example:

- Provides access to the example design packet generator.
- Execute testing procedures to verify the functionality of Ethernet IPs.
- Enable and disable MAC loopback.
- Set source and destination MAC addresses.

1.2. Supported Ethernet IP Cores and Devices

Table 1. Ethernet Toolkit Supported IP Cores, Devices, and Tiles

Supported Ethernet IP Cores	Supported Tile	Supported Device	Initial Supported Intel Quartus Prime Version	Initial Supported IP Version
Intel Stratix® 10 10GBASE-KR PHY IP	L- and H-tile	Intel Stratix 10	20.1	19.1.0
Low Latency 40G Ethernet Intel FPGA IP	L- and H-tile	Intel Stratix 10	20.1	19.1.0
Low Latency 100G Ethernet Intel FPGA IP	L- and H-tile	Intel Stratix 10	20.1	19.1.1
H-Tile Hard IP for Ethernet Intel FPGA IP	H-tile	Intel Stratix 10	20.1	19.2.0
Low Latency 40G for ASIC Proto Ethernet Intel FPGA IP	H-tile	Intel Stratix 10 GX 10M	20.1	19.1.0
E-Tile Hard IP for Ethernet Intel FPGA IP	E-tile	Intel Stratix 10	20.1	19.3.0
E-Tile Ethernet IP for Intel Agilex FPGA	E-tile	Intel Agilex™	20.1	19.3.0
Low Latency E-Tile 40G Ethernet Intel FPGA IP	E-tile	Intel Stratix 10	20.1	19.1.0
		Intel Agilex		
F-Tile Ethernet Intel FPGA Hard IP[1]	F-tile	Intel Agilex	21.3	3.0.0

(1) The Ethernet Toolkit is not available for the multi-instance IP design examples.

2. Setting up the Ethernet Toolkit

This section describes how to set up and run the Ethernet Toolkit for your Ethernet Intel FPGA IP.

2.1. System Requirements and Prerequisites

2.1.1. System Requirements

You must meet the following software and hardware requirements to run the Ethernet Toolkit:

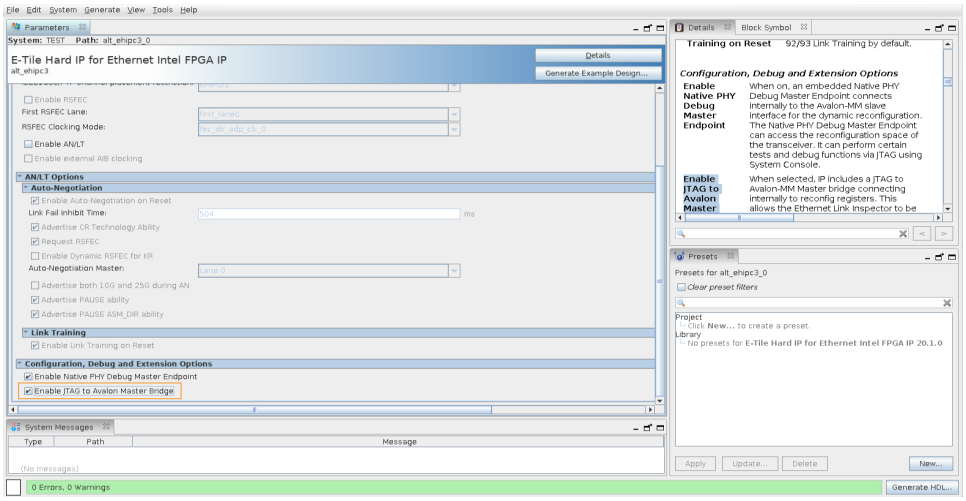
- Windows PC or Linux workstation
- Intel Quartus Prime Pro Edition software

  Note: Refer to Supported Ethernet IP Cores and Devices on page 4 for information on specific Intel Quartus Prime Pro Edition software version needed for each supported Ethernet Intel FPGA IP.
- Device specific Intel FPGA Development Kit that you use to run your Ethernet IP

2.1.2. Enabling your Design for the Ethernet Toolkit

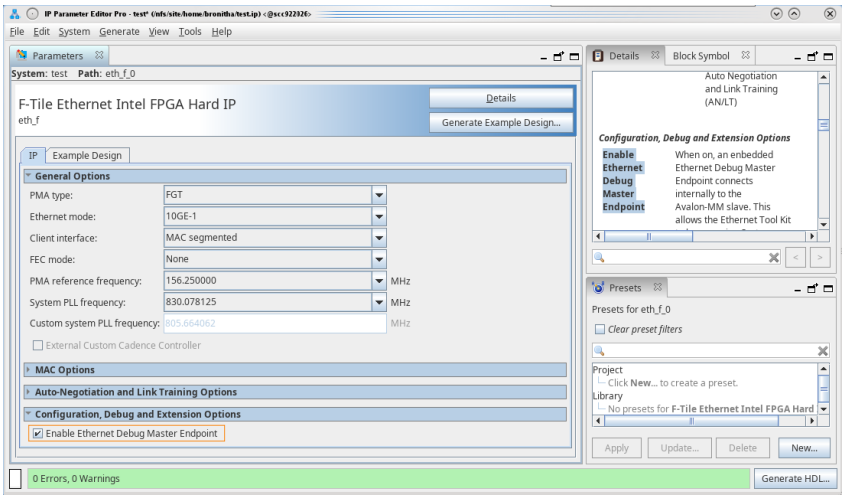
To enable the use of the Ethernet Toolkit for E-, H-, and L-Tile Ethernet IPs, you must turn on the **Enable JTAG to Avalon Master Bridge** parameter in the Ethernet IP parameter editor.

Figure 2. Example of E-Tile Hard IP for Ethernet Intel FPGA IP Parameter Editor



To enable the use of the Ethernet Toolkit for F-Tile Ethernet IP, you must turn on the **Enable Ethernet Debug Master Endpoint** parameter in the Ethernet IP parameter editor.

Figure 3. Example of F-Tile Ethernet Intel FPGA Hard IP Parameter Editor



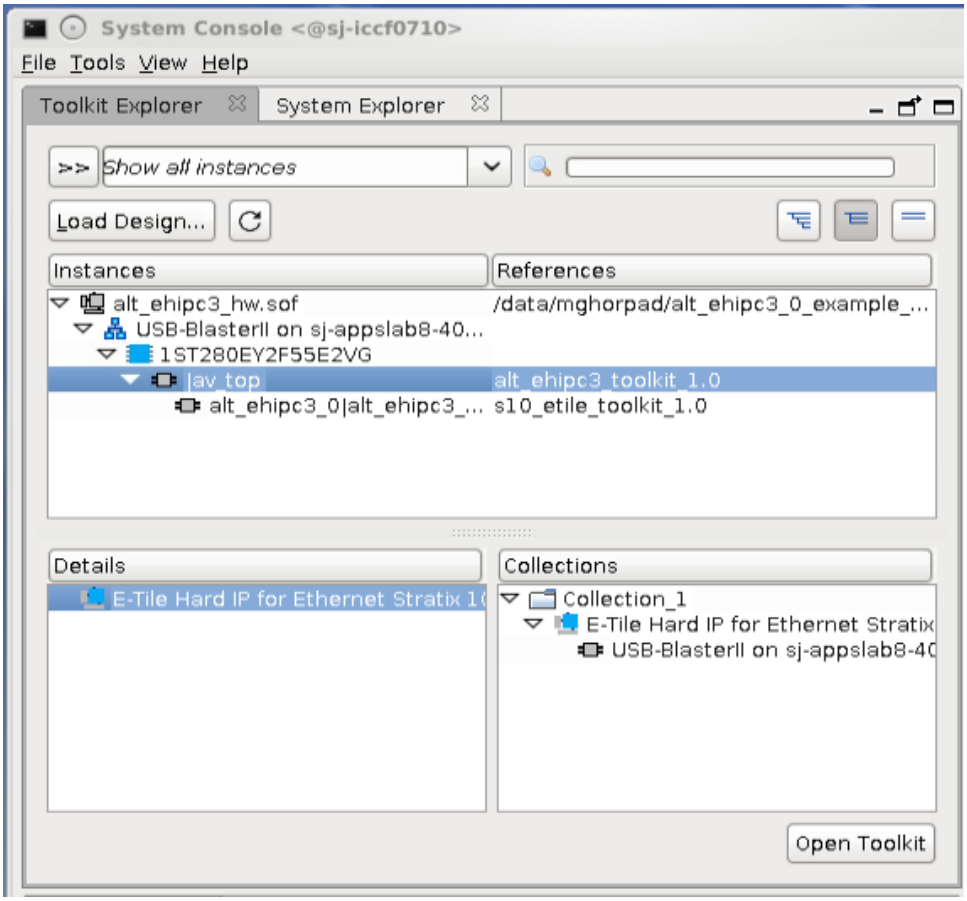
2.2. Running the Ethernet Toolkit

Before you begin with running the Ethernet toolkit, you must compile your Ethernet Intel FPGA IP with JTAG to Avalon Memory-Mapped master bridge parameter enabled.

Avalon® memory-mapped interface provides access to various toolkits. To avoid possible Avalon memory-mapped interface arbitration issues, ensure only one toolkit has access to the interface at the time.

If your E-tile Ethernet IP design example has auto-negotiation and link training enabled, set `0xB0[31]` register bit to `1` before accessing PMA registers via the transceiver reconfiguration interface. Read back `0xB0[31]` register bit to ensure no conflict with the auto-negotiation and link training function. For register description, refer to the *E-tile Hard IP User Guide*.

Figure 4. Opening Ethernet Toolkit in Intel Quartus Prime Software



Perform the following steps to launch the Ethernet Toolkit:

1. In the Intel Quartus Prime Pro Edition software, select **Tools ➤ System Debugging Tools ➤ System Console** to launch the system console.
2. In the system console, click **Load Design** in the **Toolkit Explorer** tab, and load the generated `.sof` file. If you already have Intel Quartus Prime project containing `.sof` is open, you just need to launch the system console.
3. You can see all of the Ethernet IP instances supported by Ethernet Toolkit within the design. Select one of the instances. The Ethernet Toolkit can automatically detect an instance of a supported Ethernet Intel FPGA IP within a design.
4. Now select the toolkit corresponding to the Ethernet IP that was selected in **Details** tab, and click **Open Toolkit**.

Related Information

- Analyzing and Debugging Designs with System Console
- E-tile Hard IP User Guide
- F-Tile Ethernet Intel FPGA Hard IP User Guide

3. Functional Description

The Ethernet Toolkit is a TCL-based graphical user interface (GUI). It allows you to perform sequences of read and write operations to CSRs, and it displays the read information visually through LEDs or text.

You can obtain the following information through the Ethernet Toolkit:

- Physical Coding Sublayer (PCS) status
- PHY status
- TX and RX Media Access Control (MAC) settings
- Auto Negotiation (AN), and Link Training (LT) status[2]
- Reed Solomon Forward Error Correction (RS-FEC) status

3.1. Ethernet Toolkit Groups and Tabs

The Ethernet Toolkit GUI is organized in the following groups and Tabs:

- IP Configuration and other Information
- General Commands
- Settings[3]
- Tabs:
  1. Status
  2. Statistics Counters
  3. Testing Features

Each group or tab can access various Control and Status Registers (CSR) of the selected Ethernet IP core.

[2] This feature is not available for F-Tile Ethernet Intel FPGA Hard IP in Intel Quartus Prime software version 21.3.

[3] This feature is not available for F-Tile Ethernet Intel FPGA Hard IP.

Figure 5. Ethernet Toolkit Groups and Tabs for E-, H-, and L-Tile Ethernet IPs

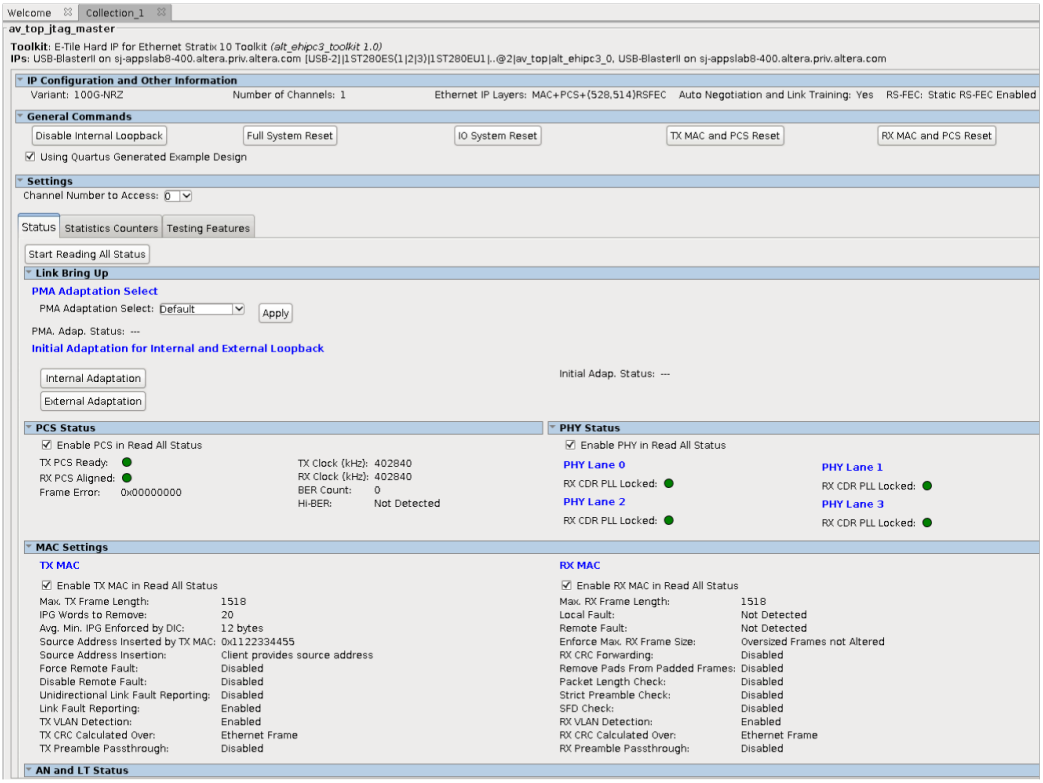
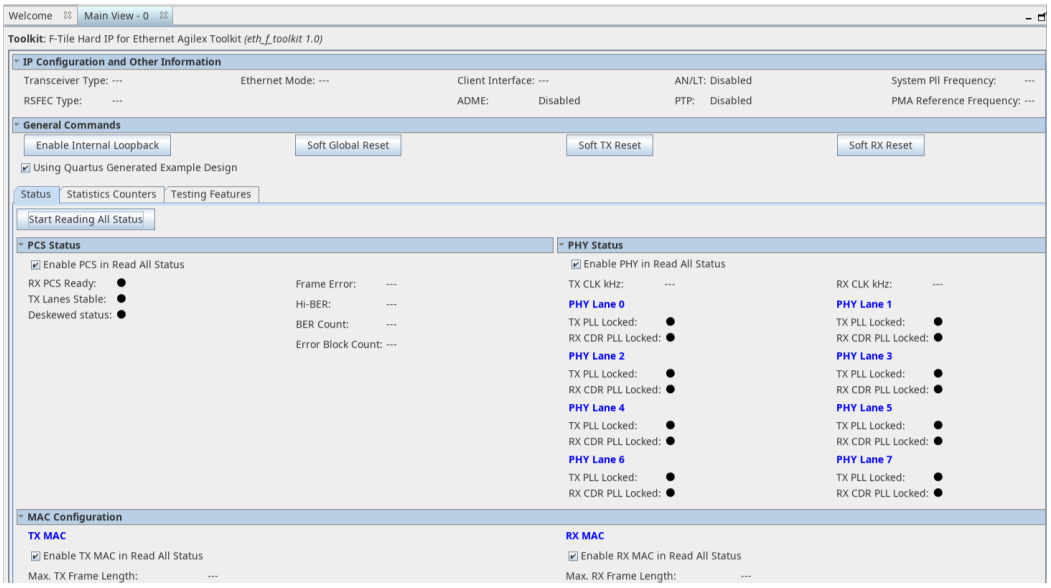


Figure 6. Ethernet Toolkit Groups and Tabs for F-Tile Ethernet IPs



The following sections include the examples of Ethernet Toolkit Groups and Tabs for E-Tile Hard IP for Ethernet Intel FPGA IP and F-Tile Ethernet Intel FPGA Hard IP.

3.1.1. IP Configuration and Other Information

This **IP Configuration and Other Information** group displays information about the variant of the Ethernet IP being used in the design.

Figure 7. Example of IP Configuration and Other Information Group for E-Tile Ethernet IP

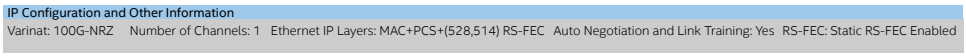
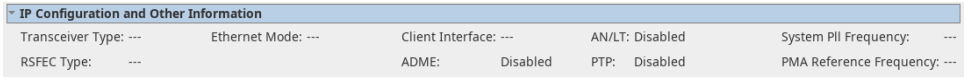


Figure 8. Example of IP Configuration and Other Information Group for F-Tile Ethernet IP



3.1.2. General Commands

The **General Commands** group provides option to assert and deassert the IP resets.

There is a checkbox for **Using Quartus Generate Example Design** that provides access to the example design packet generator, and to the PHY and packet generator loopback test. This option releases the JTAG master service provided by the JTAG to Avalon Memory-Mapped master bridge instantiated within the IP, and claims the master service provided by the JTAG to Avalon Memory-Mapped master bridge external to the IP, which the example design instantiates, allowing for the communication with the packet generator.

Figure 9. Example of General Commands Group for E-Tile Ethernet IP

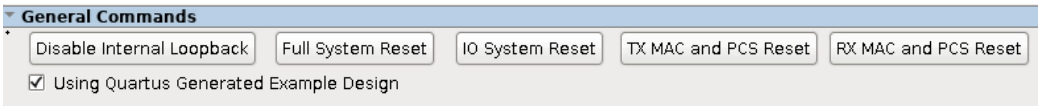
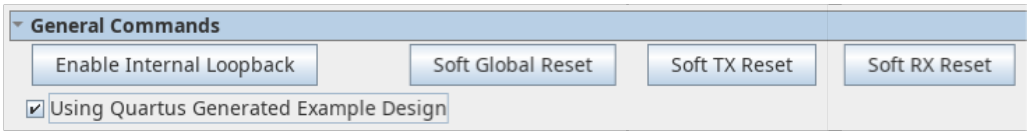


Figure 10. Example of General Commands Group for F-Tile Ethernet IP



3.1.3. Settings

This feature is only available for E-tile Ethernet IPs.

For the E-Tile Hard IP for Ethernet Intel FPGA IP and E-Tile Hard IP for Intel Agilex FPGA IP, the **Settings** group allows you to select the number of channels you want to access in case of multi-channel 10G/25G design. In case of Low Latency 40G Ethernet Intel FPGA IP and Low Latency 100G Ethernet Intel FPGA IP, you should see a text box that allow you to set the value of `clk_status` signal. This value is being used in calculation of TX and RX clock values.

Figure 11. Example of Settings Group

3.1.4. Status

The **Status** tab provides different values of various status and settings registers. You need to click **Start Reading All Status** button to start reading the registers. The read happens on discrete time intervals, and continue to read until you click **Stop Reading All Status** button.

The status tab of the Ethernet Toolkit has the following five tabs:

- Link Bring Up[(4)]
- PCS Status
- PHY Status
- MAC Settings
- AN and LT Status[(4)]

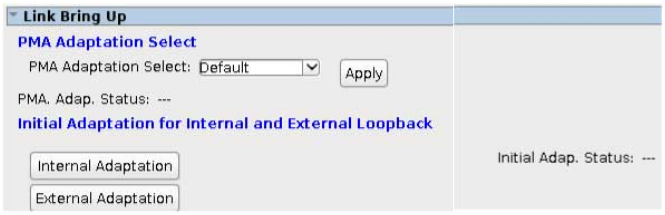
In each status tab, there is a checkbox that allows you to enable or disable that tab for the reading all status options.

For E-tile Ethernet IP designs, the Ethernet Toolkit is able to automatically detect AN/LT status tab if your design has AN/LT and RS-FEC functionalities enabled for the Ethernet instance. If you don't enable the AN/LT and RS-FEC functionality for your Ethernet design, these options are grayed out in the tool.

3.1.4.1. Link Bring Up

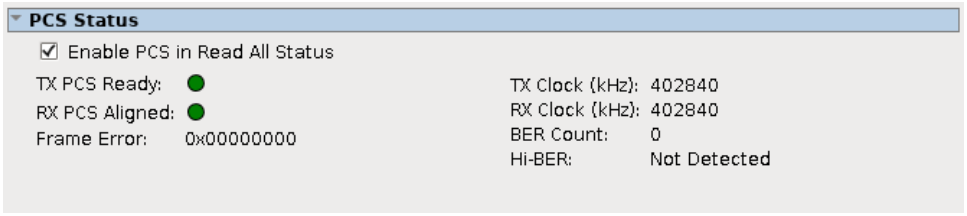
This feature is available for E-, H-, and L-tile Ethernet IPs.

Figure 12. Example of Link Bring Up Tab



3.1.4.2. PCS Status

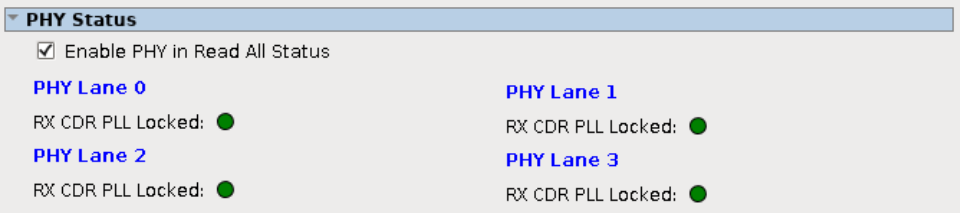
Figure 13. Example of PCS Status Tab



(4) This feature is only available for E-tile Ethernet IPs.

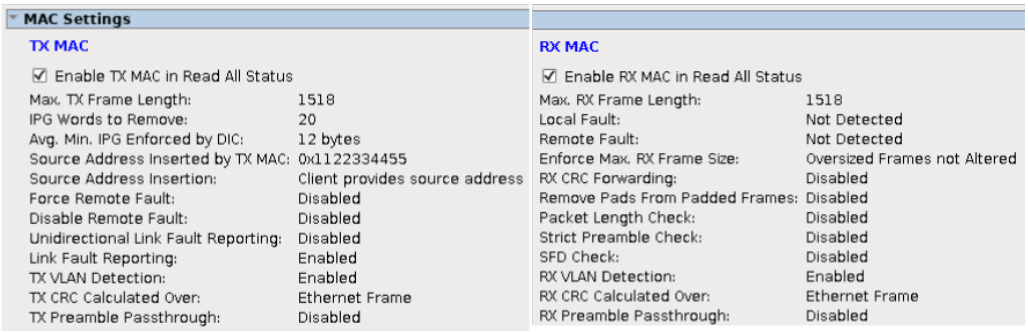
3.1.4.3. PHY Status

Figure 14. Example of PHY Status Tab



3.1.4.4. MAC Settings

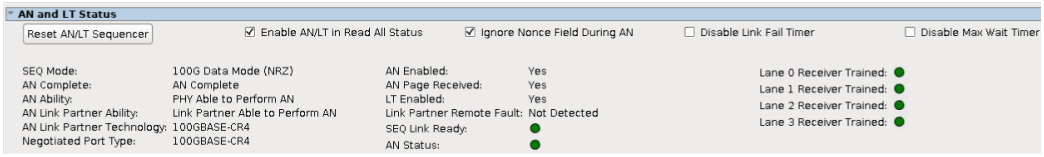
Figure 15. Example of MAC Settings Tab



3.1.4.5. AN and LT Status

This feature is only available for E-Tile Ethernet IPs.

Figure 16. Example of AN and LT Status Tab



3.1.5. Statistics Counters

The statistics counters tab has three following tabs:

- Example Design Packet Generator Settings
- Transmitter and Receiver Statistics
- RS-FEC

3.1.5.1. Example Design Packet Generator Settings

You can access **Example Design Packet Generator Settings** tab only if you are using an Intel Quartus Prime generated design example. You can start and stop the packet generator using the options from the tab. You can also set the source and destination address using this tab.

3.1.5.1.1. Packet Generator for E-, H-, and L-tile Ethernet IPs

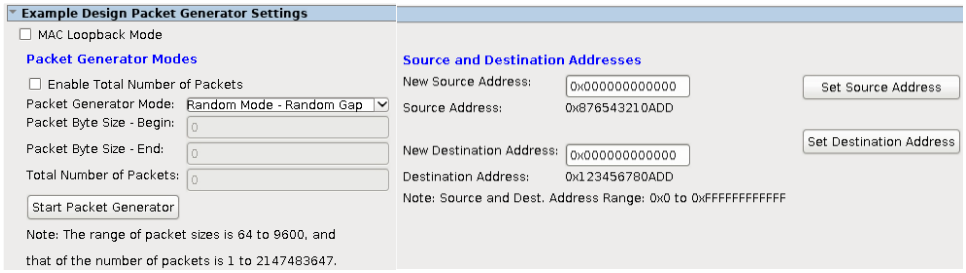
You can set the packet generator mode for the following options:

- Random Mode - Random Gap
- Random Mode - No Gap
- Fixed Size Mode
- Incremental Mode

You can set the total number of packets limit using the fixed size and incremental mode options.

Note: The **Example Design Packet Generator Settings** tab is not available for E-Tile Hard IP for Ethernet Intel FPGA IP and E-Tile Hard IP for Intel Agilex FPGA IP variants with PCS only and PCS+RS-FEC modes.

Figure 17. Example Design Packet Generator Settings Tab



3.1.5.1.2. Packet Generator for F-tile Ethernet IP

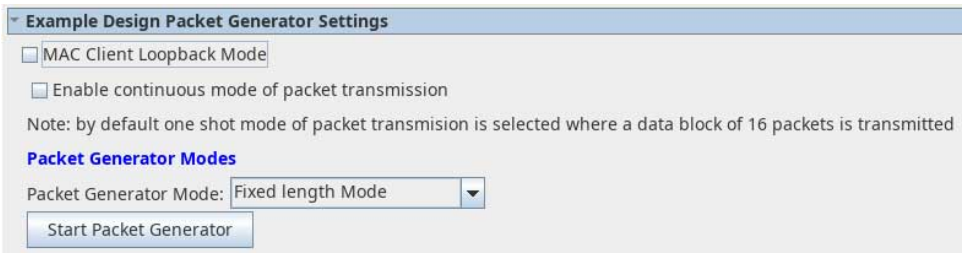
You can set the packet generator mode for the following options:

- **MAC Client Loopback Mode**: Performs exactly 16 packets transfers. Each packet has a start and a stop for each packet generation cycle.
- **Enable continuous mode of packet transmission**: Performs continuous packet generation. The packet generation is initiated by the start packet generation and terminated by the stop packet generation.

The types of packets sent to the packet generator are available in the following modes:

- **Fixed Length Mode**: Fixed packet length of 64 bytes with incremental data
- **Incremental Length Mode**: Incremental packet length of 64 - 79 bytes range with incremental data
- **Random Length Mode**: Random packet length with random data

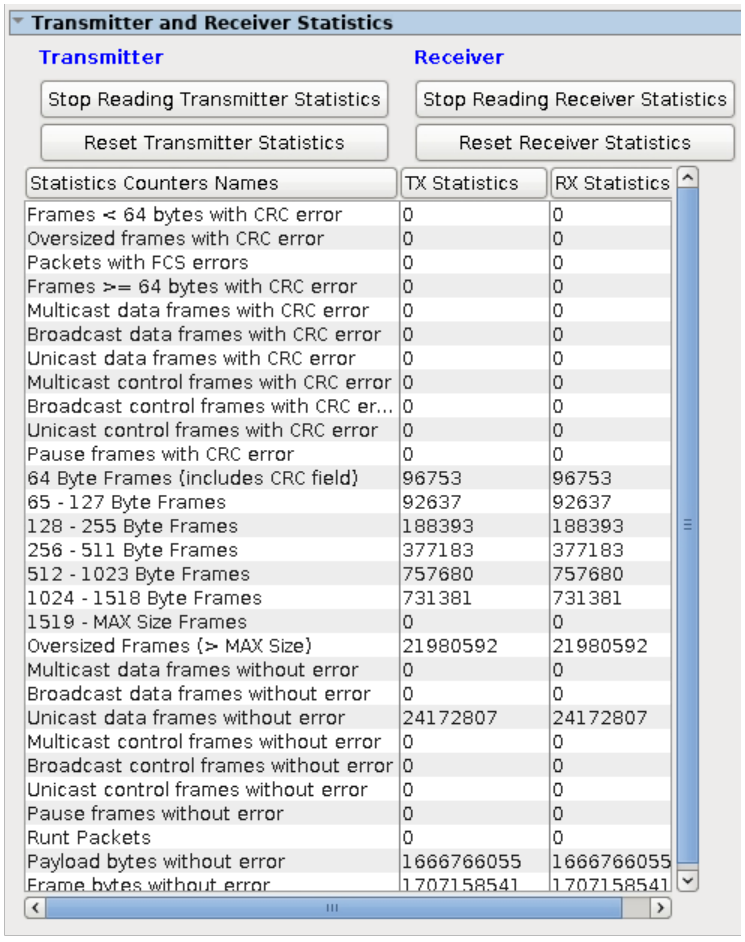
Figure 18. Example Design Packet Generator Settings Tab



3.1.5.2. Transmitter and Receiver Statistics

You can read multiple transmitter and receiver statistics registers in the **Transmitter and Receiver Statistics** tab. Click **Start Reading Transmitter** or **Start Reading Receiver** option to read the registers in discrete time intervals.

Figure 19. Example of Transmitter and Receiver Statistics Tab

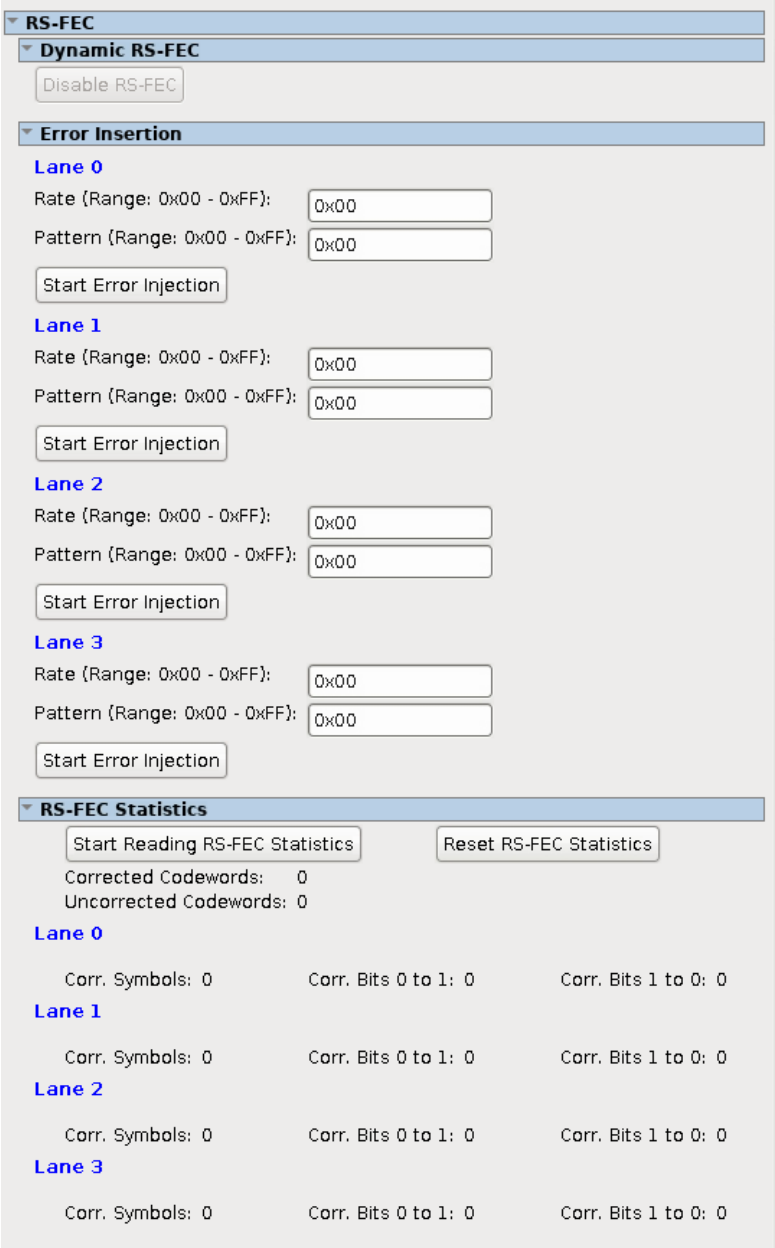


Statistics Counters Names	TX Statistics	RX Statistics
Frames < 64 bytes with CRC error	0	0
Oversized frames with CRC error	0	0
Packets with FCS errors	0	0
Frames >= 64 bytes with CRC error	0	0
Multicast data frames with CRC error	0	0
Broadcast data frames with CRC error	0	0
Unicast data frames with CRC error	0	0
Multicast control frames with CRC error	0	0
Broadcast control frames with CRC er...	0	0
Unicast control frames with CRC error	0	0
Pause frames with CRC error	0	0
64 Byte Frames (includes CRC field)	96753	96753
65 - 127 Byte Frames	92637	92637
128 - 255 Byte Frames	188393	188393
256 - 511 Byte Frames	377183	377183
512 - 1023 Byte Frames	757680	757680
1024 - 1518 Byte Frames	731381	731381
1519 - MAX Size Frames	0	0
Oversized Frames (> MAX Size)	21980592	21980592
Multicast data frames without error	0	0
Broadcast data frames without error	0	0
Unicast data frames without error	24172807	24172807
Multicast control frames without error	0	0
Broadcast control frames without error	0	0
Unicast control frames without error	0	0
Pause frames without error	0	0
Runt Packets	0	0
Payload bytes without error	1666766055	1666766055
Frame bytes without error	1707158541	1707158541

3.1.5.3. RS-FEC

You can use **RS-FEC** tab to perform error insertion. You can also read the RS-FEC registers using the **Start Reading RS-FEC Statistics** option which displays corrected and uncorrected codewords.

Figure 20. Example of RS-FEC Tab



3.1.6. Testing Features

The testing features contains three following tabs:

- Example Design PHY and Packet Generator Loopback Test

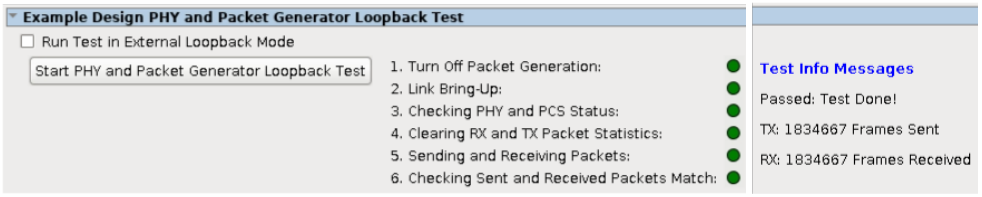
  Note: You can access this tab only if you are using an Intel Quartus Prime generated design example.
- Read Register
- Write to Register

3.1.6.1. Example Design PHY and Packet Generator Loopback Test

You can access **Example Design PHY and Packet Generator Loopback Test** tab only if you are using an Intel Quartus Prime generated design example. To use this tab of the Ethernet Toolkit, you must disable **MAC Loopback Mode** option in **Example Design Packet Generator Settings** group under **Statistics Counter** tab.

When you turn on the **Run Test in External Loopback Mode** option, the internal serial loopback is disabled for the IP. When you turn on the **Start PHY and Packet Generator Loopback Test** option, the test procedure runs a series of processes as shown in the figure below.

Figure 21. Example Design PHY and Packet Generator Loopback Test

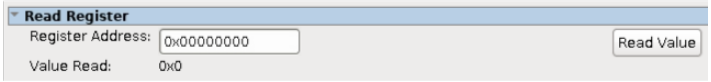


3.1.6.2. Read Register

You can directly read all accessible IP registers using **Read Register** tab by providing the 32-bit register base address.

Note: Do not attempt to access any register address that is reserved or undefined. Access to registers that do not exist in your IP core variation have unspecified results.

Figure 22. Example of Read Register

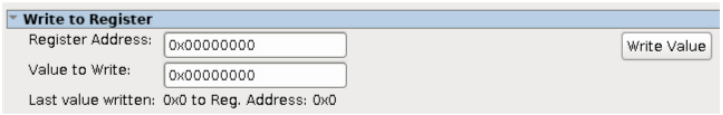


3.1.6.3. Write to Register

You can directly write to all accessible IP registers using **Write to Register** tab by providing the 32-bit register base address.

Note: Do not attempt to access any register address that is reserved or undefined. Access to registers that do not exist in your IP core variation have unspecified results.

Figure 23. Example of Write Register



3.2. Link Bring Up Guidelines

Refer to link bring up guidelines in individual Ethernet IP user guides and map the steps to GUI options and check boxes.

3.2.1. Example Link Bring Up using E-Tile Hard IP

This section covers an example of link bring up for the E-Tile Hard IP for Ethernet Intel FPGA IP. Perform the following steps to establish Ethernet link:

If your design (`.sof`) instantiates Ethernet IP with **Enable AN/LT** parameter enabled in IP parameter editor:

1. If you configure your IP in internal or external loopback, turn on the **Ignore Nonce** parameter and if you use only internal loopback then turn on **Enable Internal Loopback** parameter.
2. Click **Reset AN/LT Sequencer** in AN and LT status tab of the Ethernet Toolkit.

If your design (`.sof`) instantiates Ethernet IP with **Enable AN/LT** parameter disabled in IP parameter editor:

- If you configure your IP in internal loopback:
  1. Turn on **Enable Internal Loopback** parameter.
  2. Turn on **Initial Adaptation** parameter.
- If you configure your IP in external loopback or connected to link partner:
  1. Choose a recipe from the **PMA Adaptation Select** option and click **Apply**.
  2. Click **External Adaption** button.

3.2.2. Example Link Bring Up using F-Tile Ethernet Intel FPGA Hard IP

This section covers an example of link bring up using the Quartus-generated F-tile Ethernet IP design example. After you compile the F-tile Ethernet IP core design example and configure the appropriate device, you can use the System Console to program the IP core. Perform the following steps to establish the Ethernet link:

If you configure your IP in external loopback or connected to link partner:

1. In the Intel Quartus Prime Pro Edition software, go to **Tools ➤ In-System Sources and Probes Editor** window to assert and de-assert all resets. For more information, refer to *F-Tile Ethernet Intel FPGA Hard IP Design Example User Guide*.
2. Once the reset is initiated, navigate to **Tools ➤ System Debugging Tools ➤ System Console** window and load your `.sof` design.
3. Under **Statistics Counter** tab, navigate to the **Transmitter and Receiver Statistics**.
4. Click **Start Reading All Status**.
5. Click **Reset Receiver/Transmitter Statistics**.
6. Click **Start Packet Generator** in **Statistics Counter** tab and click **Start Reading Receiver/Transmitter Statistics**.

Related Information

F-Tile Ethernet Intel FPGA Hard IP Design Example User Guide

4. Document Revision History for the Ethernet Toolkit User Guide

Document Version	Changes
2021.10.04	• Globally added F-Tile Ethernet Intel FPGA Hard IP to the list of Ethernet Toolkit supported IP cores. — Updated existing descriptions if specific for E-Tile Ethernet IP. — Added new GUI screenshots and descriptions for F-Tile Ethernet IP. — Clarified the list of features supported for E-Tile Ethernet IP and F-Tile Ethernet IP • Separated *Example Design Packet Generator Settings* and *Link Bring-Up Guidelines* section to the E-, H-, and L-tile, and F-tile subsections. • Added new topic: *Example Link Bring-Up using F-Tile Ethernet Intel FPGA Hard IP*
2021.04.02	Updated *Running the Ethernet Toolkit*. Described a limitation for design examples with enabled auto-negotiation and link training.
2020.09.28	Initial release.