Intel® Agilex™ Device Family High-Speed Serial Interface Signal Integrity Design Guidelines
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1. Signal Integrity (SI) in High-Speed PCB Designs

Many factors impact high-speed, serial interface signal integrity, for example, insertion loss (IL), insertion loss deviation (ILD), return loss, crosstalk, and mode conversion. To mitigate these factors, you must first determine the loss budget for your targeted protocol. Second, select PCB materials and a stackup design that allow you to stay under your loss budget. Then design your PCB with these materials, and run channel compliance analysis.

The final steps are post-layout model extraction and end-to-end system simulation. Use IBIS-AMI models to conduct full-channel, end-to-end eye diagram simulations with the target BER of your targeted protocol. For more details about IBIS-AMI models, contact My Intel support.
1. Signal Integrity (SI) in High-Speed PCB Designs

**Figure 1. Signal Integrity Flow in High-Speed PCB Designs**

- **Target Protocol Standard**
  - Compute the channel loss budget for your target protocol standard
  - Estimate loss for each channel in the end-to-end channel

- **PCB Materials and Stackup-Design**
  - Estimate the differential trace insertion loss in dB/inch for your trace loss budget
  - Optimize trace geometries and impedance
  - Optimize PCB vias for the breakout layers
  - Optimize the connector footprint

- **PCB Design**
  - Define your FPGA breakout strategy including whether to use single-ended or neck-down differential pin escape routings
  - Define your differential P/N deskewing strategy
  - Minimize crosstalk with staggered breakout layers between adjacent pairs
  - Design for probing by adding ground vias next to signal pins

- **PCB Pre-layout Simulation**
  - Channel impedance corner sweep
  - Channel length/loss sweep
  - If the COM simulation fails, adjust the materials and stackup
  - Record the optimized transmitter equalization information from the COM simulation

- **PCB Post-layout Simulation**
  - For impedance and crosstalk validation, pick three or more pairs of channels with the worst via coupling for s-parameter extraction
  - Simulate P/N skew; then deskew the channels based on your simulation results
  - Perform time-domain, channel-eye simulation with IBIS-AMI models

**Related Information**

**My Intel Support**

1.1. Supported Protocols

For supported protocols, refer to the Intel® Agilex™ FPGA Device Overview. For device characteristics, refer to the Intel Agilex Device Data Sheet. For transceiver details, refer to the E-Tile Transceiver PHY User Guide. For protocol-specific layout requirements, refer to the relevant protocol specification.

**Related Information**

- Intel Agilex FPGA Device Overview
1.2. Channel Insertion Loss (IL) Budget Calculation

The following figure is an example of a channel IL budget calculation for an end-to-end (TP0 to TP5) 200GBASE-CR4 channel, with the IL estimation at the Nyquist frequency for each channel component provided. Estimate the minimum and maximum insertion loss allocations for each component of the channel (from the transmitter to the receiver) to meet the link standard (for example, IEEE 802.3cd).

Figure 2. 200GBase-CR4 End-to-End Channel IL Estimation Example

Assign a few dB of margin to the end-to-end channel PCB design to account for PCB and process, voltage, and temperature (PVT) variations.

- Nyquist frequency 13.28 GHz
- IL (TX PCB Via) = -1 dB
- IL (TX PCB Trace) = -6 dB
- IL (TX Connector + footprint) = -1.45 dB
- IL (Cable) = -12 dB
- IL (RX Connector + footprint) = -1.45 dB
- IL (RX PCB Trace) = -6 dB
- IL (RX PCB Via) = -1 dB
- Total IL = sum of IL = -28.9 dB

1.3. PCB Materials and Stackup Design Guidelines

The PCB stackup is the substrate upon which all design components are assembled. A well-designed PCB stackup can maximize the electrical performance of signal transmissions, power delivery, manufacturability, and long-term reliability of the finished product.

You need to know the following in order to decide the required number of signal and power layers.

- Board thickness requirements
- Connector requirements, for example, gold finger or edge finger
- Mechanical limitations
• PCB manufacturing capability limitations
• Your critical devices and their placement requirements
• High-speed signal data rate and connection requirements
• External memory interface configuration requirements
• The power tree and power budget for each power rail

1.3.1. Mitigating Insertion Loss with Dielectric Material

• Applications like E-tile to the quad small form factor pluggable double-density (QSFP-DD) interface and P-tile to the gold finger interface in a PCI Express* (PCIe*) add-in card have very strict IL requirements. Use the following dielectric constant (Dk) and dissipation factor (Df) values as a reference only for low-loss and ultra-low-loss dielectric materials. Test your design with a vector network analyzer (VNA).
  — Dk = 3.5 and Df = 0.007 (at 1 GHz) for low-loss material
  — Dk = 3.4 and Df = 0.002 (at 1 GHz) for ultra-low-loss material
• Use low-surface-roughness copper materials such as very low profile (VLP) and hyper very low profile (HVLP) to mitigate insertion loss caused by the skin effect. Copper resistance is a function of frequency, so, as the frequency increases, the resistive loss increases because of the skin depth (δ). This skin effect reduces the cross-sectional area of the channel, increasing the copper resistance.
• Use thick dielectric material (with the corresponding wider traces) for high-speed differential channel routing layers. Wider trace widths increase the effective surface area and reduce the skin effect.

1.3.2. Power Layers

For details about designing your power distribution network (PDN), see the Intel Agilex Device Power Distribution Network PCB Design User Guide.
• Use 1 or 2 oz. thick copper foil where possible to provide a stronger current carrying capability in the same routing space.
• For high current power rails, like the core power rail which may carry a current of more than 100 A, use multi-layers in parallel.
• When designing in multiple planes for a single supply, add enough stitching vias for the power planes to provide a low resistance vertical path.
• Place power layers next to a ground layers to create planar capacitance, which aids high-frequency decoupling, reduces electromagnetic interference (EMI) radiation, and enhances electromagnetic compliance (EMC) robustness. Because planar capacitance is inversely proportional to the dielectric thickness between the power and ground planes, choose thin dielectrics between the power and ground planes to increase the planar capacitance while reducing planar spreading inductance.

Related Information
Intel Agilex Device Power Distribution Network PCB Design User Guide
1.3.3. Reference Planes

- Make sure all high-speed signals reference to solid planes over the length of their routing (ground reference is preferred) and do not cross plane splits.
- Use a layer topology of ground-signal-ground for high-speed signal layers to provide good isolation and reference.

1.3.4. Layer Assignment

- For high-speed differential traces, avoid long via coupling between the closest transmit (TX) and receive (RX) transceiver channels.
- Make sure the via coupling length is as short as possible to reduce crosstalk.
- Use shallow layers for high-speed signals, especially for lanes that support PAM4.

1.3.5. Impedance

- Strictly control the impedance tolerance of high-speed traces. Generally, ten percent can be used for stripline impedance, but seven percent is better.
- Breakout routing usually has limited routing space which may cause impedance discontinuity. Optimize breakout routing trace geometries to reduce the impedance discontinuity for better return loss performance.

1.3.6. Via Drill Size

- The aspect ratio (AR) is the ratio of a via length or depth to its drill hole diameter. An AR of 15 is a common manufacturing capability provided by PCB vendors, but PCB vendors define the exact AR based on the board thickness specified by their manufacturing capabilities.
- To meet the target differential via impedance, the optimized anti-pad size is usually larger than the default via anti-pad which may cause a reference issue for breakout routing in the BGA area. Check via impedance with time domain reflectometry (TDR), and use a teardrop or wider trace segment in the breakout area for a smooth impedance transition to the global area.

1.3.7. Fiber Weave

- A composite of fiber and resin make up the PCB material. The strand bundles of fiber run perpendicular to each other. Depending on the orientation of the weave relative to the trace, there can be a resin or a fiber bundle beneath the trace. The differing dielectric constants of these two materials may introduce a phase skew among signals that comprise a differential pair, manifesting itself as an AC common mode noise at the receiver, affecting both the voltage and timing margin at the receiver. This is the fiber weave effect. To mitigate the fiber weave effect, specify a dense spread of weave (1078, 1067, 2116, 2113) rather than a sparse weave (106, 1080) for prepreg\(^{(1)}\) and core.
- Use a 2-ply (1078x2, 1078+1067) prepreg and core to mitigate the fiber weave effect.
- For more details about the fiber weave effect, refer to AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing.
1.3.8. Reference Stackup

The following figure is a PCIe add-in card reference stackup example. With 18 layers, it is a total of 62 mils thick. It has two 1 oz power layers at the center of the stackup, isolated with two ground layers on each side. The ground-signal-ground layer pattern is used for all signal layers, and a dense weave (1078, 1035) prepreg and core were used for dielectric prepreg and core.

(1) "Prepreg" is an abbreviation of "pre-impregnated material," in this case, referring to the PCB fiberglass impregnated with resin (an epoxy-based material) used in multilayer boards.
1.4. PCB Design Guidelines

1.4.1. General PCB Design Guidelines

Each component in a high-speed channel can impact the overall system performance. From end-to-end, these components are the device packages, PCB traces, PCB vias, connectors, cables, and landing pads of integrated circuit pins, connector pins, and alternating current (AC) coupling capacitor pins.
1.4.1.1. PCB Traces

- Use stripline routing for better far end crosstalk performance and a tight impedance tolerance, and keep trace lengths shorter than the maximum allowed length limited by the full-channel IL and eye diagram simulation results.

- Follow the general stripline pair-to-pair spacing rule of 5H for TX-to-TX and RX-to-RX, 9H for TX-to-RX, TX-to-others, and RX-to-others, where 'H' is the dielectric distance from the signal layer to the closest reference layer.

- Use a solid ground reference for high-speed differential pairs.

- Keep at least 5H of spacing between the edge of a trace and the void and between the edge of a trace and the edge of the reference plane in the open field area.

- Maintain symmetrical routing between two signals that comprise a differential pair from end to end, including the trace length, the transition via location, and the placement of DC blocking capacitors. Failure to maintain layout symmetry introduces differential-to-common-mode or common-to-differential-mode conversion AC noise.

**Figure 4. Symmetrical and Non-symmetrical Routing Examples**

Avoid: Non-symmetrical Routing

Preferred: Symmetrical Routing

- Breakout routing usually has a smaller trace width and smaller pair-to-pair spacing, so keep the breakout routing as short as possible to minimize reflection and insertion loss and reduce crosstalk.

- To mitigate near end crosstalk, route the high-speed TX and RX signals on different layers, or separate the TX and RX signals with large spacing of at least 9H in the stripline layer.

- In the BGA pin field via array, avoid high-speed traces routed between two vias that comprise a differential via, and make the coupling area between the high-speed trace and via as small as possible. Follow the guidelines in the following figure to minimize crosstalk in the pin field area. Note that each differential pair has a short bar connecting the P and N in the figure to indicate the differential via.
Figure 5. **Routing Rule in Hex Pattern Pin Field Via Array**

- Preferred Patterns with Minimum Crosstalk
- Acceptable Patterns with Moderate Crosstalk
- Not-recommended Patterns

Figure 6. **Breakout Routing Example of Hex Pattern BGA**

- To increase the common mode noise immunity, start differential pair P/N deskew at the transmitter, end deskew at the receiver, and compensate for the skew after the skew happens and close to the point where the variation occurs.

Figure 7. **Intra-pair Deskew Close to the Skew Happened Location**
Minimize serpentine layouts, making them transparent to the signal, because serpentine layouts introduce discontinuity to the differential channel. You can minimize them by making electrical lengths shorter than the signal rise time. In general, keep the serpentine routing length <100 mils with arcs and bends of 45 degrees. A loosely coupled differential pair is less affected by serpentine lines.

**Figure 8. Deskew Trombone Routing Rule**

A loosely coupled differential pair is less affected by serpentine lines.

Intra-pair differential skew compensation
Recommended dimensions: A = B = C = D,
E = F = G = 3W (W = trace width) and S2<2S1

Do not use tightly coupled high-speed differential pairs for a given routing density because they increases the impedance fluctuation caused by the deskew trombone and manufacturing tolerance. The general rule for intra-pair spacing is between one and two times the trace width.

Use arc routing for high-speed differential traces.

Use teardrop traces for high-speed differential traces in the pad and via area.

Mitigate the fiber weave effect with techniques like zig-zag routing and image rotation (see below).

The following figure shows zig-zag routing. If the weave is aligned to the PCB edges, follow a zig-zag routing of differential traces. Generally, maintain a minimum angle of 10 degrees between the trace and fiber weave; this angles traces relative to the PCB edge. For more details about the fiber weave effect, refer to AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing.

**Figure 9. Zig-Zag Routing**

Another solution is image rotation that maintains an angle between the trace and the fiber weave pattern. Rotate until the traces are at a 10 degree angle relative to the fiber weave. Rotate by cutting the PCB board at an angle, as shown in following figure, or by rotating the layout database relative to the edge of the PCB board.
1. Signal Integrity (SI) in High-Speed PCB Designs

Figure 10. Cutting the PCB Board to Rotate the Image Relative to the Fiber Weave Pattern

Related Information
AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing

1.4.1.2. PCB Vias

- Vias impact high-speed channel loss and the jitter budget, so use as few vias as possible for the high-speed differential channel.
- Keep impedance continuity between the high-speed PCB via and trace. Vias usually have higher capacitance and lower impedance than traces.
- Optimize via impedance, using a 3D electromagnetic (EM) solver, by sweeping the anti-pad width, length, and radius for your specific stackup, drill size, and via stub. Keep in mind that:
  - The smaller the drill size, the higher the via impedance
  - The larger the anti-pad size, the higher the via impedance
  - The shorter the via stub, the higher the via impedance
  - The smaller the via top, bottom, and functional pads, the higher the impedance
Figure 11. Hex Pattern BGA Via Optimization

- Make sure that each high-speed signal via has a ground via for reference, and make sure that the two signal vias of a differential pair have symmetrical ground vias as the above figure shows. If you do not do this, mode conversion is introduced.

- Remove non-functional pads for high-speed signal vias and ground vias to lower via capacitance.

- Make the closest TX and RX signal via coupling length as short as possible through an appropriate layer assignment.

Stackup: 22 layers, 2.7 mm thick
Pin pitch: 1 mm
Via drill diameter: 8 mils
Pad diameter: 16 mils
Target impedance: 95 Ω
Reference anti-pad for top to layer 7 via:
  - Anti-pad width = 24 mils
  - Anti-pad length = 67.37 mils
  - Anti-pad radius = 14 mils
Figure 12. Via Coupling Reduction by Routing Layer Assignment

- During insertion loss evaluation, there is a resonance that can occur in the frequency range of three times the Nyquist frequency. Control the via stub length to avoid this.

1.4.1.3. Connector Breakout

For high-speed routing, use the correct breakout orientation to avoid long stubs caused by the connector pin and PCB pad.

Figure 13. Connector Pin and PCB Pad Connection

This is a surface-mount, ground-signal-signal-ground connector pin interconnection with the PCB. The different layers in the stackup are indicated with different colors.

Optimize and tune the connector break-in and breakout to reach the target trace impedance and increase continuity. To test the interaction between the connector pin and PCB pad, co-simulate the connector-to-PCB interaction with the connector structures included in a 3D EM simulation tool.
1.4.1.4. DC Blocking Capacitor

The layout design of DC blocking capacitors can impact high-speed channel performance.

- Use a 0402 or 0201 size capacitor for a smaller parasitic and smaller footprint.
- Place the DC blocking capacitors at the device end or connector end. Do not place them in the middle of the trace routing.
- Keep the placement of the DC blocking capacitors on the two lines of a differential pair symmetrical, make sure that the fan-in and fan-out routing of the capacitors is symmetric, and make sure the line lengths on either side of the capacitors match.
- Similar to the connector landing pad, optimize the cut-out size under the capacitor pad using a 3D EM simulation tool for your specific stackup and capacitor pad size. Some basic rules to start with:
  - Cut the direct, next-layer ground plane of the capacitor pad.
  - Keep a gap greater than 1H between the edge of the AC capacitor pad and the adjacent ground planes.

Figure 14. DC Blocking Capacitor Layout
1.4.1.5. Others

- Do not route high-speed differential traces under power connectors, power delivery inductors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices, or integrated circuits that use or duplicate clocks.
- Keep large spacing between high-speed traces, vias, and pads and high-noise power nets, a spacing of greater than 100 mils is preferred. High-noise power nets are nets like the switching node (phase node) of a voltage regulator module (VRM), 12 V power net, and high current transient power net.
- If a dog-bone fan-out was used in the BGA pin area, use a ground reference plane cutout under the high-speed signal pad to reduce the capacitance.

1.4.2. E-Tile and H-Tile PCB Design Guidelines

- Use a trace impedance of 90-100 Ω for differential signals. The normal package impedance of the Intel Agilex FPGA interface is 90 Ω.
- Route lanes that support 56G PAM4 on shallow layers to reduce via length, with connectors placed on the PCB close to the FPGA to reduce trace length.
- Make via stubs as short as possible. Use top-drill, back-drill, buried via, blind via, and micro-via techniques as necessary to shorten the via stubs. Stub lengths of less than 10 mils are recommended.
- **E-tile Only**: Use layer assignment to keep the coupling length of the closest TX and RX vias as short as possible. A coupling length including via stubs of less than 56 mils is recommended.
- Use additional ground reference vias for the package edge differential pairs in order to keep ground reference via symmetry for the two signal vias that comprise a differential pair.
Figure 15.  Adding Reference Ground Vias for Package Edge Vias

Add PCB GND Vias for Edge Pins

Legend:
- TX pins
- RX pins
- GND

- Make sure that QSFP-DD connector high-speed signal pin breakouts are on the side that faces toward the FPGA rather than the side that faces the board edge to avoid the long stub caused by the connector pin and PCB pad. For the QSFP-DD connector and PCB pad connection, refer to the following figures.

Figure 16.  QSFP-DD Connector and PCB Connection
Figure 17. QSFP-DD Transition Via Layout

- The zQSFP+ connector has a different connection compared to a QSFP-DD connector as shown in the following figures. Keep the breakouts at the periphery of the zQSFP+ connectors.

Figure 18. zQSFP+ Connector and PCB Connection
Add ground vias on both sides of the connector ground pin and connect them with short, thick ground trace in order to minimize the inductance of the ground connection as shown in the figure below.
1.4.3. P-Tile PCB Design Guidelines

- For PCIe add-in-card designs, the insertion loss from the top of the edge finger to the silicon pad (including the package insertion loss and the silicon loss) for both the receiver and transmitter interconnect must not exceed 8 dB at 8 GHz. Because the P-tile package plus silicon loss is under 3 dB, you may have an add-in-card PCB loss under 5 dB.

- Use an insertion loss of 28 dB including the transmitter and receiver packages as the reference value maximum for end-to-end channel design, but validate the final design through completed channel simulation and measurements.

- Use a trace impedance of 85 Ω for P-tile differential channels.

- Make via stubs as short as possible. Use top-drill, back-drill, buried via, blind via, and micro-via techniques as necessary to shorten the via stubs. Stub lengths of less than 30 mils are recommended.

- Use additional ground reference vias for the package edge differential pairs in order to keep ground reference via symmetry for the two signal vias that comprise a differential pair.

- Place the DC blocking capacitors on TX channels close to the FPGA or connector. Do not place them in the middle of the trace routing.

- Optimize the PCIe slot connector footprint by cutting the ground planes beneath the connector PCB pad, considering the interaction of the connector pin and PCB pad, for less return loss.

- Make sure that the PCIe slot connector high-speed signal pin breakout is at the periphery of the connector as shown below to avoid a long stub caused by the connector pin and PCB pad.
For an add-in card that supports PCIe Gen4 16.0 GT/s, make sure that there are no inner-layer conductors of any kind, including ground or power planes, beneath the edge-fingers (for a distance of 15 mils). You may add inner plane layers beneath any of the edge fingers if they extend no more than 2 mm into the edge finger region from the main routing area of the board and are at a depth of at least 15 mils (0.38 mm) beneath the edge finger copper pads on the surface of the PCB.
Figure 23. Add-in Card Edge-finger Regions with Allowed Inner Layer Plane Volume Indicated

- For add-in-card ground fingers, make sure that the distance between a horizontal line across the top edge ground fingers and a horizontal line across the bottom edge of the ground via pads does not exceed 15 mils. Also join the adjacent edge-fingers at the lowered via location to provide additional improvement in the ground resonance.

Figure 24. Add-in-card Ground Finger Layout

1.5. Document Revision History for the Intel Agilex Device Family High-Speed Serial Interface Signal Integrity Design Guidelines

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<th>Document Version</th>
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