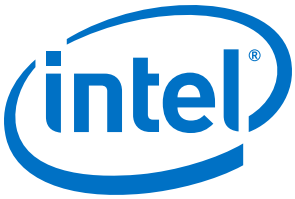

Scalable Switch Intel® FPGA IP for PCI Express* User Guide

Updated for Intel® Quartus® Prime Design Suite: **20.4**

IP Version: **1.0.0**

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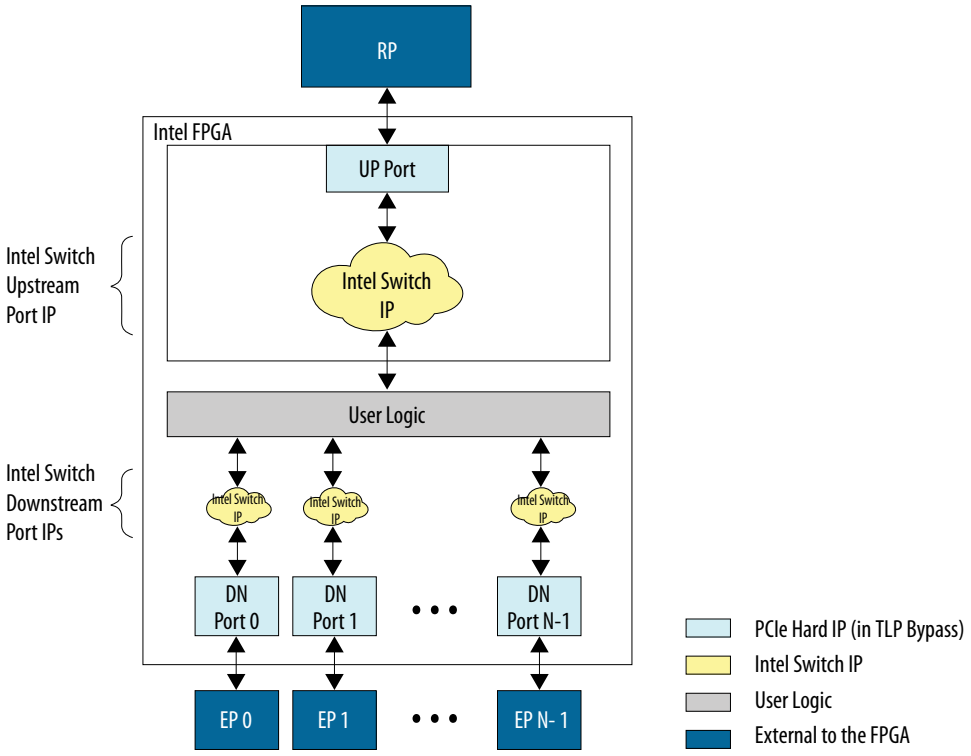
1. Introduction

The Scalable Switch Intel FPGA IP for PCI Express is a fully configurable switch that implements one fully configurable upstream port and connectivity for up to 32 discrete (i.e., external) downstream ports or embedded (i.e., internal) endpoints. This IP supports Hot Plug capability for the downstream ports. You can use the Scalable Switch Intel FPGA IP along with the Intel P-Tile Avalon Streaming IP for PCI Express in TLP Bypass mode to configure the discrete downstream ports or use the Scalable Switch Intel FPGA IP to configure the embedded endpoints allowing the use of fewer PCIe physical links. The Scalable Switch Intel FPGA IP implements the upstream and downstream port configuration spaces and associated logic to route packets between the different ports.

The following figure shows the Scalable Switch Intel FPGA IP with discrete EPs. Note that the Switch can also support embedded EPs.

Figure 1. Scalable Switch Intel FPGA IP for PCI Express with Discrete EPs



To purchase a license for the Scalable Switch Intel FPGA IP for PCI Express, contact your local Intel Regional Sales Office and use the ordering code IP-PCIESCSWTCH.