Intel® Stratix® 10 Configuration via Protocol (CvP) Implementation User Guide

Updated for Intel® Quartus® Prime Design Suite: 18.1
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1. Overview

Configuration via Protocol (CvP) is a configuration scheme supported in Arria® V, Cyclone® V, Stratix® V, Intel® Arria 10, Intel Stratix 10, and Intel Cyclone 10 GX device families. The CvP configuration scheme creates separate images for the periphery and core logic. You can store the periphery image in a local configuration device and the core image in host memory, reducing system costs and increasing the security for the proprietary core image. CvP configures the Intel FPGA fabric through the PCI Express* (PCIe*) link, and is available for Endpoint variants only. This document describes the CvP configuration scheme for Intel Stratix 10 device family.

Related Information

- Arria 10 CvP Initialization and Partial Reconfiguration over PCI Express User Guide
  Provides more information about the CvP implementation in Arria 10 devices.
  Provides more information about the CvP implementation in V-series FPGA devices.
- Additional Clock Requirements for Transceivers, HPS, PCIe, High Bandwidth Memory (HBM2) and SmartVID

1.1. Benefits of Using CvP

The CvP configuration scheme has the following advantages:

- Reduces system costs by reducing the size of the local flash device that stores the configuration data. The smallest EPCQ-L device is large enough for all Intel Stratix 10 periphery images.
- Allows update of the FPGA without reprogramming the flash.
- Enables dynamic core updates without requiring a system power down. CvP allows you to update the FPGA core fabric through the PCIe link without a host reboot or FPGA full chip reinitialization.
- Provides a simpler software model for configuration. A smart host can use the PCIe protocol and the application topology to initialize and update the FPGA core fabric.
- Allows quick update of your design for changing application loads.

1.2. CvP System

A CvP system typically consists of an FPGA, a PCIe host, and a configuration device.
1. **Overview**

1. The FPGA connects to the configuration device using the Active Serial x4 (fast mode) configuration scheme.
2. CvP and other applications use the PCIe Hard IP block (bottom left).
   - Many Intel Stratix 10 FPGAs include more than one Hard IP block for PCI Express. The CvP configuration scheme can only utilize the bottom left PCIe Hard IP block on each device. You must configure this as an Endpoint.
3. You can use other PCIe Hard IP blocks for PCIe applications and cannot use the blocks for CvP.

*Note:* To avoid configuration failure, you must provide a free running and stable reference clock source to PCIe IP core before you start the configuration.

### 1.3. CvP Modes

The CvP configuration scheme supports the following modes:
- CvP Initialization mode
- CvP Update mode

**CvP Initialization Mode**

This mode configures the CvP PCIe core using the peripheral image of the FPGA through the on-board configuration device. Subsequently, configures the core fabric and all GPIOs through PCIe link.
Benefits of using CvP Initialization mode include:
- Satisfying the PCIe wake-up time requirement
- Saving cost by storing the core image in the host memory

**CvP Update Mode**

In the CvP update mode, you reconfigure the entire device except the CvP PCIe core after the device enters the user mode through full chip configuration or CvP initialization. The subsequent core image updates use the PCIe link (the periphery must not change during CvP update).

The CvP update mode uses the same process as root partition reuse in block-based design, which allows you to reuse the device periphery.

Choose this mode if you want to update the core image for any of the following reasons:
- To change core algorithms logic blocks
- To perform standard updates as part of a release process
- To customize core processing for different components that are part of a complex system

*Note:* The CvP update mode is available after the FPGA enters user mode. In user mode, the PCIe link is available for normal PCIe applications as well as to perform an FPGA core image update.

### Table 1. CvP Support for Intel Stratix 10 Device Family

<table>
<thead>
<tr>
<th>PCIe Version</th>
<th>Supported CvP Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gen 1 / Gen 2 / Gen 3</td>
<td>CvP Initialization, CvP Update</td>
</tr>
</tbody>
</table>

**Related Information**

Reusing Root Partitions

### 1.3.1. CvP Limitations and Restrictions

The Intel Stratix 10 CvP implementation has the following limitations and restrictions in the current version of the Intel Quartus® Prime software:
• Only MemWR transactions can be used to write fabric configuration data to the CvP data register. ConfigWR transactions are not supported.

• When you poll the CVP_CREDIT bits from the CvP credit register, you must write the next 4KB of fabric configuration data to the CvP data register within 50 ms of receiving an additional credit. Failure to send the data results in configuration failure.

• The CvP response time is variable and depends on different conditions. The typical delay time is 5 sec and it is safe to wait till 1 min. So the driver should poll status in credit register to decide on driver timeout.

• In CvP initialization and update mode, when FPGA fabric is not programmed, the PCIe features that uses FPGA fabric are not accessible.

• To generate the update image in the CvP update mode, you must use the same version of the Intel Quartus Prime software that you use to generate the base image.

1.3.1.1. CvP Error Recovery

This section describes expected behavior during different error situations.

Table 2. Intel Stratix 10 CvP Error Events and Suggested Recovery Methods

<table>
<thead>
<tr>
<th>Error Events</th>
<th>Suggested Recovery Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>A bitstream is corrupted within the first 168KB of data.</td>
<td>The CVP_CONFIG_ERROR bit in the CvP status register goes high. Go through the Teardown sequence prior to sending another bitstream.</td>
</tr>
<tr>
<td>A bitstream is corrupted after the first 168KB of data.</td>
<td>The CVP_CONFIG_ERROR bit in the CvP status register goes high. To recover the system, you must power-cycle the targeted Intel Stratix 10 device.</td>
</tr>
<tr>
<td>PCIe bus error during CvP</td>
<td>System is unrecoverable and you must power-cycle the system.</td>
</tr>
<tr>
<td>PCIe bus error results in PERST assert.</td>
<td>System is unrecoverable and you must power-cycle the system.</td>
</tr>
<tr>
<td>CvP operation requests to abort</td>
<td>Unsupported. Aborting configuration after requesting CvP operation is not supported. Intel recommends to power-cycle the system.</td>
</tr>
<tr>
<td>A bitstream is provided from an Intel Quartus Prime version other than the one used to generate configuration firmware currently running in the device.</td>
<td>The CVP_CONFIG_ERROR bit in the CvP status register goes high. Go through the Teardown sequence prior to sending another bitstream. Mixing bitstreams from different Quartus versions is not supported.</td>
</tr>
</tbody>
</table>
2. CvP Description

2.1. Configuration Images

In CvP, you split your bitstream into two images: periphery image and core image.

You use the Intel Quartus Prime Pro Edition software to generate the images:

- Periphery image (*.periph.jic) — contains all of the periphery. The entire periphery image is static and cannot be reconfigured.
- Core image (*.core.rbf) — contains all of the core components of the design.

2.2. CvP Modes

2.2.1. CvP Initialization Mode

In this mode, an external configuration device stores the periphery image and it loads into the FPGA through the Active Serial x4 (Fast mode) configuration scheme. The host memory stores the core image and it loads into the FPGA through the PCIe link.

After the periphery image configuration is complete, the CONF_DONE signal goes high and the FPGA starts PCIe link training. When PCIe link training is complete, the PCIe link transitions to L0 state and then allows the host to complete PCIe enumeration of the link. The PCIe host then initiates the core image configuration through the PCIe link. The PCIe REFCLK needs to be running prior to sending the periphery image.

After the core image configuration is complete, the CvP_CONF_DONE pin (if enabled) goes high, indicating the FPGA is fully configured.

2.2.2. CvP Update Mode

CvP update mode is a reconfiguration scheme that allows a host device to deliver an updated bitstream to a target FPGA device after the device enters user mode. In this mode, the FPGA device initializes by loading the full configuration image from the external local configuration device to the FPGA or after CvP initialization.

You can perform CvP update on a device that you originally configure using CvP initialization or any other configuration scheme. CvP initialization is not a prerequisite for performing CvP update.
In user mode, the PCIe links are available for normal PCIe applications. You can use the CvP PCIe link to perform an FPGA core image update. To perform the FPGA core image update, you can create one or more FPGA core images in the Intel Quartus Prime Pro Edition software that have identical connections to the periphery image.

Figure 2. Periphery and Core Image Storage Arrangement for CvP Core Image Update
The periphery image remains the same for different core image updates. If you change the periphery image, you must reprogram the local configuration device with the new periphery image.

2.3. Compression Features

Data Compression
The Intel Quartus Prime Pro Edition software compresses all Intel Stratix 10 bitstreams to reduce the storage requirement and increase bitstream processing speed. The periphery and core images are both compressed.

2.4. Pin Description
The following table lists the CvP pin descriptions and connection guidelines:

Table 3. CvP Pin Descriptions and Connection Guidelines

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Pin Description</th>
<th>Pin Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>CvP_CONFDONE</td>
<td>Output</td>
<td>The CvP_CONFDONE pin is driven low during configuration. When configuration via PCIe is complete, this signal is actively driven high.</td>
<td>If this pin is set as dedicated output, the VCCIO_SDM power supply must meet the input voltage specification of the receiving side. You can assign SDM.IO0, SDM.IO10, SDM.IO11, SDM.IO12, SDM.IO13, ( \text{continued...} )</td>
</tr>
</tbody>
</table>
### Pin Description

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Pin Description</th>
<th>Pin Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>During FPGA configuration in CvP initialization and update mode, you may observe this pin after the CONF_DONE pin goes high to determine if the FPGA is successfully configured.</strong></td>
<td><strong>Output</strong></td>
<td><strong>The INIT_DONE pin goes high indicating the device has entered user mode upon completion of configuration.</strong></td>
<td><strong>Intel recommends using SDM_IO0 pin for implementing the INIT_DONE function, provided that this function is enabled in the Intel Quartus Prime Pro Edition software.</strong></td>
</tr>
<tr>
<td><strong>The CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, CONF_DONE is driven high. In CvP initialization mode, CONF_DONE goes high after the periphery is configured.</strong></td>
<td><strong>Output</strong></td>
<td><strong>Internal recommend using SDM_IO16 pin implementing the CONF_DONE function, provided that this function is enabled in the Intel Quartus Prime Pro Edition software.</strong></td>
<td></td>
</tr>
<tr>
<td><strong>The nPERST pin is only available when you use PCI Express hard IP. When the PCIe hard IP on a side (left or right) is enabled, then nPERST pins on that side cannot be used as general-purpose I/Os (GPIOs). In this case, connect the nPERST pin to the system PCIe nPERST signal to ensure that both ends of the link start link-training at the same time. The nPERST pins on a side are available as GPIOs only when the PCIe hard IP on that side is not enabled. When this pin is low, the transceivers are in reset. When this pin is high, the transceivers are out of reset. When you do not use this pin as the fundamental reset, you can use this pin as a user I/O pin.</strong></td>
<td><strong>Input</strong></td>
<td><strong>Connect this pin as defined in the Intel Quartus Prime Pro Edition software. For more details, refer to Intel Stratix 10 Avalon®-MM/ST Interface for PCIe Solutions User Guide.</strong></td>
<td></td>
</tr>
<tr>
<td><strong>This pin is powered by the VCCIO3V supply. When you connect a 3.0-V supply to VCCIO3V, you must use a diode to clamp the 3.3V LVTTL PCIe input signal to the VCCIO3V power of the device. When VCCIO3V is connected to any voltage other than 3.0V, you must use a level translator to shift down the voltage from 3.3V LVTTL to the corresponding voltage level powering the VCCIO3V pin. Only one nPERST pin is used per PCIe hard IP. The Intel Stratix 10 device components may have all six pins listed even when the specific component might only have 1 or 2 PCIe hard IPs:</strong></td>
<td><strong>Input</strong></td>
<td><strong>Connect this pin as defined in the Intel Quartus Prime Pro Edition software. For more details, refer to Intel Stratix 10 Avalon®-MM/ST Interface for PCIe Solutions User Guide.</strong></td>
<td></td>
</tr>
<tr>
<td><strong>nPERST[L,R][0:2]</strong></td>
<td><strong>Input</strong></td>
<td><strong>This pin is powered by the VCCIO3V supply. When you connect a 3.0-V supply to VCCIO3V, you must use a diode to clamp the 3.3V LVTTL PCIe input signal to the VCCIO3V power of the device. When VCCIO3V is connected to any voltage other than 3.0V, you must use a level translator to shift down the voltage from 3.3V LVTTL to the corresponding voltage level powering the VCCIO3V pin. Only one nPERST pin is used per PCIe hard IP. The Intel Stratix 10 device components may have all six pins listed even when the specific component might only have 1 or 2 PCIe hard IPs:</strong></td>
<td><strong>Connect this pin as defined in the Intel Quartus Prime Pro Edition software. For more details, refer to Intel Stratix 10 Avalon®-MM/ST Interface for PCIe Solutions User Guide.</strong></td>
</tr>
<tr>
<td><strong>This pin is powered by the VCCIO3V supply. When you connect a 3.0-V supply to VCCIO3V, you must use a diode to clamp the 3.3V LVTTL PCIe input signal to the VCCIO3V power of the device. When VCCIO3V is connected to any voltage other than 3.0V, you must use a level translator to shift down the voltage from 3.3V LVTTL to the corresponding voltage level powering the VCCIO3V pin. Only one nPERST pin is used per PCIe hard IP. The Intel Stratix 10 device components may have all six pins listed even when the specific component might only have 1 or 2 PCIe hard IPs:</strong></td>
<td><strong>Input</strong></td>
<td><strong>Connect this pin as defined in the Intel Quartus Prime Pro Edition software. For more details, refer to Intel Stratix 10 Avalon®-MM/ST Interface for PCIe Solutions User Guide.</strong></td>
<td></td>
</tr>
</tbody>
</table>

**continued...**
### Pin Connection Table

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Pin Description</th>
<th>Pin Connection</th>
</tr>
</thead>
<tbody>
<tr>
<td>nPERSTR0</td>
<td></td>
<td>Bottom Right PCIe hard IP (When available)</td>
<td></td>
</tr>
<tr>
<td>nPERSTR1</td>
<td></td>
<td>Middle Right PCIe hard IP (When available)</td>
<td></td>
</tr>
<tr>
<td>nPERSTR2</td>
<td></td>
<td>Top Right PCIe hard IP (When available)</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** For maximum compatibility, always use the bottom left PCIe Hard IP first, as this is the only location that supports Configuration via Protocol (CvP) using the PCIe link.

### Related Information

- [Intel Stratix 10 Avalon-MM Interface for PCI Express Solutions User Guide](#)
- [Intel Stratix 10 Avalon-ST and Single Root I/O Virtualization (SR-IOV) Interface for PCI Express Solutions User Guide](#)
- [Intel Stratix 10 Device Family Pin Connection Guidelines](#)
3. CvP Topologies

CvP supports two types of topologies that allow you to configure single or multiple FPGAs.

3.1. Single Endpoint

Use the single endpoint topology to configure a single FPGA. In this topology, the PCIe link connects one PCIe endpoint in the FPGA device to one PCIe root port in the host.

**Figure 3. Single Endpoint Topology**

3.2. Multiple Endpoints

Use the multiple endpoints topology to configure multiple FPGAs through a PCIe switch. This topology provides you with the flexibility to select the device to be configured or update through the PCIe link. You can connect any number of FPGAs to the host in this topology.

The PCIe switch controls the core image configuration through the PCIe link to the targeted PCIe endpoint in the FPGA. You must ensure that the root port can respond to the PCIe switch and direct the configuration transaction to the designated endpoint based on the bus/device/function address of the endpoint specified by the PCIe switch.
Figure 4. Multiple Endpoints Topology
4. Design Considerations

4.1. Designing CvP for an Open System

Follow these guidelines when designing an open CvP system where you do not have complete control of both ends of the PCIe link.

4.1.1. FPGA Power Supplies Ramp Time Requirement

For an open system, you must ensure that your design adheres to the FPGA power supplies ramp-up time requirement.

The power-on reset (POR) circuitry keeps the FPGA in the reset state until the power supply outputs are in the recommended operating range. A POR event occurs from when you power up the FPGA until the power supplies reach the recommended operating range within the maximum power supply ramp time, $t_{\text{RAMP}}$. If $t_{\text{RAMP}}$ is not met, the device I/O pins and programming registers remain tri-stated, during which device configuration could fail.

To meet the PCIe link up time for CvP, the total $t_{\text{RAMP}}$ must be less than 10 ms, from the first power supply ramp-up to the last power supply ramp-up. You must select ASx4 fast mode for MSEL settings to make sure the shortest POR delay.

Figure 5. Power Supplies Ramp-Up Time and POR

![Power Supplies Ramp-Up Time and POR](image-url)
4. Design Considerations

4.1.2. PCIe Wake-Up Time Requirement

For an open system, you must ensure that the PCIe link meets the PCIe wake-up time requirement as defined in the *PCI Express CARD Electromechanical Specification*. The transition from power-on to the link active (L0) state for the PCIe wake-up timing specification must be within 200 ms. The timing from FPGA power-up until the Hard IP for PCI Express IP Core in the FPGA is ready for link training must be within 120 ms.

4.1.2.1. For CvP Initialization Mode

To meet the 120 ms wake-up time requirement for the PCIe Hard IP in CvP initialization mode, you need to use periphery image because the configuration time for periphery image is significantly less than the full FPGA configuration time. You must use the Active Serial x4 (fast mode) configuration scheme for the periphery image configuration.

To ensure successful configuration, all POR-monitored power supplies must ramp up monotonically to the operating range within the 10 ms ramp-up time. The PERST# signal indicates when the FPGA power supplies are within their specified voltage tolerances and the REFCLK is stable(1). The embedded hard reset controller triggers after the internal status signal indicates that the periphery image has been loaded. This reset does not trigger off of PERST#. For CvP Initialization mode, the PCIe link supports the FPGA core image configuration and subsequent PCIe applications in user mode.

**Note:**

For Gen 2/Gen 3 capable Endpoints, after loading the core bitstream (core.rbf), Intel recommends to verify that the link has been trained to the expected Gen 2/Gen3 rate. If the link is not operating at Gen 2/Gen3, software can trigger the Endpoint to retrain.

---

(1) REFCLK must be stable 80 ms after the power supplies are stable in order to achieve the 145 ms link training complete time
4.1.2.2. For CvP Update Mode

Before you perform CvP update mode, the device must be in user mode.

Note: For Gen 2/Gen 3 capable Endpoints, in user mode, Intel recommends to verify that the link has been trains to the expected Gen 2/Gen 3 rate. If the link is not operating at Gen 2/Gen3, software can trigger the Endpoint to retrain.

4.2. Designing CvP for a Closed System

While designing CvP for a closed system where you control both ends of the PCIe link, estimate the periphery configuration time for CvP Initialization mode or full FPGA configuration time for CvP update mode. You must ensure that the estimated
configuration time is within the time allowed by the PCIe host. Your driver can poll the USERMODE bit of the CvP Status Register to determine if the FPGA enters the user mode.

**Related Information**

*CvP Status Register* on page 21
5. CvP Driver and Registers

5.1. CvP Driver Support

You can develop your own custom CvP driver for Linux using the sample Linux driver source code provided by Intel.

Note: The Linux driver provided by Intel is not a production driver. You must adapt this driver to your design's strategy.

Related Information
Download the OpenSource Linux CvP Driver

5.2. CvP Driver Flow

The CvP driver flow assumes that the FPGA is powered up and the SDM control block has already configured the FPGA with the periphery image, which is indicated by the CVP_EN bit in the CvP status register.
5.3. VSEC Registers for CvP

The Vendor Specific Extended Capability (VSEC) registers occupy byte offsets 0xB80 to 0xBC0 in the PCIe Configuration Space. The PCIe host uses these registers to communicate with the FPGA control block. The following table shows the VSEC register map. Subsequent tables provide the fields and descriptions of each register.

Table 5. VSEC Registers for CvP

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Register Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xB80</td>
<td>Vendor Specific Capability Header</td>
</tr>
<tr>
<td>0xB84</td>
<td>Vendor Specific Header</td>
</tr>
<tr>
<td>0xB88</td>
<td>Intel Marker</td>
</tr>
</tbody>
</table>
5.3.1. Vendor Specific Capability Header Register

Table 6. Vendor Specific Capability Header Register (Byte Offset: 0xB80)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>PCI Express Extended Capability ID</td>
<td>0x000B</td>
<td>RO</td>
<td>PCIe specification defined value for VSEC Capability ID.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>Version</td>
<td>0x1</td>
<td>RO</td>
<td>PCIe specification defined value for VSEC version.</td>
</tr>
<tr>
<td>[31:20]</td>
<td>Next Capability Offset</td>
<td>Variable</td>
<td>RO</td>
<td>Starting address of the next Capability Structure implemented, if any.</td>
</tr>
</tbody>
</table>

5.3.2. Vendor Specific Header Register

Table 7. Vendor Specific Header Register (Byte Offset: 0xB84)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>VSEC ID</td>
<td>0x1172</td>
<td>RO</td>
<td>A user configurable VSEC ID.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>VSEC Revision</td>
<td>0</td>
<td>RO</td>
<td>A user configurable VSEC revision.</td>
</tr>
<tr>
<td>[31:20]</td>
<td>VSEC Length</td>
<td>0x05C</td>
<td>RO</td>
<td>Total length of this structure in bytes.</td>
</tr>
</tbody>
</table>

5.3.3. Intel Marker Register

Table 8. Intel Marker Register (Byte Offset: 0xB88)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:0]</td>
<td>Intel Marker</td>
<td>0x41721172</td>
<td>RO</td>
<td>An additional marker.</td>
</tr>
</tbody>
</table>

(2) This register is no longer functional in Intel Stratix 10 devices.
5.3.4. User Configurable Device/Board ID Register

Table 9. User Configurable Device/Board ID Register (Byte Offset: 0xB9C)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>User Configurable Device/Board ID</td>
<td>0x00</td>
<td>RO</td>
<td>Helps user to select the correct programming file.</td>
</tr>
</tbody>
</table>

5.3.5. CvP Status Register

Table 10. CvP Status Register (Byte Offset: 0xB9E)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[10]</td>
<td>CVP_CONFIG_SUCCESS</td>
<td>Variable</td>
<td>RO</td>
<td>Status bit set by the device to indicate that the core image configuration was successful.</td>
</tr>
<tr>
<td>[8]</td>
<td>PLD_CLK_IN_USE</td>
<td>Variable</td>
<td>RO</td>
<td>From clock switch module to fabric. You can use this bit for debug.</td>
</tr>
<tr>
<td>[7]</td>
<td>CVP_CONFIG_DONE</td>
<td>Variable</td>
<td>RO</td>
<td>Indicates that the device has completed the device configuration via CvP and there were no errors.</td>
</tr>
<tr>
<td>[5]</td>
<td>USERMODE</td>
<td>Variable</td>
<td>RO</td>
<td>Indicates if the configurable FPGA fabric is in user mode.</td>
</tr>
<tr>
<td>[4]</td>
<td>CVP_EN</td>
<td>Variable</td>
<td>RO</td>
<td>Indicates if the device has enabled CvP mode.</td>
</tr>
<tr>
<td>[3]</td>
<td>CVP_CONFIG_ERROR</td>
<td>Variable</td>
<td>RO</td>
<td>Reflects the value of this signal from the device, checked by software to determine if there was an error during configuration.</td>
</tr>
<tr>
<td>[2]</td>
<td>CVP_CONFIG_READY</td>
<td>0x0</td>
<td>RO</td>
<td>Reflects the value of this signal from the device, checked by software during programming algorithm to determine the device is ready for configuration.</td>
</tr>
<tr>
<td>[1:0]</td>
<td>—</td>
<td>Variable</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

5.3.6. CvP Mode Control Register

Table 11. CvP Mode Control Register (Byte Offset: 0xBA0)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:3]</td>
<td>—</td>
<td>0x0000</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[2]</td>
<td>—</td>
<td>0x0000</td>
<td>RW</td>
<td>Reserved&lt;sup&gt;(3)&lt;/sup&gt;.</td>
</tr>
<tr>
<td>[1]</td>
<td>PLD_DISABLE</td>
<td>1’b0</td>
<td>RW/RO</td>
<td>Enables/disables the PLD interface. This allows Host driver to switch the PLD interface out before USER MODE deasserts,</td>
</tr>
</tbody>
</table>

<sup>(3)</sup> Intel recommends to set the reserved bit to 0 for write operation. For read operations, the PCIe IP always generates 0 as the output.
and to switch the PLD interface back in only after USER MODE has been asserted. This helps to prevent any glitches or race conditions during the USER MODE switching.

- 1: Disable the application layer interface.
- 0: Enable the application layer interface.

Only change the value of this signal when there has been no other TLP's to or from the HIP for 10 us. There should be no TLP's issued to the HIP for 10 us after this value changes. When entering CVP, this bit should be set before CVP_MODE is set. When exiting CVP, it should be cleared after CVP_MODE is cleared. This ensures that there is no PLD switching during CVP. This field is RW when cvp_en=1, and RO when cvp_en=0.

### Table 12. CVP Data Register (Byte Offsets: 0xBA4 - 0xBA8)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:0]</td>
<td>CVP_DATA</td>
<td>0x00000000</td>
<td>RW</td>
<td>Write the configuration data to this register. The data is transferred to the SDM to configure the device. Software must ensure that all bytes in the memory write dword are enabled. You can access this register using configuration writes. Alternatively, when in CVP mode, this register can also be written by a memory write to any address defined by a memory space BAR for this device. Using memory writes are higher throughput than configuration writes.</td>
</tr>
</tbody>
</table>

### 5.3.8. CVP Programming Control Register

Table 13. CVP Programming Control Register (Byte Offset: 0x22C)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:2]</td>
<td>—</td>
<td>0x0000</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[1]</td>
<td>START_XFER</td>
<td>1'b0</td>
<td>RW</td>
<td>Sets the CVP output to the FPGA control block indicating the start of a transfer.</td>
</tr>
<tr>
<td>[0]</td>
<td>CVP_CONFIG</td>
<td>1'b0</td>
<td>RW</td>
<td>When set to 1, the FPGA control block begins a transfer via CVP.</td>
</tr>
</tbody>
</table>
5.3.9. CvP Credit Register

The credit registers slow down the transmission of the CvP data to handle back pressure when there is no buffer space available within the configuration system. The crediting mechanism handles the back pressure from the configuration system. The total credits register increments each time an additional 4k buffer is available.

Table 14. CvP Credits Register (Byte Offset: 0xBC8)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Reset Value</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:16]</td>
<td>0x00</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>0x00</td>
<td>RO</td>
<td>Least significant 8 bits of the total number of 4k credits granted.</td>
</tr>
<tr>
<td>[7:0]</td>
<td>0x00</td>
<td>RO</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
6. Understanding the Design Steps for CvP Initialization and Update Mode in Intel Stratix 10

6.1. Implementation of CvP Initialization Mode

CvP Initialization mode splits the bitstream into periphery and core images. The periphery image is stored in a local flash device on the PCB. The core image is stored in host memory. You must download the core image to the FPGA using the PCI Express link.

You must specify CvP Initialization mode in the Intel Quartus Prime Pro Edition software by selecting the CvP Settings Initialization and Update and you must also instantiate the Avalon-ST Intel Stratix 10 Hard IP for PCI Express (4).

---

(4) CvP also supports Avalon-MM.
Figure 8. Example Implementation Flow for CvP Initialization

The CvP Initialization demonstration (based on the Intel Stratix 10 FPGA Development Kit) walkthrough includes the following steps:

- Generating the Synthesis HDL files for Avalon-ST Intel Stratix 10 Hard IP for PCI Express on page 26
- Setting up the CvP Parameters in Device and Pin Options on page 27
- Compiling the Design on page 28
- Converting the SOF File on page 28
- Bringing up the Hardware on page 30
6.1.1. Generating the Synthesis HDL files for Avalon-ST Intel Stratix 10 Hard IP for PCI Express

Follow these steps to generate the synthesis HDL files with CvP enabled:

1. Open the Intel Quartus Prime Pro Edition software.
2. On the Tools menu, click **Platform Designer**. The **Open System** window appears.
3. For **System**, click + and specify a **File Name** to create a new platform designer system. Click **Create**.
4. On the **System Contents** tab, delete the `clock_in` and `reset_in` components that appear by default.
5. In the IP Catalog locate and double-click **Avalon-ST Intel Stratix 10 Hard IP for PCI Express**. The new window appears.
6. On the **IP Settings** tab, specify the parameters and options for your design variation.
7. On the **Example Designs** tab, select the **Simulation** option to generate the testbench, and select the **Synthesis** option to generate the hardware design example.
8. For **Generated file format**, only **Verilog** is available.
9. For **Target Development Kit**, select the board of your choice.
10. Click the **Generate Example Design** button. The **Select Example Design Directory** dialog box appears. Click **OK**. The software generates Intel Quartus Prime project files for PCI Express reference design. Click **Close** when generation completes. An example design `pcie_s10_hip_ast_0_example_design` is created in your project directory.
11. Click **Finish**. Close your current project and open the generated PCI Express example design (`pcie_example_design.qpf`).
12. Complete your CvP design by adding any desired top-level design and any other required modules. Pin assignments already being assigned properly based on the target development kit that user specified earlier.

Alternatively, you can download the complete Intel Stratix 10 CvP Initialization reference design from the link below.

**Note:** Reference design for CvP update is not available in the current version of the Intel Quartus Prime software.

**Related Information**
- Intel Stratix 10 Avalon-MM Interface for PCI Express Solutions User Guide
- Intel Stratix 10 CvP Initialization Reference Design for 17.1 Quartus Version
- Download the OpenSource Linux CvP Driver
6.1.2. Setting up the CvP Parameters in Device and Pin Options

Follow these steps to specify CvP parameters:

1. On the Intel Quartus Prime Assignment menu, select **Device**, and then click **Device and Pin Options**.
2. Under **Category**, select **Configuration** and then enable the following options:
   a. For **Configuration scheme**, select **Active Serial x4(can use Configuration Device)**.
   b. For **Use configuration device**, select **EPCQL1024**.
   c. For **Configuration pin**, click **Configuration Pin Options** and then turn on **USE CONF_DONE output** and **USE CVP_CONF_DONE output**. Click **OK**.

Figure 9. CvP Parameters in Configuration Tab

3. Under **Category**, select **CvP Settings** to specify CvP settings. For **Configuration via Protocol**, select **Initialization and update** option. Click **OK**.
4. Click OK.

6.1.3. Compiling the Design

To compile the design, on the Processing menu, select Start Compilation to create the .sof file.

6.1.4. Converting the SOF File

Follow these steps to convert your .sof file into separate images for the periphery and core logic.

1. After the .sof file is generated, under File menu, select Convert Programming Files. The new window appears.
2. Under Output programming file section, specify the following parameters:

Table 15. Parameters: Output Programming File Tab

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming file type</td>
<td>JTAG Indirect Configuration File (.jic)</td>
</tr>
<tr>
<td>Configuration device</td>
<td>EPCQL1024</td>
</tr>
<tr>
<td>Mode</td>
<td>Active Serial x4</td>
</tr>
</tbody>
</table>

continued...
3. Under **Input files to convert**, specify the following parameters:

<table>
<thead>
<tr>
<th>Table 16. Parameters: Input Files to Convert Tab</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Parameter</strong></td>
</tr>
<tr>
<td>Flash Loader</td>
</tr>
<tr>
<td>SOF Data</td>
</tr>
</tbody>
</table>

**Note:** Make sure to turn on the Create CvP files option. If you do not select this option, the Intel Quartus Prime software does not create separate files for the periphery and core images.

4. Click **Generate** to create *.periph.jic and *.core.rbf files.
6.1.5. Bringing up the Hardware

Before testing the design in hardware, you must install the CvP driver in your DUT system. You can also install RW Utilities or other system verification tools to monitor the link status of the Endpoint and to observe traffic on the link. You can download these utilities for free from many web sites.

Note: You can develop your own custom CvP driver for Linux using the sample Linux driver source code provided by Intel.

The test setup includes the following components:
1. Intel Stratix 10 FPGA Development Kit
2. Intel FPGA Download Cable
3. A DUT PC with PCI Express slot to plug in the FPGA Development Kit
4. A PC running the Intel Quartus Prime software to program the periphery image, .sof or .pof file.

Related Information
Intel Stratix 10 GX FPGA Development Kit User Guide

6.1.5.1. Installing Open Source CvP Driver in Linux Systems

1. Download the open source Linux CvP driver from the CvP Driver.
2. Navigate to the driver directory.
3. Unzip the drive by typing the following command:
   \[\text{tar -zxvf <driver>.gz}\]
4. Run the installation by typing the following command:
   \[\text{sudo make} \]
   \[\text{sudo make install}\]
5. Once the installation completed successfully, it generates the altera_cvp file under directory /dev/altera_cvp.

6.1.5.2. Modifying MSEL/DIP switch on Intel Stratix 10 FPGA Development Kit

The MSEL/DIP switch labeled SW1 at the front part of the Intel Stratix 10 FPGA Development Kit. Select Active Serial x4 (Fast mode) for CvP operation.

Table 17. MSEL Pin Settings for Each Configuration Scheme of Intel Stratix 10 Devices

<table>
<thead>
<tr>
<th>Configuration Scheme</th>
<th>MSEL[2:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS (Fast mode - for CvP)(^{(5)})</td>
<td>001</td>
</tr>
</tbody>
</table>

\(^{(5)}\) To support AS fast mode, the V\(_{CCIO\_SDM}\) of Intel Stratix 10 device must be fully ramped-up within 10ms to the recommended operating conditions. The delay between the device exiting POR and the SDM Boot-up is shorter for the fast mode compared to the normal mode. Therefore, AS fast mode is the recommended configuration scheme for CvP because the device can conform to the PCIe 100ms power-up-to-active time requirement.
Related Information
Intel Stratix 10 Device Family Pin Connection Guidelines

6.1.5.3. Programming CvP Images

You must program the periphery image (.periph.jic) into your AS configuration device and then download the core image (.core.rbf) using the PCIe Link. You can use Active Serial x4 (Fast mode) to load .periph.jic into your selected CvP initialization enabled Intel Stratix 10 device.

After loading the periphery image, the Intel Stratix 10 is triggered to reconfigure from AS to load it. The link should reach the expected data rate and link width. You can confirm the PCIe link status using the RW Utilities. Follow these steps to program and test the CvP functionality:

1. Plug the Intel Stratix 10 FPGA Development Kit into the PCI Express slot of the DUT PC and power it ON. It is recommended to use the ATX power supply that the development kit includes.
2. Open the Intel Quartus Prime Tools menu and select Programmer.
3. Click Auto Detect to verify that the Intel FPGA Download Cable recognizes the Intel Stratix 10 FPGA.
4. Follow these steps to program the periphery image:
   a. Select Stratix 10 device, and then right click None under File column and select Change File.
   b. Navigate to .periph.jic file and click Open.
   c. Under Program/Configure column, select the respective devices. For example, 1SG280LU3S1 and EPCQL1024.
   d. Click Start to program the periphery image into EPCQL1024 flash.

Figure 12. Illustrating the Specified Options to the Program Periphery Image

5. After the .periph.jic is programmed, the FPGA must be powered cycle to allow the new peripheral image to load from the on-board flash into the FPGA. To force the DUT PC to re-enumerate the link with the new image, power cycle the DUT PC and the Intel Stratix 10 FPGA Development Kit.
6. You can use RW Utilities or another system software driver to verify the link status. You can also confirm expected link speed and width.

7. Follow these steps to program the core image:
   a. Copy the `.core.rbf` file to your working directory.
   b. Open a console in Linux. Change the directory to the same mentioned above where the file is copied.
   c. Program the core image by typing the following command: `cp *.core.rbf /dev/altera_cvp`

8. You can see your core image running on the Intel Stratix 10 FPGA Development Kit. Alternatively, print out the kernel message using the `dmesg` to ensure the CvP is completed successfully.

### 6.2. Implementation of CvP Update Mode

CvP update mode is a reconfiguration scheme to deliver an updated bitstream to a target device after the device enters user mode.

You must specify this mode in the Intel Quartus Prime Pro Edition software by selecting the CvP Settings Initialization and Update. The following figure provides the high-level steps for CvP update mode.
Figure 13. Example Implementation Flow for CvP Update

The CvP update mode demonstration walkthrough includes the following steps:
6. Understanding the Design Steps for CvP Initialization and Update Mode in Intel Stratix 10

- Instantiating the PCIe Hard IP on page 34
- Setting Up the CvP Parameters on page 34
- Setting up the Base Revision on page 34
- Setting up and Compile the Updated Revision on page 37
- Converting the SOF file of the Updated Revision on page 39
- Programming the FPGA using the Base Revision Image on page 40

6.2.1. Instantiating the PCIe Hard IP

Follow the steps from Generating the Synthesis HDL files for Avalon-ST Intel Stratix 10 Hard IP for PCI Express on page 26 section to instantiate PCIe Hard IP and generate the synthesis HDL files with CvP enabled.

6.2.2. Setting Up the CvP Parameters

Specify the CvP parameters in Device and Pin options using the instructions in the Setting up the CvP Parameters in Device and Pin Options on page 27 section.

6.2.3. Setting up the Base Revision

To set up the base revision, you must create a periphery reuse core partition, define a logic lock region and then compile the base revision. After compilation, you need to export the root partition.

Related Information
Reusing Root Partitions

6.2.3.1. Creating a Reserved Core Partition

The following instructions are for creating a reserved core partition from the base revision:

1. To elaborate the hierarchy of the design, click Processing ➤ Start ➤ Start Analysis & Synthesis.

2. Right-click an instance in the Project Navigator and click Design Partition ➤ Set as Design Partition. A design partition icon appears next to each instance you assign.
3. When defining the partition, select **Reserved Core** for the partition **Type**. Ensure that all other partition options are set to default values.

   This setting corresponds to the following assignment in the `.qsf`:

   ```qsf
   set_instance_assignment -name RESERVED CORE ON -to <partition hierarchical path>
   ```

4. To export the finalized static region from this base revision compile and to use in subsequent CvP update revision compile, in the **Post Final Export File** cell, double-click the entry for **root_partition** and type **root_partition.qdb**.

6.2.3.2. Defining a Logic Lock Region

   To reserve core resources in an updated revision for the reserved core partition, you must define a fixed size and location, core-only, reserved Logic Lock region. The updated revision uses this area for core development, and the area can contain only core logic. Ensure that the reserved placement region is large enough to contain all core logic in the updated revision.
Follow these steps to define a Logic Lock region for core base revision:

1. Right-click the design instance in the Project Navigator and click Logic Lock Region ➤ Create New Logic Lock Region. The region appears in the Logic Lock Regions Window. You can also verify the region in the Chip Planner (Locate Node ➤ Locate in Chip Planner).

Figure 16. Creating Logic Lock Region from Project Navigator

2. In the Logic Lock Regions window, specify the Width, Height and the placement region co-ordinates in the Origin column.
3. Enable the Reserved and Core-Only options.
4. For Size/State, select Fixed/Locked.
5. Double-click the Routing Region cell. The Logic Lock Routing Region Settings dialog box appears.

Figure 17. Logic Lock Regions Window

6. Specify Fixed with expansion with Expansion Length of 1 for the Routing Type.
7. Click OK.
8. Click File ➤ Save Project.
6.2.3.3. Compiling and Exporting the Root Partition

To compile the base revision and export the root partition:
1. To compile the base revision, click **Processing ➤ Start Compilation**
2. The base revision provides the exported .qdb file and any optional .sdc files for the periphery reuse core to the new revision.

6.2.4. Setting up and Compile the Updated Revision

In this section, you create a new revision that serves as the updated revision of the base design. The new revision reuses the root partition that is exported from the base revision. However, it uses a new core logic.

Perform the following steps to create and compile an updated revision:
1. To create a new revision, Click **Project ➤ Revisions**.
2. The new **Revision** window appears. To create a new revision, double-click **<<new revision>>**.
3. Specify the revision name in **Revision name** field.
4. For the **Revision Type**, select **same as Base revision**.
5. Enable **This project uses a Partition Database (.qdb) file for the root partition**. This setting is also present in the Design Partitions window.
6. Use entity rebinding assignment in design partitions window to change the logic associated with the reserved core partition.

For example, First you use green_led as the logic within reserved core partition. Now you change the green_led logic to red_led via entity rebinding, which replaces the green_led instance with a red_led instance.

Figure 19. Design Partitions Window

Ensure that your Intel Quartus Prime project includes source files associated with updated Reserved Core partition logic in Intel Quartus Prime.

7. To run compilation, click Processing ➤ Start Compilation.
6.2.5. Converting the SOF file of the Updated Revision

Follow these steps to convert your .sof file of the updated revision into periphery and core images for CvP update mode.

1. On the File menu, select Convert Programming Files.
2. Under Output programming file section, specify the following parameters:

Table 18. Parameters: Output Programming File Tab

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programming file type</td>
<td>JTAG Indirect Configuration File (.jic)</td>
</tr>
<tr>
<td>Configuration device</td>
<td>EPCQL1024</td>
</tr>
<tr>
<td>Mode</td>
<td>Active Serial x4</td>
</tr>
<tr>
<td>File name</td>
<td>cvp_init.jic</td>
</tr>
<tr>
<td>Create Memory Map File (Generate output_file.map)</td>
<td>Turn this option on.</td>
</tr>
<tr>
<td>Create CvP files (Generate cvp_init.periph.jic and cvp_init.core.rbf)</td>
<td>Turn this option on. This option is only available when you specify the SOF Data file under Input files to convert.</td>
</tr>
</tbody>
</table>

Note: Make sure to turn on the Create CvP files option. If you do not select this option, the Intel Quartus Prime software does not create separate files for the periphery and core images.

3. Under Input files to convert, specify the following parameters:

Table 19. Parameters: Input Files to Convert Tab

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash Loader</td>
<td>First click Flash Loader. Click Add Device, under Device family, select Stratix 10 and then for Device name select 1SG280LU3F50I1VGS1. Click OK.</td>
</tr>
<tr>
<td>SOF Data</td>
<td>First click SOF Data. Click Add File and then select *.sof.</td>
</tr>
</tbody>
</table>
4. Click **Generate** to create *.periph.jic and *.core.rbf files.

### 6.2.6. Programming the FPGA using the Base Revision Image

For CvP update mode, you must program the FPGA using the base revision image through any configuration scheme. After programming completes the FPGA enters user mode.

The following steps illustrate CvP update on the base revision image programmed through JTAG mode.

**Before you begin:**

- Connect the Intel FPGA Download Cable II between your PC USB port and the USB port on the Intel Stratix 10 FPGA Development Kit.
- You must install the `altera_cvp` driver in your DUT PC system. You can download the open source Linux CvP driver from the [CvP Driver](#).
  
  *Note:* The Linux driver provided by Intel is not a production driver.
- Set the MSEL switches of the Intel Stratix 10 FPGA Development Kit to JTAG mode for CvP update operation.
Follow these steps to program and test CvP update functionality:

1. Plug the Intel Stratix 10 FPGA Development Kit into the PCI Express slot of the DUT PC and power it ON. It is recommended to use the ATX power supply that the development kit includes.

2. Open the Intel Quartus Prime Pro Edition software and click **Tools ➤ Programmer**.

3. Click **Auto Detect** to verify that the Intel FPGA Download Cable II recognizes the Intel Stratix 10 FPGA.

4. Follow these steps to program the base revision .sof file:
   a. Select **Stratix 10** device, and then right click **None** under **File** column and select **Change File**.
   b. Navigate to * .sof file generated from the base revision and click **Open**.
   c. Under **Program/Configure** column, select the device. For example, **1SG280LU3S1**.
   d. Click **Start**. The progress bar reaches 100% when device configuration is complete. The device is fully configured and in operation.
   e. After the .sof file is programmed, perform the soft reset on the PC.
   f. Once PC has completed soft rebooting, type the following command in a terminal window to make sure the PCIe link is up and running: **lspci -v vvd1172**.
   g. At this time, the FPGA enters into user mode with a functional PCIe link to the DUT PC and you are ready to use the **altera_cvp** driver to perform the CvP update.
   h. Follow these steps to program the core.rbf:
   i. Type **lspci -v vvd1172** in a terminal window to make sure that you have an active PCIe link.
   j. Program the core.rbf generated from the updated revision by typing the following command: **cp <new core.rbf file> /dev/altera_cvp**.

If an IP core version is not listed, the user guide for the previous IP core version applies.

<table>
<thead>
<tr>
<th>Quartus Version</th>
<th>User Guide</th>
</tr>
</thead>
<tbody>
<tr>
<td>18.0</td>
<td>Intel Stratix 10 Configuration via Protocol (CvP) Implementation User Guide</td>
</tr>
<tr>
<td>17.1</td>
<td>Intel Stratix 10 Configuration via Protocol (CvP) Implementation User Guide</td>
</tr>
</tbody>
</table>
# 8. Document Revision History for Intel Stratix 10

## Configuration via Protocol Implementation User Guide

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019.06.20</td>
<td>18.1</td>
<td>Clarified how to program the FPGA for CvP update mode.</td>
</tr>
</tbody>
</table>
| 2019.01.17       | 18.1                        | - Modified the following in Setting up the Base Revision section:  
  - Figure: Creating Design Partition from Project Navigator  
  - Figure: Design Partitions Window  
  - Figure: Creating Logic Lock Region from Project Navigator  
  - Added Figure: Design Partitions Window in section Setting up and Compile the Updated Revision section. |
| 2018.11.29       | 18.1                        | Modified the following diagrams:  
  - Figure: Single Endpoint Topology  
  - Figure: Multiple Endpoints Topology |
| 2018.09.24       | 18.1                        | - CvP update mode is now supported in the current version of the Intel Quartus Prime Pro Edition software.  
  - Added new section Implementation of CvP Update Mode.  
  - Modified diagrams:  
    - Figure: Periphery and Core Image Storage Arrangement for CvP Core Image Update  
    - Figure: Single Endpoint Topology  
    - Figure: Multiple Endpoints Topology  
  - Updated Figure: CvP Driver Flow in section CvP Driver Flow.  
  - CVP_DATA2 register is no longer functional in Intel Stratix 10 devices.  
  - Added new sections:  
    - CvP Limitations and Restrictions  
    - CvP Error Recovery  
    - Intel Stratix 10 Configuration via Protocol (CvP) Implementation User Guide Archives |
| 2018.07.17       | 18.0                        | - Added a note in CvP Modes section to clarify CvP update mode support in the current version of the Intel Quartus Prime Pro Edition software.  
  - Modified Figure: PCIe Timing Sequence in CvP Initialization Mode diagram. |
| 2018.06.18       | 18.0                        | - Corrected the periphery image and core image definitions in Configuration Images section.  
  - Added Figure: PCIe Timing Sequence in CvP Initialization Mode diagram and Table: Power-up Sequence Timing in CvP Initialization Mode information for CvP initialization.  
  - Modified Figure: Single Endpoint Topology and Figure: Multiple Endpoint Topology in CvP Topologies chapter.  
  - Added a note to clarify the Linux driver support provided by Intel.  
  - Updated the Figure: CvP Driver Flow.  
  - Corrected the VSEC registers for CvP in VSEC Registers for CvP section.  
  - Minor updates in Implementation of CvP Initialization Mode section. |
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tr>
<td>December 2017</td>
<td>2017.12.18</td>
<td>Initial release.</td>
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