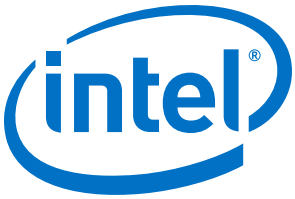

Random Number Generator IP Core User Guide

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1. Random Number Generator IP Core User Guide

The random number generator IP core allows you to define the random sequence seed manually.The uniformly distributed integer number generator is a random sequence of 32 bit data, which can be interpreted as signed or unsigned integer.

The IP core offers two algorithms to generate the Gaussian sequence: central-limit theorem (CLT) components and Box-Muller transform. The CLT components make use of a mixture of Irwin-hall distribution (the distribution of sum of uniform distribution) to approximate the Gaussian distribution. The classic Box-Muller transform is for reference, as it is more costly to implement on hardware and has only average random sequence quality.

1.1. Random Number Generator IP Core Features

- Uniformly distributed integer number
- Uniformly distributed floating point number
- Floating point number under Gaussian distribution

1.2. Random Number Generator Device Family Support

Intel offers the following device support levels for Intel FPGA IP cores:

- Advance support—the IP is available for simulation and compilation for this device family. FPGA programming file (`.pof`) support is not available for Quartus Prime Pro Stratix 10 Edition Beta software and as such IP timing closure cannot be guaranteed. Timing models include initial engineering estimates of delays based on early post-layout information. The timing models are subject to change as silicon testing improves the correlation between the actual silicon and the timing models. You can use this IP core for system architecture and resource utilization studies, simulation, pinout, system latency assessments, basic timing assessments (pipeline budgeting), and I/O transfer strategy (data-path width, burst depth, I/O standards tradeoffs).
- Preliminary support—Intel verifies the IP with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. You can use it in production designs with caution.
- Final support—Intel verifies the IP with final timing models for this device family. The IP core meets all functional and timing requirements for the device family. You can use it in production designs.

Table 1. DSP IP Device Family Support

Device Family	Support
Arria® II GX	Final
Arria II GZ	Final
Arria V	Final
Intel® Arria 10	Final
Intel Cyclone® 10	Final
Stratix® IV GT	Final
Stratix IV GX/E	Final
Stratix V	Final
Intel Stratix 10	Final
Other device families	No support

1.3. Random Number Generator Performance and Resource Usage

Table 2. Performance and Resource Usage

Targeting 10AX115S3F45E2SGE3 Arria 10 device.

Parameters	ALMs	Memory Bits	RAM Blocks	DSP Blocks	f_{MAX} (MHz)
Uniform distribution integer	113	0	0	0	693
Uniform distribution float	308	0	0	0	484
Normal distribution with central limit transform (CLT) components	3,469	4096	1	6	405
Normal distribution with Box-Muller	5,511	452,952	29	40	298

1.4. Random Number Generator IP Core Signals

Table 3. Parameters

Name	Direction	Description
clock	Input	Clock.
resetn	Input	Reset.
Call signals		
start	Input	Enable.
rand_num signals		
rand_num_data	Output	Data.
rand_num_ready	Input	Stalls the IP core for backpressure.
rand_num_valid	Output	Indicates valid output.

1.5. Random Number Generator IP Core Parameters

Set the parameters to create an IP core suitable for your design.

Table 4. Parameters

Name	Values	Description
Type of the generator	Uniform distribution (integer), uniform distribution (float), normal distribution (float)	The type of the random number generator.
Generator architecture	Central limit components (recommended) or Box Muller	The algorithm to use for the Gaussian distribution generator (**normal distribution** only).
Seed selection	Auto or manaul	Set the seed manually or automatically.
Value of the seed	1 to 2147483647; default: 68997764	Manually input the seed for the random sequence, in the format of an integer.

1.6. Document Revision History for the Random Number Generator IP Core User Guide

Date	Version	Changes
May 2020	2020.05.05	Removed support for Cyclone IV, Cyclone V, and Intel MAX 10 devices.
May 2015	2016.05.02	Initial release.
February 2017	2017.02.21	Corrected `rand_num_data` and `rand_num_valid` signals to be output.