Intel® Quartus® Prime Pro Edition
User Guide

Timing Analyzer

Updated for Intel® Quartus® Prime Design Suite: 21.1
1. Timing Analysis Introduction

Comprehensive timing analysis of your design allows you to validate circuit performance, identify timing violations, and drive the Fitter's placement of logic to meet your timing goals. The Intel® Quartus® Prime Timing Analyzer uses industry-standard constraint and analysis methodology to report on all data required times, data arrival times, and clock arrival times for all register-to-register, I/O, and asynchronous reset paths in your design.

The Timing Analyzer verifies that required timing relationships are met for your design to correctly function, and confirms actual signal arrival times against the constraints that you specify. This user guide provides an introduction to basic timing analysis concepts, along with step-by-step instructions for using the Intel Quartus Prime Timing Analyzer.

1.1. Timing Analysis Basic Concepts

This user guide introduces the following concepts to describe timing analysis:

Table 1. Timing Analyzer Terminology

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arrival time</td>
<td>The Timing Analyzer calculates the data and clock arrival time versus the required time at register pins.</td>
</tr>
<tr>
<td>Cell</td>
<td>Device resource that contains look-up tables (LUT), registers, digital signal processing (DSP) blocks, memory blocks, or input/output elements. In Intel Stratix® series devices, the LUTs and registers are contained in logic elements (LE) modeled as cells.</td>
</tr>
<tr>
<td>Clock</td>
<td>Named signal representing clock domains inside or outside of your design.</td>
</tr>
<tr>
<td>Clock-as-data analysis</td>
<td>More accurate timing analysis for complex paths that includes any phase shift associated with a PLL for the clock path, and considers any related phase shift for the data path.</td>
</tr>
<tr>
<td>Clock hold time</td>
<td>Minimum time interval that a signal must be stable on the input pin that feeds a data input or clock enable, after an active transition on the clock input.</td>
</tr>
<tr>
<td>Clock launch and latch edge</td>
<td>The launch edge is the clock edge that sends data out of a register or other sequential element, and acts as a source for the data transfer. The latch edge is the active clock edge that captures data at the data port of a register or other sequential element, acting as a destination for the data transfer.</td>
</tr>
<tr>
<td>Clock pessimism</td>
<td>Clock pessimism refers to use of the maximum (rather than minimum) delay variation associated with common clock paths during static timing analysis.</td>
</tr>
<tr>
<td>Clock setup time</td>
<td>Minimum time interval between the assertion of a signal at a data input, and the assertion of a low-to-high transition on the clock input.</td>
</tr>
<tr>
<td>Maximum or minimum delay constraint</td>
<td>A constraint that specifies timing path analysis with a non-default setup or hold relationship.</td>
</tr>
<tr>
<td>Net</td>
<td>A collection of two or more interconnected components.</td>
</tr>
</tbody>
</table>

continued...
### Term and Definition

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Node</td>
<td>Represents a wire carrying a signal that travels between different logical components in the design. Most basic timing netlist unit. Used to represent ports, pins, and registers.</td>
</tr>
<tr>
<td>Pin</td>
<td>Inputs or outputs of cells.</td>
</tr>
<tr>
<td>Port</td>
<td>Top-level module inputs or outputs; for example, a device pin.</td>
</tr>
<tr>
<td>Metastability</td>
<td>Metastability problems can occur when a signal transfers between circuitry in unrelated or asynchronous clock domains. The Timing Analyzer analyzes the potential for metastability in your design and can calculate the MTBF for synchronization register chains.</td>
</tr>
<tr>
<td>Multicorner analysis</td>
<td>Timing analysis of slow and fast timing corners to verify your design under a variety of voltage, process, and temperature operating conditions.</td>
</tr>
<tr>
<td>Multicycle paths</td>
<td>A data path that requires a non-default number of clock cycles for proper analysis.</td>
</tr>
<tr>
<td>Recovery and removal time</td>
<td>Recovery time is the minimum length of time for the deassertion of an asynchronous control signal relative to the next clock edge. Removal time is the minimum length of time the deassertion of an asynchronous control signal must be stable after the active clock edge.</td>
</tr>
<tr>
<td>Timing netlist</td>
<td>A Compiler-generated list of your design's synthesized nodes and connections. The Timing Analyzer requires this netlist to perform timing analysis.</td>
</tr>
<tr>
<td>Timing path</td>
<td>The wire connection (net) between any two sequential design nodes, such as the output of a register to the input of another register.</td>
</tr>
</tbody>
</table>

### 1.1.1. Timing Path and Clock Analysis

The Timing Analyzer measures the timing performance for all timing paths identified in your design. The Timing Analyzer requires a timing netlist that describes your design's nodes and connections for analysis. The Timing Analyzer also determines clock relationships for all register-to-register transfers in your design by analyzing the clock setup and hold relationship between the launch edge and latch edge of the clock.

#### 1.1.1.1. The Timing Netlist

The Timing Analyzer uses the timing netlist data to determine the data and clock arrival time versus required time for all timing paths in the design. You can generate the timing netlist in the Timing Analyzer any time after running the Fitter.

The following figures illustrate division of a simple design schematic into timing netlist delays.

**Figure 1. Simple Design Schematic**

![Simple Design Schematic](image-url)
1.1.1.2. Timing Paths

Timing paths connect two design nodes, such as the output of a register to the input of another register.

Understanding the types of timing paths is important to timing closure and optimization. The Timing Analyzer recognizes and analyzes the following timing paths:

- **Edge paths**—connections from ports-to-pins, from pins-to-pins, and from pins-to-ports.
- **Clock paths**—connections from device ports or internally generated clock pins to the clock pin of a register.
- **Data paths**—connections from a port or the data output pin of a sequential element to a port or the data input pin of another sequential element.
- **Asynchronous paths**—connections from a port or asynchronous pins of another sequential element such as an asynchronous reset or asynchronous clear.

In addition to identifying various paths in a design, the Timing Analyzer analyzes clock characteristics to compute the worst-case requirement between any two registers in a single register-to-register path. You must constrain all clocks in your design before analyzing clock characteristics.
1.1.1.3. Data and Clock Arrival Times

After the Timing Analyzer identifies the path type, the Timing Analyzer can report data and clock arrival times at register pins.

The Timing Analyzer calculates data arrival time by adding the launch edge time to the delay from the clock source to the clock pin of the source register, the micro clock-to-output delay (\(\mu t_{CO}\)) of the source register, and the delay from the source register’s data output (Q) to the destination register’s data input (D).

The Timing Analyzer calculates data required time by adding the latch edge time to the sum of all delays between the clock port and the clock pin of the destination register. It includes any clock port buffer delays and subtracts the micro setup time (\(\mu t_{SU}\)) (or adds the micro hold time) of the destination register. Where the \(\mu t_{SU}\) is the intrinsic setup time of an internal register in the FPGA.

Figure 4. Data Arrival and Data Required Times

![Data Arrival and Data Required Times Diagram]

The basic calculations for data arrival and data required times including the launch and latch edges.

Figure 5. Data Arrival and Data Required Time Equations

Data Arrival Time \(=\) Launch Edge + Source Clock Delay + \(\mu t_{CO}\) + Register-to-Register Delay
Data Required Time \(=\) Latch Edge + Destination Clock Delay – \(\mu t_{SU}\)

1.1.1.4. Launch and Latch Edges

All timing analysis requires the presence of one or more clock signals. The Timing Analyzer determines clock relationships for all register-to-register transfers in your design by analyzing the clock setup and hold relationship between the launch edge and latch edge of the clock.

The launch edge of the clock signal is the clock edge that sends data out of a register or other sequential element, and acts as a source for the data transfer. The latch edge is the active clock edge that captures data at the data port of a register or other sequential element, acting as a destination for the data transfer.
**Figure 6. Setup and Hold Relationship for Launch and Latch Edges 10ns Apart**

In this example, the launch edge sends the data from register `reg1` at 0 ns, and the register `reg2` captures the data when triggered by the latch edge at 10 ns. The data arrives at the destination register before the next latch edge.

You must define all clocks in your design by assigning a clock constraint to each clock source node. These clock constraints provide the structure required for repeatable data relationships. If you do not constrain the clocks in your design, the Intel Quartus Prime software analyzes all clocks as 1 GHz clocks to maximize timing based Fitter effort. To ensure realistic slack values, you must constrain all clocks in your design with real values.

### 1.1.2. Clock Setup Analysis

To perform a clock setup check, the Timing Analyzer determines a setup relationship by analyzing each launch and latch edge for each register-to-register path.

For each latch edge at the destination register, the Timing Analyzer uses the closest previous clock edge at the source register as the launch edge. The following figure shows two setup relationships, setup A and setup B. For the latch edge at 10 ns, the closest clock that acts as a launch edge is at 3 ns and has the setup A label. For the latch edge at 20 ns, the closest clock that acts as a launch edge is 19 ns and has the setup B label. The Timing Analyzer analyzes the most restrictive setup relationship, in this case setup B; if that relationship meets the design requirement, then setup A meets the requirement by default.

**Figure 7. Setup Check**

The Timing Analyzer reports the result of clock setup checks as slack values. Slack is the margin by which a timing requirement is met or not met. Positive slack indicates the margin by which a requirement is met; negative slack indicates the margin by which a requirement is not met.
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Figure 8. **Clock Setup Slack for Internal Register-to-Register Paths**

- Clock Setup Slack = Data Required Time – Data Arrival Time
- Data Arrival Time = Launch Edge + Clock Network Delay + Source Register + µt_u + Register-to-Register Delay
- Data Required Time = Latch Edge + Clock Network Delay to Destination Register – µt_u – Setup Uncertainty

The Timing Analyzer performs setup checks using the maximum delay when calculating data arrival time, and minimum delay when calculating data required time. Some of the spread between maximum arrival path delays and minimum required path delays may be recoverable with path pessimism removal, as **Timing Pessimism** on page 15 describes.

Figure 9. **Clock Setup Slack from Input Port to Internal Register**

- Clock Setup Slack = Data Required Time – Data Arrival Time
- Data Arrival Time = Launch Edge + Clock Network Delay + Input Maximum Delay + Port-to-Register Delay
- Data Required Time = Latch Edge + Clock Network Delay to Destination Register – µt_u – Setup Uncertainty

Figure 10. **Clock Setup Slack from Internal Register to Output Port**

- Clock Setup Slack = Data Required Time – Data Arrival Time
- Data Arrival Time = Launch Edge + Clock Network Delay to Source Register +µt_u + Register-to-Port Delay
- Data Required Time = Latch Edge + Clock Network Delay to Output Port – Output Maximum Delay

### 1.1.3. Clock Hold Analysis

To perform a clock hold check, the Timing Analyzer determines a hold relationship for each possible setup relationship that exists for all source and destination register pairs. The Timing Analyzer checks all adjacent clock edges from all setup relationships to determine the hold relationships.

The Timing Analyzer performs two hold checks for each setup relationship. The first hold check determines that the data launched by the current launch edge is not captured by the previous latch edge. The second hold check determines that the data launched by the next launch edge is not captured by the current latch edge. From the possible hold relationships, the Timing Analyzer selects the hold relationship that is the most restrictive. The most restrictive hold relationship is the hold relationship with the smallest difference between the latch and launch edges and determines the minimum allowable delay for the register-to-register path. In the following example, the Timing Analyzer selects hold check A2 as the most restrictive hold relationship of two setup relationships, setup A and setup B, and their respective hold checks.

Figure 11. **Setup and Hold Check Relationships**

Source Clock

**Hold Check A1**

**Setup A**

**Hold Check A2**

**Hold Check B1**

**Hold Check B2**

Destination Clock

0 ns  8 ns  16 ns  24 ns  32 ns
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1.1.4. Recovery and Removal Analysis

Recovery time is the minimum length of time for the deassertion of an asynchronous control signal relative to the next clock edge.

For example, signals such as clear and preset must be stable before the next active clock edge. The recovery slack calculation is similar to the clock setup slack calculation, but the calculation applies to asynchronous control signals.

Figure 15. Recovery Slack Calculation if the Asynchronous Control Signal is Registered

Recovery Slack Time = Data Required Time – Data Arrival Time
Data Required Time = Latch Edge + Clock Network Delay to Destination Register – μ_{R}
Data Arrival Time = Launch Edge + Clock Network Delay to Source Register + μ_{s} + Register-to-Register Delay

Figure 16. Recovery Slack Calculation if the Asynchronous Control Signal is not Registered

Recovery Slack Time = Data Required Time – Data Arrival Time
Data Required Time = Latch Edge + Clock Network Delay to Destination Register – μ_{R}
Data Arrival Time = Launch Edge + Clock Network Delay + Input Maximum Delay + Port-to-Register Delay

Note:

If the asynchronous reset signal is from a device I/O port, you must create an input delay constraint for the asynchronous reset port for the Timing Analyzer to perform recovery analysis on the path.

Removal time is the minimum length of time the deassertion of an asynchronous control signal must be stable after the active clock edge. The Timing Analyzer removal slack calculation is similar to the clock hold slack calculation, but the calculation applies to asynchronous control signals.
Figure 17. Removal Slack Calculation if the Asynchronous Control Signal is Registered

\[ \text{Removal Slack Time} = \text{Data Arrival Time} - \text{Data Required Time} \]
\[ \text{Data Arrival Time} = \text{Launch Edge + Clock Network Delay to Source Register + } \mu t_{s} \text{ of Source Register + Register-to-Register Delay} \]
\[ \text{Data Required Time} = \text{Latch Edge + Clock Network Delay to Destination Register + } \mu t_{h} \]

Figure 18. Removal Slack Calculation if the Asynchronous Control Signal is not Registered

\[ \text{Removal Slack Time} = \text{Data Arrival Time} - \text{Data Required Time} \]
\[ \text{Data Arrival Time} = \text{Launch Edge + Clock Network Delay + Input Minimum Delay of Pin + Minimum Pin-to-Register Delay} \]
\[ \text{Data Required Time} = \text{Latch Edge + Clock Network Delay to Destination Register + } \mu t_{h} \]

If the asynchronous reset signal is from a device pin, you must create an input delay constraint to the asynchronous reset pin for the Timing Analyzer to perform removal analysis on the path.

1.1.5. Multicycle Path Analysis

Multicycle paths are data paths that require either a non-default setup or hold relationship, for proper analysis.

For example, a register may be required to capture data on every second or third rising clock edge. A multicycle path is between the input registers of a multiplier and an output register where the destination latches data on every other clock edge.

Figure 19. Multicycle Path

A register-to-register path is for the default setup and hold relationship. Also for the respective timing diagrams for the source and destination clocks and the default setup and hold relationships, when the source clock, src_clk, has a period of 10 ns and the destination clock, dst_clk, has a period of 5 ns. The default setup relationship is 5 ns; the default hold relationship is 0 ns.
To accommodate the system requirements you can modify the default setup and hold relationships by specifying a multicycle timing constraint to a register-to-register path.

The exception has a multicycle setup assignment of two to use the second occurring latch edge; in this example, to 10 ns from the default value of 5 ns.

1.1.5.1. Multicycle Clock Hold

The number of clock periods between the clock launch edge and the latch edge defines the setup relationship.
By default, the Timing Analyzer performs a single-cycle path analysis. When analyzing a path, the Timing Analyzer performs two hold checks. The first hold check determines that the data that launches from the current launch edge is not captured by the previous latch edge. The second hold check determines that the data that launches from the next launch edge is not captured by the current latch edge. The Timing Analyzer reports only the most restrictive hold check. The Timing Analyzer calculates the hold check by comparing launch and latch edges.

**Figure 23. Hold Check**

The Timing Analyzer uses the following calculation to determine the hold check.

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
\text{hold check 2} = \text{next launch edge} - \text{current latch edge}
\]

**Tip:** If a hold check overlaps a setup check, the hold check is ignored.

A start multicycle hold assignment modifies the launch edge of the source clock by moving the launch edge the number of clock periods you specify to the right of the default launch edge. The following figure shows various values of the start multicycle hold (SMH) assignment and the resulting launch edge.

**Figure 24. Start Multicycle Hold Values**

An end multicycle hold assignment modifies the latch edge of the destination clock by moving the latch edge the specific number of clock periods to the left of the default latch edge. The following figure shows various values of the end multicycle hold (EMH) assignment and the resulting latch edge.

**Figure 25. End Multicycle Hold Values**
The following shows the hold relationship the Timing Analyzer reports for the negative hold relationship:

**1.1.5.2. Multicycle Clock Setup**

The setup relationship is defined as the number of clock periods between the latch edge and the launch edge. By default, the Timing Analyzer performs a single-cycle path analysis, which results in the setup relationship being equal to one clock period (latch edge – launch edge). Applying a multicycle setup assignment, adjusts the setup relationship by the multicycle setup value. The adjustment value may be negative.

An end multicycle setup assignment modifies the latch edge of the destination clock by moving the latch edge the specified number of clock periods to the right of the determined default latch edge. The following figure shows various values of the end multicycle setup (EMS) assignment and the resulting latch edge.

A start multicycle setup assignment modifies the launch edge of the source clock by moving the launch edge the specified number of clock periods to the left of the determined default launch edge. A start multicycle setup (SMS) assignment with various values can result in a specific launch edge.
1.1.6. Metastability Analysis

Metastability problems can occur when a signal transfers between circuitry in unrelated or asynchronous clock domains because the signal does not meet setup and hold time requirements.

To minimize the failures due to metastability, circuit designers typically use a sequence of registers, also known as a synchronization register chain, or synchronizer, in the destination clock domain to resynchronize the data signals to the new clock domain.

The mean time between failures (MTBF) is an estimate of the average time between instances of failure due to metastability.

The Timing Analyzer analyzes the potential for metastability in your design and can calculate the MTBF for synchronization register chains. The Timing Analyzer then estimates the MTBF of the entire design from the synchronization chains the design contains.

In addition to reporting synchronization register chains found in the design, the Intel Quartus Prime software also protects these registers from optimizations that might negatively impact MTBF, such as register duplication and logic retiming. The Intel Quartus Prime software can also optimize the MTBF of your design if the MTBF is too low.

Related Information

- Understanding Metastability in FPGAs
1.1.7. Timing Pessimism

Common clock path pessimism removal accounts for the minimum and maximum delay variation associated with common clock paths during static timing analysis by adding the difference between the maximum and minimum delay value of the common clock path to the appropriate slack equation.

Minimum and maximum delay variation can occur when two different delay values are used for the same clock path. For example, in a simple setup analysis, the maximum clock path delay to the source register is used to determine the data arrival time. The minimum clock path delay to the destination register is used to determine the data required time. However, if the clock path to the source register and to the destination register share a common clock path, both the maximum delay and the minimum delay are used to model the common clock path during timing analysis. The use of both the minimum delay and maximum delay results in an overly pessimistic analysis since two different delay values, the maximum and minimum delays, cannot be used to model the same clock path.

Figure 30. Typical Register to Register Path

Segment A is the common clock path between reg1 and reg2. The minimum delay is 5.0 ns; the maximum delay is 5.5 ns. The difference between the maximum and minimum delay value equals the common clock path pessimism removal value; in this case, the common clock path pessimism is 0.5 ns. The Timing Analyzer adds the common clock path pessimism removal value to the appropriate slack equation to determine overall slack. Therefore, if the setup slack for the register-to-register path in the example equals 0.7 ns without common clock path pessimism removal, the slack is 1.2 ns with common clock path pessimism removal.

You can also use common clock path pessimism removal to determine the minimum pulse width of a register. A clock signal must meet a register’s minimum pulse width requirement to be recognized by the register. A minimum high time defines the minimum pulse width for a positive-edge triggered register. A minimum low time defines the minimum pulse width for a negative-edge triggered register.

Clock pulses that violate the minimum pulse width of a register prevent data from being latched at the data pin of the register. To calculate the slack of the minimum pulse width, the Timing Analyzer subtracts the required minimum pulse width time from the actual minimum pulse width time. The Timing Analyzer determines the actual minimum pulse width time by the clock requirement you specified for the clock that
feeds the clock port of the register. The Timing Analyzer determines the required minimum pulse width time by the maximum rise, minimum rise, maximum fall, and minimum fall times.

**Figure 31.** Required Minimum Pulse Width time for the High and Low Pulse

<table>
<thead>
<tr>
<th>High Pulse Width</th>
<th>Minimum Rise Rise Arrival Times</th>
<th>Maximum Rise Rise Arrival Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.5</td>
<td></td>
</tr>
<tr>
<td>0.9</td>
<td>0.7</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low Pulse Width</th>
<th>Minimum Fall Fall Arrival Times</th>
<th>Maximum Fall Fall Arrival Times</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.8</td>
<td>0.5</td>
<td></td>
</tr>
</tbody>
</table>

With common clock path pessimism, the minimum pulse width slack can be increased by the smallest value of either the maximum rise time minus the minimum rise time, or the maximum fall time minus the minimum fall time. In the example, the slack value can be increased by 0.2 ns, which is the smallest value between 0.3 ns (0.8 ns – 0.5 ns) and 0.2 ns (0.9 ns – 0.7 ns).

### 1.1.8. Clock-As-Data Analysis

The majority of FPGA designs contain simple connections between any two nodes known as either a data path or a clock path.

A data path is a connection between the output of a synchronous element to the input of another synchronous element.

A clock is a connection to the clock pin of a synchronous element. However, for more complex FPGA designs, such as designs that use source-synchronous interfaces, this simplified view is no longer sufficient. Clock-as-data analysis is performed in circuits with elements such as clock dividers and DDR source-synchronous outputs.

The connection between the input clock port and output clock port can be treated either as a clock path or a data path. **Figure 32** on page 16 shows a design where the path from port `clk_in` to port `clk_out` is both a clock and a data path. The clock path is from the port `clk_in` to the register `reg_data` clock pin. The data path is from port `clk_in` to the port `clk_out`.

**Figure 32.** Simplified Source Synchronous Output
With clock-as-data analysis, the Timing Analyzer provides a more accurate analysis of the path based on user constraints. For the clock path analysis, any phase shift associated with the phase-locked loop (PLL) is taken into consideration. For the data path analysis, any phase shift associated with the PLL is taken into consideration rather than ignored.

The clock-as-data analysis also applies to internally generated clock dividers. In the following figure, the waveforms are for the inverter feedback path, analyzed during timing analysis. The output of the divider register determines the launch time, and the clock port of the register determines the latch time.

**Figure 33. Clock Divider**

![Clock Divider Diagram]

**1.1.9. Multicorner Timing Analysis**

You can direct the Timing Analyzer to perform multicorner timing analysis to verify your design under different voltage, process, and temperature operating conditions.

To ensure that no violations occur under different timing conditions (models) during device operation, you must perform static timing analysis under all available operating conditions.

You specify the operating conditions in the Timing Analyzer prior to running analysis.

**Related Information**

Setting the Operating Conditions on page 27

**1.1.10. Time Borrowing**

Time borrowing can improve performance by enabling the path ending at a time-borrowing flip-flop or latch to "borrow" time from the next path in the register pipeline. The borrowed time subtracts from the next path, resulting in the same cumulative timing. In this way, time borrowing can shift slack to more critical parts of the design. Without time borrowing, the Timing Analyzer analyzes each path independently and normally assumes exactly one clock cycle for each transfer.
Some of the flip-flops in Intel Stratix 10 and Intel Arria® 10 devices allow time borrowing. The exact size of the available time borrow window depends on hardware settings. The Fitter (Finalize) stage automatically configures the appropriate borrow window for each time-borrowing flip-flop, based on hardware restrictions and the available hold slack.\(^{(1)}\)

Intel FPGA devices generally support only a few borrow window sizes. For example, Intel Stratix 10 devices support narrow, medium, and wide. Typically, groups of several flip-flops must share the same setting. The actual borrowed amount is completely flexible within a given borrow window. The Timing Analyzer calculates the borrowed amount separately for each operating condition, clock, and signal rise and fall edge. Selecting a wider borrow window reduces hold slack. The Compiler only selects wider settings if hold slack allows. Furthermore, if the Compiler determines that a narrower window is sufficient for a given group of registers (based on the optimal time borrowing solution), the Compiler uses the narrower window, even if there is sufficient hold slack for a wider window.

\(^{(1)}\) In Partial Reconfiguration designs, additional restrictions may apply to time-borrowing window size.
For a given borrow window size, the exact size of the borrow window may depend on
the register input (for example, d or sclr), the edge of the incoming signal (rising or
falling), the device speed grade, and operating conditions.

You can enable automatic implementation of time borrowing without making any RTL
changes. Once enabled, the Fitter automatically configures the window size. The Fitter
also determines the optimal time borrow amount within the available borrow window
for any design registers that the Fitter places in time-borrowing flip-flops.

Proper timing analysis of designs that contain level-sensitive latches typically requires
time borrowing. However, the automatic Fitter time borrowing optimizations do not
apply for level-sensitive latches, as Time Borrowing with Latches on page 20
describes in detail.

Related Information
- Enabling Time Borrowing Optimization on page 29
- Report Time Borrowing Data on page 59

1.1.10.1. Time Borrowing Limitations

Time borrowing optimization, which occurs in the Fitter (Finalize) stage, cannot occur
for the following registers. For these registers, the time borrowing optimization is zero,
and the maximum operating frequency in the Fmax Summary reports include zero
time borrowing:

- Any register that is the source of a cross-clock transfer
- Any register that is the source of a set_max_skew or set_max_delay
  assignment
- Any register in a clock domain with one or more level-sensitive latch

Furthermore, registers that are destinations of cross-clock transfers, set_max_skew
or set_max_delay constraints do not have borrowing values that are optimized for
such transfers (but may still have non-zero borrowing from other transfers).

If any such registers are on the critical timing path, you can possibly report better
performance by enabling Dynamic time borrowing mode, which reports time
borrowing for all borrow-capable registers. Dynamic time borrowing mode can then
provide a more accurate (less pessimistic) analysis, but only at a specific set of clock
frequencies that you specify in the .sdc.

To view time borrowing results for such registers:
1. Set the clock frequency in the .sdc file to a value higher than the clock frequency
   that Fmax Summary reports.
2. Reset your design and re-read the SDC file in the Timing Analyzer.
3. Run the update_timing_netlist -dynamic_borrow command.
4. View the results in Slack Summary reports (Reports ▶ Slack) to determine if
timing passes. The Fmax Summary report does not reflect any gains from
dynamic borrowing.
Note: Time borrowing is similar to the beneficial clock skew technique, whereby you delay the clock to a given register, giving more time to the incoming paths at the expense of the outgoing paths. However, time borrowing and beneficial clock skew have the following important differences:

- Time borrowing offers more flexibility than clock skew in distributing setup slack. Skewing is typically limited to fixed increments. You can use borrowing to shift any amount of slack (however small) from one side of the register to the other, as long as the amounts fit within the available borrow window. Furthermore, borrow amounts calculate separately for each operating condition, making it possible to shift the optimum amount of slack for each operating condition. This type of shifting is not possible with skewing.

- You can use beneficial clock skew to increase Hold slack on outgoing paths from the register where the clock is skewed. Time borrowing does not offer this benefit.

1.1.10.2. Time Borrowing with Latches

The Intel Quartus Prime Timing Analyzer treats level-sensitive latches similar to registers. The Timing Analyzer treats the latch enable pin as a clock pin, while modifying the clock relationship appropriately.

You can run Reports ➤ Diagnostic ➤ Check Timing in the Timing Analyzer Tasks pane to view a list of the level-sensitive latches in your design.

Implementation of latch time borrowing requires that you enable Dynamic borrowing mode (update_timing_netlist -dynamic_borrow). Otherwise, the Timing Analyzer calculates zero time borrowing for latches. In Dynamic mode, the Timing Analyzer simply reports the amount of time borrowing that would physically happen in the circuit, given the clock frequencies you specify in SDC constraints, and does not actually optimize borrowing in any way.

For latches, the setup relationship is to the opening edge of the latch, which allows time borrowing. The hold relationship is to the closing edge of the latch. For example, a path from a positive register to another positive register has a default setup clock relationship of one clock period. A path from a positive register to a positive (open-high), level-sensitive latch has a default setup clock relationship of zero clock periods, plus any time borrow value.

The Timing Analyzer treats paths to and from a latch as two separate paths. For example, in a positive register--> positive latch--> negative register transfer, the Timing Analyzer does not analyze the overall register-->register transfer, even though you expect the latch to be transparent for the entire duration of the transfer. The Timing Analyzer analyzes and reports the paths to and from the latch separately.

The Timing Analyzer automatically computes the maximum amount of time borrowing available for each latch. Typically, the maximum amount of time borrowing available is roughly equivalent to half the clock period. The exact amount of time borrowing available is based on:

- The timing of opening and closing latch edges
- Physical latch implementation (closing-edge $\mu t_{SU}$ of the latch)
- Clock uncertainty and other effects
The time borrowing never exceeds the maximum borrow value. However, you can specify a smaller maximum borrow time with the `set_max_time_borrow` SDC constraint. For example:

```c
#Borrow at most 3ns at all "lat*" latches:
set_max_time_borrow 3 [get_registers lat*]
```

Specifying a clock with a negative borrow window can result in negative maximum borrowable time, which is equivalent to a minimum pulse width violation. For example, this condition can occur if half the clock period is smaller than the closing-edge $\mu t_{SU}$ of the latch. If such a violation occurs, a warning indicates that the design cannot pass timing.

**Note:** Whether you use time borrowing or not, do not rely on the timing analysis Fmax Summary report for any clock domains with latches. The Fmax Summary values for such clock domains include no borrowing, and are therefore significantly pessimistic.

---

### 1.2. Timing Analysis Overview Document Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020.09.28</td>
<td>20.3</td>
<td>• Revised setup arrow direction in multiple timing diagrams for consistency.</td>
</tr>
<tr>
<td>2020.04.13</td>
<td>20.1</td>
<td>• Added &quot;Time Borrowing&quot; section.</td>
</tr>
<tr>
<td>2019.09.30</td>
<td>19.3</td>
<td>• Updated &quot;MultiCorner Timing Analysis&quot; code example and stated limitation for operating conditions.</td>
</tr>
<tr>
<td>2019.07.15</td>
<td>19.2</td>
<td>• Updated &quot;MultiCorner Analysis&quot; for SmartVID timing models.</td>
</tr>
<tr>
<td>2018.09.24</td>
<td>18.1</td>
<td>Minor text enhancements for clarity and style.</td>
</tr>
</tbody>
</table>

**Table 2. Document Revision History**

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2016.10.31</td>
<td>16.1</td>
<td>• Implemented Intel rebranding.</td>
</tr>
<tr>
<td>2016.05.02</td>
<td>16.0</td>
<td>Corrected typo in Fig 6-14: Clock Hold Slack Calculation from Internal Register to Output Port</td>
</tr>
<tr>
<td>2015.11.02</td>
<td>15.1</td>
<td>Changed instances of Quartus II to Intel Quartus Prime.</td>
</tr>
<tr>
<td>2014.12.15</td>
<td>14.1</td>
<td>Moved Multicycle Clock Setup Check and Hold Check Analysis section from the Timing Analyzer chapter.</td>
</tr>
<tr>
<td>June 2014</td>
<td>14.0</td>
<td>Updated format</td>
</tr>
<tr>
<td>June 2012</td>
<td>12.0</td>
<td>Added social networking icons, minor text updates</td>
</tr>
<tr>
<td>November 2011</td>
<td>11.1</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
2. Using the Intel Quartus Prime Timing Analyzer

The Intel Quartus Prime Timing Analyzer is a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design using an industry-standard constraint, analysis, and reporting methodology. Use the Timing Analyzer GUI or command-line interface to constrain, analyze, and report results for all timing paths in your design.

Figure 36. Intel Quartus Prime Timing Analyzer

Related Information
- Timing Analyzer Quick-Start Tutorial: Intel Quartus Prime Pro Edition
2. Using the Intel Quartus Prime Timing Analyzer

UG-20140 | 2021.08.27

- Timing Analyzer Resource Center
- Intel FPGA Technical Training

2.1. Timing Analysis Flow

After creating your design and setting up a project, you define the required timing constraints for your design in a Synopsys* Design Constraints (.sdc) file. The Fitter then attempts to place logic to meet or exceed your constraints. The Timing Analyzer reports conditions that do not meet constraints, allowing you to correct critical timing issues. The following steps describe the basic timing analysis flow:

- Step 1: Specify Timing Analyzer Settings on page 23
- Step 2: Specify Timing Constraints on page 25
- Step 3: Run the Timing Analyzer on page 26
- Step 4: Analyze Timing Reports on page 31

2.2. Step 1: Specify Timing Analyzer Settings

Before running timing analysis, you must open an Intel Quartus Prime project and run the Fitter to generate the timing netlist. You can consider and specify general settings for timing analysis, as well as other project-wide Compiler settings that impact the timing analysis results:

To specify general Timing Analyzer settings, follow these steps:

1. Click File > New Project Wizard to create a new project, or click File > Open Project to open an existing project.
2. Click Assignments ➤ Settings ➤ Timing Analyzer to open the Timing Analyzer settings.
3. In the **Timing Analyzer** page, specify one or more `.sdc` file for timing analysis, and any of the following options:

**Table 3. Timing Analyzer General Settings**

<table>
<thead>
<tr>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDC files to include in the project</td>
<td>Specifies the name and processing order of Synopsis Design Constraint (.sdc) files in the project.</td>
</tr>
<tr>
<td>Interactive Timing Analysis</td>
<td>Specify options for automatically running timing analysis, reading constraints, and generating reports automatically. Turn on or off:</td>
</tr>
<tr>
<td></td>
<td>• Automatically launch Timing Analyzer GUI after a full compilation (default, on)</td>
</tr>
<tr>
<td></td>
<td>• Automatically read constraints and update the timing netlist when project is opened in Timing Analyzer (default, on)</td>
</tr>
<tr>
<td></td>
<td>• Automatically run setup summary report when project is opened in Timing Analyzer (default, on)</td>
</tr>
<tr>
<td>Default Reporting</td>
<td>Specify options to automatically Report worst-case paths during compilation (default, on). Specify the Paths reported per clock domain (default, 10), and whether to Show routing (default, off) in reports.</td>
</tr>
<tr>
<td>Tcl Script Options</td>
<td>Tcl Script File name specifies the file name for a custom timing analysis script. You can specify whether to Run default timing analysis before running custom script.</td>
</tr>
<tr>
<td>Metastability Analysis</td>
<td>Specifies how the Timing Analyzer identifies registers as being part of a synchronization register chain for metastability analysis.</td>
</tr>
</tbody>
</table>

4. Consider and specify project-wide Compiler settings that can have a significant impact on Timing Analysis:
Table 4. Compiler Settings Impacting Timing Analysis

<table>
<thead>
<tr>
<th>Setting</th>
<th>Description</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable multicorner support for Timing Analyzer and EDA Netlist Writer (default, on)</td>
<td>Directs the Timing Analyzer to perform multicorner timing analysis by default, which analyzes the design against best-case and worst-case operating conditions.</td>
<td>Assignments ➤ Settings ➤ Compilation Process Settings</td>
</tr>
<tr>
<td>Optimization Mode (default, Balanced)</td>
<td>Specifies the focus of Compiler optimization efforts during synthesis and fitting. Specify a Balanced strategy, or optimize for Performance, Area, Power, Routability, or Compile Time.</td>
<td>Assignments ➤ Settings ➤ Compiler Settings</td>
</tr>
<tr>
<td>SDC Constraint Protection (default, off)</td>
<td>Verifies .sdc constraints in register merging. This option helps to maintain the validity of .sdc constraints through compilation.</td>
<td>Assignments ➤ Settings ➤ Compiler Settings ➤ Advanced Settings (Synthesis)</td>
</tr>
<tr>
<td>Synchronization Register Chain Length (default, 3)</td>
<td>Specifies the maximum number of registers in a row that the Compiler considers as a synchronization chain. The Compiler prevents optimizations of these registers, such as retiming. When gate-level retiming is enabled, the Compiler does not remove these registers.</td>
<td>Assignments ➤ Settings ➤ Compiler Settings ➤ Advanced Settings (Synthesis)</td>
</tr>
<tr>
<td>Optimize Design for Metastability (default, on)</td>
<td>This setting improves the reliability of the design by increasing its Mean Time Between Failures (MTBF). The Fitter increases the output setup slacks of synchronizer registers in the design. This slack can exponentially increase the design MTBF. This option only applies when using the Timing Analyzer for timing-driven compilation. Use the Timing Analyzer report_metastability command to review the synchronizers detected in your design and to produce MTBF estimates.</td>
<td>Assignments ➤ Settings ➤ Compiler Settings ➤ Advanced Settings (Fitter)</td>
</tr>
</tbody>
</table>

2.3. Step 2: Specify Timing Constraints

You must specify timing constraints that describe the clock frequency requirements, timing exceptions, and I/O timing requirements of your design for comparison against actual conditions during timing analysis. You define timing constraints in one or more Synopsys Design Constraints (.sdc) files that you add to the project.

If you are unfamiliar with .sdc files, you can create an initial .sdc file in the Timing Analyzer GUI, or with provided .sdc file templates. If you are familiar with timing analysis, you can create an .sdc file in any text editor, and then add the file to the project.

1. Use any combination of the following to enter the timing constraints for your design in an .sdc file:
   - Enter constraints in the Timing Analyzer GUI—click Tools ➤ Timing Analyzer, click Update Timing Netlist in the Tasks pane, and then enter constraints from the Constraints menu. The GUI displays the corresponding SDC command that applies.
   - Create an .sdc file on your own. You can start by adding the Recommended Initial SDC Constraints on page 68, and then iteratively modify .sdc constraints and reanalyze the timing results. You must first create clock constraints before entering any constraints dependent on the clock.
2. Save the .sdc file. When entering constraints in the Timing Analyzer GUI, click **Constraints ➤ Write SDC File** to save the constraints you enter in the GUI to an .sdc file.

3. Add the .sdc file to your project, as **Step 1: Specify Timing Analyzer Settings** on page 23 describes.

**Related Information**
- [Using Entity-bound SDC Files](#) on page 73
- [Applying Timing Constraints](#) on page 68

### 2.4. Step 3: Run the Timing Analyzer

You must run the Fitter to generate a timing netlist before running the Timing Analyzer. The Fitter attempts to place logic of your design to comply with the timing constraints that you specify. The Timing Analyzer then reports the margin (slack) by which your design meets or fails each constraint.

1. To generate the timing netlist and run the Timing Analyzer:
Click the Fitter’s **Plan, Place, Route, Retime**, or **Fitter (Finalize)** stage from the Compilation Dashboard, and then click the stage’s Timing Analyzer icon on the Compilation Dashboard. By default, the Timing Analyzer runs analysis on the latest available Fitter snapshot, and then opens the Setup Summary report automatically.

Or

Run a full compilation by clicking **Compile Design** on the Compilation Dashboard. By default, the Timing Analyzer runs analysis with the final timing netlist, and then opens the Setup Summary report automatically.

**Figure 39. Fitter Plan Stage Timing Analyzer Icon**

2. Review the timing reports. To generate additional timing reports for analysis, click the **Reports** menu, and then click a **Slack**, **Datasheet**, **Device Specific**, **Diagnostic**, **Custom**, or **Design Metrics** timing report, as Step 4: Analyze Timing Reports on page 31 describes.

**Figure 40. Setup Summary Report**

3. To run timing analysis under different operation conditions, click **Set Operating Conditions** on the **Tasks** pane and specify options, as Setting the Operating Conditions on page 27 describes.

4. If you specify any settings or constraints that impact timing analysis, click **Update Timing Netlist** on the **Tasks** pane to apply the new constraints to the timing netlist.

**Related Information**

Timing Analyzer Tcl Commands on page 127

**2.4.1. Setting the Operating Conditions**

Click **View ▶ Timing Corners** in the Timing Analyzer to specify operating conditions for analysis under different power and temperature ranges. The available operating conditions vary by device and speed grade. The operating conditions represent the “timing corners” in a multi-corner timing analysis.
Select one or more voltage/temperature combinations and double-click **Report Timing** under **Custom Reports** in the **Tasks** pane to generate timing analysis reports for that model. After generating the report for that model, the report shows the worst-case timing path slacks across all operating conditions that you select.

You can use the following context menu options to generate or regenerate reports in the **Report** window:

- **Regenerate**—regenerates the report you select.
- **Regenerate All Out of Date**—regenerates all reports that are outdated because of SDC changes since the last generation.
- **Delete All Out of Date**—removes all outdated report data.

The following operating conditions are available, depending on your target device and speed grade:

**Table 5. Operating Conditions for Timing Analysis**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Speed Grade</th>
<th>Voltage</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slow 900mV 100C Model</td>
<td>Low voltage, high temperature</td>
<td>Slowest speed grade in device density</td>
<td>$V_{CC}$ minimum supply $^{(1)}$</td>
<td>Maximum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Slow 900mV 0C Model</td>
<td>Low voltage, low temperature</td>
<td>Slowest speed grade in device density</td>
<td>$V_{CC}$ minimum supply $^{(1)}$</td>
<td>Minimum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Fast 900mV 100C Model</td>
<td>High voltage, high temperature</td>
<td>Fastest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Maximum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Fast 900mV 0C Model</td>
<td>High voltage, low temperature</td>
<td>Fastest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Minimum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Slow vid&lt;n&gt; 100C Model</td>
<td>High voltage, high temperature operating conditions for timing analysis with SmartVID.$^{(2)}$</td>
<td>Slowest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Maximum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Slow vid&lt;n&gt; 0C Model</td>
<td>High voltage, low temperature operating conditions for timing analysis with SmartVID.$^{(2)}$</td>
<td>Fastest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Minimum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Slow vid&lt;n&gt; 0C Model$^{(3)}$</td>
<td>High voltage, low temperature operating conditions for timing analysis with SmartVID.$^{(2)}$</td>
<td>Slowest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Minimum $T_J$ $^{(1)}$</td>
</tr>
<tr>
<td>Slow vid&lt;n&gt; 100C Model$^{(3)}$</td>
<td>High voltage, high temperature operating conditions for timing analysis with SmartVID.$^{(2)}$</td>
<td>Slowest speed grade in device density</td>
<td>$V_{CC}$ maximum supply $^{(1)}$</td>
<td>Maximum $T_J$ $^{(1)}$</td>
</tr>
</tbody>
</table>

*continued...*
## 2. Using the Intel Quartus Prime Timing Analyzer

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Speed Grade</th>
<th>Voltage</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast vid&lt;\text{n}&gt; 0C Model(^{(3)})</td>
<td>High voltage, low temperature for timing analysis with SmartVID.(^{(2)})</td>
<td>Fastest speed grade in device density.</td>
<td>(V_{cc}) maximum supply(^{(1)})</td>
<td>Minimum (T_J)(^{(1)})</td>
</tr>
<tr>
<td>Fast vid&lt;\text{n}&gt; 100C Model(^{(3)})</td>
<td>High voltage, high temperature for timing analysis with SmartVID.(^{(2)})</td>
<td>Fastest speed grade in device density.</td>
<td>(V_{cc}) maximum supply(^{(1)})</td>
<td>Maximum (T_J)(^{(1)})</td>
</tr>
</tbody>
</table>

Note:
1. Refer to the applicable device Handbook for \(V_{cc}\) and \(T_J\) values.
2. Intel Stratix 10 and Intel Agilex™ SmartVID designs require this additional model to ensure complete coverage.
3. Intel Agilex devices only.
4. \(n\) refers to device speed grade.

As an alternative to the GUI, you can run the `set_operating_conditions` command with the `-model`, `-speed`, `-temperature`, and `-voltage` options to specify the operating conditions. When running `set_operating_conditions`, you must only specify valid operating conditions for the current device. Run the `get_available_operating_conditions` command to return a list of all valid operating conditions for the current device.

The following example sets the operating conditions to the slow timing model, with a voltage of 1100 mV, and temperature of 85°C:

```plaintext
set_operating_conditions -model slow -temperature 85 -voltage 1100
```

**Related Information**

- Multicorner Timing Analysis on page 17

### 2.4.2. Enabling Time Borrowing Optimization

During any High or Superior **Performance** compilation, the Compiler automatically computes and stores **Optimal** time borrow values for Intel Stratix 10 and Intel Arria 10 designs during the Finalize stage. By default, the subsequent timing analysis results reflect the **Optimal** borrow values from the Finalize stage.

Follow these steps to enable time borrowing for supported devices:

1. Click **Assignments ➤ Settings ➤ Compiler Settings ➤ Optimization Mode**. Select any high or superior **Performance** setting.
2. Run the Fitter and Timing Analyzer, as Step 3: Run the Timing Analyzer on page 26 describes.

3. To generate reports showing time borrowing data, click Reports ➤ Custom Reports ➤ Report Timing. Time borrowing data appears on the critical path for a given clock domain, as Report Time Borrowing Data on page 59 describes.

- To specify time borrowing optimization without changing the Compiler Optimization Mode, specify the following assignment in the project .qsf:

```
set_global_assignment -name ENABLE_TIME_BORROWING_OPTIMIZATION <ON|OFF>
```

- To manually specify the time borrow mode during timing analysis, run one of the following `update_timing_netlist` command options:

### Table 6. Time Borrowing Modes

<table>
<thead>
<tr>
<th>Time Borrowing Mode</th>
<th>Command Option</th>
<th>Default Mode For</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Optimal</strong>—timing analysis includes optimal time borrow values from the Finalize stage. You can optionally add the <code>recompute_borrow</code> option to <code>update_timing_netlist</code> to recompute the borrow amounts, but not the borrow window sizes.</td>
<td><code>update_timing_netlist</code></td>
<td>High and Superior performance compilations for Intel Stratix 10 and Intel Arria 10 designs.</td>
</tr>
<tr>
<td><strong>Dynamic</strong>—timing analysis reports the time borrowing that would physically occur on the device, with respect to your SDC constraints, without any optimization. That is, timing analysis applies as much borrowing as necessary to fix all negative slack. Timing analysis assumes maximum possible borrowing for any timing path where the maximum amount of time borrowing is insufficient to eliminate all negative slack. Only mode that allows borrowing for level-sensitive latches.</td>
<td><code>update_timing_netlist - dynamic_borrow</code></td>
<td>None</td>
</tr>
<tr>
<td><strong>Zero</strong>—timing analysis uses zero time borrowing.</td>
<td><code>update_timing_netlist - no_borrow</code></td>
<td>Unsupported devices, or any Compiler Optimization mode other than a Performance mode.</td>
</tr>
</tbody>
</table>
**Note:** Dynamic mode cannot yield the optimal results with overconstrained clocks, as overconstrained clocks result in excessive negative slack on almost every path. This condition causes use of maximum time borrowing everywhere, which is unlikely to be optimal. When using Partial Reconfiguration, if you compile the base design with time borrowing enabled, compile the implementation design(s) with time borrowing enabled. Otherwise, time borrowing amounts in the base design are reset to zero, and the design may not pass timing. If this condition occurs, you can use the `update_timing_netlist -recompute_borrow` command to restore time borrowing amounts throughout the design.

**Related Information**
Time Borrowing on page 17

### 2.5. Step 4: Analyze Timing Reports

During analysis, the Timing Analyzer examines the timing paths in the design, calculates the propagation delay along each path, checks for timing constraint violations, and reports timing results as positive slack or negative slack. Negative slack indicates a timing violation. Positive slack indicates that timing requirements are met.

The Timing Analyzer provides very fine-grained reporting and analysis capabilities to identify and correct violations along timing paths. Generate timing reports to view how to best optimize the critical paths in your design. If you modify, remove, or add constraints, re-run timing analysis. This iterative process helps resolve timing violations in your design.

**Figure 42. Timing Analyzer Shows Failing Paths in Red**

Reports that indicate failing timing performance appear in red text, and reports that pass appear in black text. A gold question mark icon indicates reports that are outdated due to SDC changes since generation. Regenerate these reports to show the latest data.

The following sections describe how to generate various timing reports for analysis.

### 2.5.1. Generating Timing Reports

The Timing Analyzer generates only a subset of all available reports by default, including the Setup Summary and Timing Analyzer Summary reports. However, you can generate dozens of other detailed reports in the Timing Analyzer GUI, or with command-line commands to help pin-point timing issues. You can customize the display of information in the reports.
The following describe generation of various **Custom**, **Datasheet**, **Diagnostic**, **Slack**, and **Design Metric** timing analysis reports:

- **Report Fmax Summary** on page 32
- **Report Timing** on page 33
- **Report Clock Transfers** on page 38
- **Report Logic Depth** on page 39
- **Report Neighbor Paths** on page 42
- **Report Register Spread** on page 44
- **Report Route Net of Interest** on page 47
- **Report Hierarchical Retiming Restrictions** on page 48
- **Report Reset Statistics** on page 49
- **Report Pipelining Information** on page 49
- **Report Asynchronous CDC** on page 52
- **Report CDC Viewer** on page 56
- **Report Custom CDC Viewer Command** on page 59
- **Report Time Borrowing Data** on page 59

### 2.5.1.1. Report Fmax Summary

The Timing Analyzer's **Reports > Datasheet > Report Fmax Summary** command reports the maximum frequency of each clock in your design. The equivalent scripting command is `report_clock_fmax_summary`.

The Timing Analyzer computes \( f_{\text{MAX}} \) for all paths where the same clock drives the source and destination registers or ports. The Timing Analyzer ignores paths of different clocks and generated clocks. For paths between a clock and its inversion, the Timing Analyzer computes \( f_{\text{MAX}} \) as if the rising and falling edges scale along with \( f_{\text{MAX}} \), such that the duty cycle (in terms of a percentage) is maintained. You must constrain all clocks for accurate timing analysis.

**Figure 43. Fmax Summary Report**

![Fmax Summary Report](image)

The **Restricted Fmax** can indicate a "Limit due to hold check." Typically, hold checks do not limit the maximum frequency \( (f_{\text{MAX}}) \) because these checks are for same-edge relationships, and therefore independent of clock frequency. An example of this occurs when \( \text{setup} = 0 \) and \( \text{hold} = 0 \). However, with an inverted clock transfer, or a multicycle transfer (such as \( \text{setup}=2, \text{hold}=0 \)), then the hold relationship is not a same-edge transfer and changes with the clock frequency.
2.5.1.2. Report Timing

The Timing Analyzer’s Reports ➤ Custom Reports ➤ Report Timing command reports the timing of any path or clock domain in the design. The equivalent scripting command is `report_timing`.

**Figure 44. Report Timing Report**

<table>
<thead>
<tr>
<th>Command Info</th>
<th>Summary of Paths</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slack</td>
<td>From Node</td>
</tr>
<tr>
<td>1</td>
<td>addr...g[2]</td>
</tr>
<tr>
<td>2</td>
<td>addr...g[2]</td>
</tr>
<tr>
<td>3</td>
<td>addr...g[2]</td>
</tr>
</tbody>
</table>

Path #1: Setup slack is 39.103

<table>
<thead>
<tr>
<th>Path Summary</th>
<th>Statistics</th>
<th>Data Path</th>
<th>Waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROPERTY</td>
<td>VALUE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 From Node</td>
<td>addressr_reg[2]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 To Node</td>
<td>my..._mlab_inst0</td>
<td>addr_reg_b[2]</td>
<td></td>
</tr>
<tr>
<td>3 Launch Clock</td>
<td></td>
<td>clk</td>
<td></td>
</tr>
<tr>
<td>4 Latch Clock</td>
<td></td>
<td>clk</td>
<td></td>
</tr>
<tr>
<td>5 Data Arrival Time</td>
<td>3.055</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6 Data Required Time</td>
<td>42.158</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7 Slack</td>
<td>39.103</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8 Worst-Case Operating Conditions</td>
<td>Slow 900mv 100C Model</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

You can specify various options to customize the reporting. You can specify the Clocks and Targets that the report displays, the Analysis Type to run, whether to display Extra Info in the report, and the Output options for the report. For example, you can increase the number of paths to report, add a Target filter, and add a From Clock.

**Figure 45. Report Timing Dialog Box (Top Section)**
Table 7. Report Timing Settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clocks</strong></td>
<td>From Clock and To Clock filter paths in the report to show only the launching or latching clocks you specify.</td>
</tr>
<tr>
<td><strong>Targets</strong></td>
<td>Specifies the target node for From Clock and To Clock to report paths with only those endpoints. Specify an I/O or register name or I/O port for this option. The field also supports wildcard characters. For example, to report only paths within a specific hierarchy: report_timing -from *</td>
</tr>
<tr>
<td><strong>Analysis type</strong></td>
<td>The Analysis type options are Setup, Hold, Recovery, or Removal. The Timing Analyzer reports the results for the type of analysis you select.</td>
</tr>
<tr>
<td><strong>Paths</strong></td>
<td>Specifies the number of paths to display by endpoint and slack level. The default value for Report number of paths is 10, otherwise, the report can be very long. Enable Pairs only to list only one path for each pair of source and destination. Limit further with Maximum number of paths per endpoints. You can also filter paths by entering a value in the Maximum slack limit field.</td>
</tr>
</tbody>
</table>
| **Extra Info**  | Provides additional data that is relevant for diagnosing timing failure root cause, such as intrinsic margin and unexpected routing detours caused by congestion and hold time fix-up. Specify whether to include None, Basic, or All extra information in the report. The Extra Info tab data can help you identify potential, unnecessary routing detours, as well as placement or circuit issues that restrict the path fMAX performance. Refer to Intrinsic Margin and the Extra Info Tab on page 35.  
  - All—report includes Extra Info tab that reports extra information for source timing endpoints that pass through the unregistered output of a RAM or DSP block, or for destination timing endpoints that pass through the unregistered input of a DSP block. The Data Path tab includes Estimated Delay Added for Hold and Route Stage Congestion Impact data.  
  - Basic—report includes the Extra Info tab but no extra information on the Data Path tab.  
  - None—report includes no Extra Info tab or other extra information on the Data Path tab. |
| **Output**      | Specify the path types the analysis includes in output for Detail level: continued... |
### Option and Description

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Summary</strong></td>
<td>- level includes basic summary reports. Review the Clock Skew column in the Summary report. If the skew is less than +/-150ps, the clock tree is well balanced between source and destination.</td>
</tr>
<tr>
<td><strong>Path only</strong></td>
<td>- displays all the detailed information, except the Data Path tab displays the clock tree as one line item.</td>
</tr>
<tr>
<td><strong>Path and Clock</strong></td>
<td>- displays the same as Path only with respect to the clock.</td>
</tr>
<tr>
<td><strong>Full path</strong></td>
<td>- when higher clock skew is present, enable the Full path option. This option breaks the clock tree into greater detail, showing every cell, including the input buffer, PLL, global buffer (called CLKCTRL_), and any logic. Review this data to determine the cause of clock skew in your design. Use the Full path option for I/O analysis because only the source clock or destination clock is inside the FPGA, and therefore the delay is a critical factor to meet timing.</td>
</tr>
</tbody>
</table>

**Show routing**
- Shows routing data in the report.

**Split the report by operating conditions**
- For the operating condition timing corners, subdivides the data by each operating condition.

**Report panel name**
- Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data.

**Tcl command**
- Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.

### Intrinsic Margin and the Extra Info Tab

The Extra Info tab contains other timing metrics to help you diagnose timing closure issues, including Intrinsic Margin for the path. The Extra Info tab can help you identify potential significant or unexpected routing detours caused by congestion and hold time fix-up. The Extra Info tab can also report extra information for source timing endpoints that pass through the unregistered output of a RAM or DSP block, or for destination timing endpoints that pass through the unregistered input of a DSP block. You can review the Extra Info data and Locate Path or Locate Chip Area in Chip Planner, Technology Map Viewer, or Resource Property Viewer to determine whether to make changes to improve placement and routing.

**Figure 47. Extra Info Tab**
Intrinsic margin is a numeric value that the Timing Analyzer calculates from the timing requirements and path element delays. The Timing Analyzer also derives the slack of the path from the same requirements and delays, but with a different calculation. The slack of a path specifies the margin by which the path meets its timing requirement. A path can fail timing requirements for many different reasons. For example, the clock relationship can be impossibly tight, or there can be excessive routing delays that alone cause failure for the timing path. Calculating the intrinsic margin of a timing path, and then comparing that margin to other delays of the path, can help identify the specific reasons why a path fails its timing requirement.

Some delay elements are more sensitive to a path’s placement and routing than others. Intrinsic delays are less sensitive to placement and routing, and are inherent in the RTL and timing requirements. Non-intrinsic delays are the other delays that are sensitive to placement and routing. The Timing Analyzer derives intrinsic margin from the following calculations:

Figure 48. Intrinsic Margin Calculations

- **When the intrinsic margin is less than 0**—the path has such a tight timing relationship, a large difference in microparameters, or such significant clock source uncertainty that the path fails before any additional delay is added. In this case, review the SDC constraints to verify that the timing relationship is correct. An incorrect relationship can exist between unrelated clocks that lack the proper timing cut. Ensure that parameterizable hard blocks are fully registered. Such blocks include M20K RAM and DSP blocks. Also investigate clock sources to verify that the clocks involved are promoted to use global signals for their routing.
- When the clock skew exceeds the intrinsic margin—you must address the clock transfer to meet timing on the path. You may need to create clock region assignments. You might also need to redesign cross-clock transfers to switch from synchronous to asynchronous implementation, such as by using a FIFO or other handshake.

- When the cell delay is greater than its intrinsic margin—the path would fail timing even if the clocks are perfect and uses no routing wires. In this case, you should take actions to reduce the cell delay. You can rewrite RTL to reduce the logic depth, restructure logic to allow the Compiler to use faster LUT inputs, or unblock retiming optimizations. Many stages of the compilation flow can automatically retime registers to reduce logic depth, but only in ways that maintain functionality and that the device architecture supports. Common steps to unblock the Hyper-RTimer include removing asynchronous resets and removing initial conditions. The Extra Info tab reports reasons that block the registers from retiming. Refer to "Retiming Restrictions and Workarounds" in the Intel Hyperflex™ Architecture High-Performance Design Handbook.

- When the interconnect delay is greater than its intrinsic margin—the path would fail timing even if the clocks are perfect, and there is no logic. This situation can occur if registers are too far apart, or a timing path has to detour around a congested area of the chip. Review the fan-in and fan-out of registers that are far apart to determine why they are far apart. Applying Logic Lock regions can cause the Fitter to place the registers closer together within the same region. However, to avoid introducing other problems, use Logic Lock regions to improve placement only after determining why the placement was initially poor. The Fitter can place registers far apart if you do not appropriately size or position the clock regions.

### Table 8. Extra Info Tab Data

<table>
<thead>
<tr>
<th>Extra Info Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic Margin</td>
<td>Reports the intrinsic and non-intrinsic timing elements that comprise the timing path slack value. Intrinsic margin is a numeric value that the Timing Analyzer calculates from the timing requirements and path element delays. The Timing Analyzer also derives the slack of the path from the same requirements and delays, but with a different calculation. Intrinsic delays are less sensitive to placement and routing, and are inherent in the RTL and timing requirements. Non-intrinsic delays are the other delays that are sensitive to placement and routing. Refer to Figure 48 on page 36.</td>
</tr>
<tr>
<td>Max Fanout</td>
<td>Reports the maximum fan-out of register and combinational nodes in the path.</td>
</tr>
<tr>
<td>Source/Destination Bounding Box</td>
<td>Reports the lower-left and upper-right coordinates for the boundary box enclosing the source and destination registers. In an ideal case, the Source/Destination Bounding Box, Cell Bounding Box, and Interconnect Bounding Box values are roughly the same, and the relative areas are approximately 1.0. If the cell bounding box size grows relative to the Source/Destination Bounding Box, that can indicate a potential unnecessary routing detour on the path.</td>
</tr>
<tr>
<td>Cell Bounding Box</td>
<td>Reports the lower-left and upper-right coordinates for the boundary box enclosing the source and destination registers, and any cells in the path.</td>
</tr>
<tr>
<td>Interconnect Bounding Box</td>
<td>Reports the lower-left and upper-right coordinates for the boundary box enclosing the interconnect. The Interconnect Bounding Box would likely expand beyond the Cell Bounding Box due to hold fix-up.</td>
</tr>
<tr>
<td>Source/Destination Relative Area</td>
<td>Reports the area for the source and destination, relative to the Source/Destination Bounding Box. The value is always 1.0, which equals the same size.</td>
</tr>
<tr>
<td>Cell Relative Area</td>
<td>Reports the area for the cell, relative to the Source/Destination Bounding Box. A value of 1.0 equals the same size. A value greater than 1.0 can indicate a path has a cell outside of the space between the registers in the path.</td>
</tr>
</tbody>
</table>

continued...
### Extra Info Data

<table>
<thead>
<tr>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Interconnect Relative Area</strong></td>
<td>Reports the area for the interconnect, relative to the Source/Destination Bounding Box. A value of 1.0 equals the same size. A value greater than 1.0 may indicate a path has a cell outside of the space between the registers in the path.</td>
</tr>
<tr>
<td><strong>Retiming Restriction From Node</strong></td>
<td>Reports any restrictions (for example, “preserve” assignments) that exist on the From Node that limit retiming ability. Consider removing the retiming restriction to allow retiming and improve performance for timing closure.</td>
</tr>
<tr>
<td><strong>Retiming Restriction To Node</strong></td>
<td>Reports any restrictions (for example, “preserve” assignments) that exist on the To Node that limit retiming ability. Consider removing the retiming restriction to allow retiming and improve performance for timing closure.</td>
</tr>
<tr>
<td><strong>From Node is Power-Up &quot;Don't Care&quot;</strong></td>
<td>Reports whether Power-Up &quot;Don't Care&quot; settings exist on the From Node that limit retiming ability. If From Node is Power-Up &quot;Don't Care&quot; value is Yes, this allows retiming. If From Node is Power-Up &quot;Don't Care&quot; value is No; retiming might be restricted. Consider removing the retiming restriction to allow retiming and improve performance for timing closure.</td>
</tr>
<tr>
<td><strong>To Node is Power-Up &quot;Don't Care&quot;</strong></td>
<td>Reports whether Power-Up &quot;Don't Care&quot; settings exists on the To Node that limit retiming ability. If From Node is Power-Up &quot;Don't Care&quot; value is Yes, this allows retiming. If From Node is Power-Up &quot;Don't Care&quot; value is No; retiming might be restricted. Consider removing the retiming restriction to allow retiming and improve performance for timing closure.</td>
</tr>
<tr>
<td><strong>From Node is not fully-registered</strong></td>
<td>Reports RAM or DSP blocks with unregistered outputs. Registering RAM and DSP outputs can significantly improve RAM and DSP timing.</td>
</tr>
<tr>
<td><strong>To Node is not fully-registered</strong></td>
<td>Reports RAM or DSP blocks with unregistered inputs. Registering RAM and DSP inputs can significantly improve RAM and DSP timing.</td>
</tr>
<tr>
<td><strong>Max Borrow Time From Node</strong></td>
<td>Reports the maximum amount of time borrowing that occurs across all paths that involve the From Node.</td>
</tr>
<tr>
<td><strong>Max Borrow Time To Node</strong></td>
<td>Reports the amount of time borrowing that occurs across all paths that involve the To Node.</td>
</tr>
<tr>
<td><strong>Route Stage Congestion Impact</strong></td>
<td>Reports whether routing has a Low, Medium, or High impact on congestion. A Low value suggests timing issues are not congestion related. A High value suggests competition for scarce routing resources plays a role in poor timing.</td>
</tr>
<tr>
<td><strong>Estimated Delay Added for Hold</strong></td>
<td>Reports the estimated amount of delay added on to the fastest delay route to satisfy hold. This value can help you determine whether delays are routing congestion or Hold related.</td>
</tr>
</tbody>
</table>

### Related Information

Retiming Restrictions and Workarounds, Intel Hyperflex Architecture High-Performance Design Handbook

#### 2.5.1.3. Report Clock Transfers

The Timing Analyzer's **Reports ➤ Diagnostic ➤ Report Clock Transfers** command reports all clock-to-clock transfers in the design. The equivalent scripting command is `report_clock_transfers`.

**Report Clock Transfers** generates the Setup Transfers report and the Hold Transfers report that display data about the clock-to-clock transfers.

**Figure 49. Setup Transfers Report Shows Clock-to-Clock Transfers**

<table>
<thead>
<tr>
<th>Setup Transfers</th>
<th>Setup Transfers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Show: Visible</td>
<td>Hide</td>
</tr>
<tr>
<td>From: Clock</td>
<td>To Clock</td>
</tr>
<tr>
<td>Paths FR/ Paths RF/ Paths FF/ Paths FF</td>
<td>Clock Pair Classification</td>
</tr>
<tr>
<td>1 clk</td>
<td>clk</td>
</tr>
</tbody>
</table>
The Setup Transfers report and Hold Transfers report display all possible transfers, including rising clock edge to rising clock edge (RR), falling clock edge to rising clock edge (FR), rising clock edge to falling clock edge (RF), and falling clock edge to falling clock edge (FF) paths.

- If a path exists in the design, the report column cell is white and lists the number of paths.
- If a path is a false path, the report column cell is light gray and contains the text "false path."
- If a path does not exist in the design, then the report column cell is dark gray.

The Setup Transfers report and Hold Transfers report also lists the Worst-Case Slack for setup, the Worst-Case Operating Conditions, and the Clock Pair Classification for each clock path. The Clock Pair Classification includes the following:

<table>
<thead>
<tr>
<th>Clock Pair Classification</th>
<th>Definition</th>
</tr>
</thead>
</table>
| Intra-Clock (Timed Safe)  | • From Clock and To Clock are the same.  
                              • No timing constraint required. |
| Inter-Clock Synchronous (Timed Safe) | • From Clock and To Clock relate synchronously, and have a known phase and frequency relationship.  
                                             • Multicycle path constraint may or may not exist. |
| Asynchronous (Timed Unsafe) | • From Clock and To Clock are asynchronous.  
                                        • Timing constraints (false path, clock groups, set_max_skew) do not exist. |
| Ignored (Not Timed)       | • From Clock and To Clock are asynchronous.  
                                        • Timing constraints (false path, clock groups, set_max_skew) exist and setup and hold slack are not applicable. |

2.5.1.4. Report Logic Depth

The Timing Analyzer's Reports ➤ Design Metrics ➤ Report Logic Depth command reports the number of logic levels within a clock domain. This value typically corresponds to the number of look-up tables (LUTs) that a path passes through. The equivalent scripting command is report_design_metrics -logic_depth. Report Logic Depth shows the distribution of logic depth among the critical paths, allowing you to identify areas where you can reduce logic levels in your RTL.

Figure 50. Report Logic Depth (Histogram)
Figure 51. **Report Paths of Depth 3**  
Call report logic depth by topology for each clock, intraclock only.

![Diagram of Report Paths of Depth 3](image)

Figure 52. **Summary of Paths**  
Close timing with accurate histogram cross probing.

![Summary of Paths Table](image)

You can specify various options to customize the reporting.
Figure 53. Report Logic Depth Dialog Box

Table 10. Report Logic Depth Settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clocks</td>
<td>From Clock and To Clock filter paths in the report to show only the launching or latching clocks you specify.</td>
</tr>
<tr>
<td>Targets</td>
<td>Specifies the target node for From Clock and To Clock to report logic depth with only those endpoints. Specify an I/O or register name or I/O port for this option. The field also supports wildcard characters. When the From, To, or Through boxes are empty, the Timing Analyzer assumes all possible targets in the device. The Through option limits the report for paths that pass through combinatorial logic, or a particular pin on a cell.</td>
</tr>
<tr>
<td>Analysis type</td>
<td>The Setup, Hold, Recovery, and Removal analyses report the logic depths of the top X paths by slack. Topology analysis reports the logic depths of the top X paths by logic depth.</td>
</tr>
</tbody>
</table>
Option | Description
--- | ---
**Paths**<br>Specifies the number of paths to display by endpoint and slack level. The default value for **Report number of paths** is 10, otherwise, the report can be very long. Enable **Pairs only** to list only one path for each pair of source and destination. Limit further with **Maximum number of paths per endpoints**. You can also filter paths by entering a value in the **Maximum slack limit** field.<br><br>**Detail**<br>Specify whether to display on **Histogram** or full **Path** level of detail.<br><br>**Report panel name**<br>Specifies the name of the report panel. You can optionally enable **File name** to write the information to a file. If you append `.htm` or `.html` as a suffix, the Timing Analyzer produces the report as HTML. If you enable **File name**, you can **Overwrite** or **Append** the file with latest data.<br><br>**Tcl command**<br>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the **Console** into a Tcl file.

### 2.5.1.5. Report Neighbor Paths

The Timing Analyzer’s **Reports ➤ Design Metrics ➤ Report Neighbor Paths** command helps you to determine the root cause of critical paths (for example, high logic level, retiming limitation, sub-optimal placement, I/O column crossing, hold fix-up, time borrowing, or others). The equivalent scripting command is `report_design_metrics -neighbor_paths`.

**Figure 54. Report Neighbor Paths Report**

**Report Neighbor Paths** reports the most timing-critical paths in the design, including associated slack, additional path summary information, and path bounding boxes. **Report Neighbor Paths** shows the most timing-critical **Path Before** and **Path After** each critical **Path**. Retiming or logic balancing of the **Path** can simplify timing closure if there is negative slack on the **Path**, but positive slack on the **Path Before** or **Path After**.
# Table 11. Report Neighbor Path Dialog Box Settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clocks</strong></td>
<td>From Clock and To Clock filter paths in the report to show only the launching or latching clocks you specify.</td>
</tr>
<tr>
<td><strong>Targets</strong></td>
<td>Specifies the target node for From Clock and To Clock to report neighbor paths with only those endpoints. Specify an I/O or register name or I/O port for this option. The field also supports wildcard characters. When the From, To, or Through boxes are empty, the Timing Analyzer assumes all possible targets in the device. The Through option limits the report for paths that pass through combinatorial logic, or a particular pin on a cell.</td>
</tr>
<tr>
<td><strong>Analysis type</strong></td>
<td>The Analysis type options are Setup, Hold, Recovery, or Removal. The Timing Analyzer reports the results for the type of analysis you select.</td>
</tr>
<tr>
<td><strong>Paths</strong></td>
<td>Specifies the number of paths to display by endpoint and slack level. The default value for Report number of paths is 10, otherwise, the report can be very long. Enable Pairs only to list only one path for each pair of source and destination. Limit further with Maximum number of paths per endpoints. You can also filter paths by entering a value in the Maximum slack limit field.</td>
</tr>
<tr>
<td><strong>Report panel name</strong></td>
<td>Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data.</td>
</tr>
<tr>
<td><strong>Tcl command</strong></td>
<td>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.</td>
</tr>
<tr>
<td><strong>Extra Info</strong></td>
<td>Specifies extra info.</td>
</tr>
</tbody>
</table>
2.5.1.6. Report Register Spread

The Timing Analyzer's **Reports ➤ Design Metrics ➤ Report Register Spread** command analyzes the final placement to identify registers with sinks pulling them in various directions. These registers are potential candidates for duplication. The equivalent scripting command is `report_register_spread`.

Registers that drive in opposite directions and connect to high fan-out can have placement-warping effects on the floorplan that impact $f_{\text{MAX}}$. The placement-warping may not cause timing failures. Therefore, you can view this report to identify such registers. Taking steps to address the registers listed in the report can make placement of the design easier and improve $f_{\text{MAX}}$ performance.

You can automate duplication of registers with the `DUPLICATE_REGISTER` and `DUPLICATE_HIERARCHY_DEPTH .qsf` assignments, or you can manually modify RTL to duplicate registers or refactor logic. Refer to "Automatic Register Duplication: Hierarchical Proximity" in *Intel Quartus Prime Pro Edition User Guide: Design Optimization*.
You can specify various options to customize the report.

**Table 12. Report Register Spread Settings**

<table>
<thead>
<tr>
<th>Option</th>
<th>Available Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Spread Type</strong></td>
<td>Specifies the type of spread data in the report:</td>
</tr>
<tr>
<td></td>
<td>- <strong>Tension</strong>—reports the sum over each sink of the distance from it to the centroid of all the sinks.</td>
</tr>
<tr>
<td></td>
<td>- <strong>Span</strong>—reports the maximum 1-dimensional delta between the left bottom-most sink and the right top-most sink.</td>
</tr>
<tr>
<td></td>
<td>- <strong>Count</strong>—reports registers with the largest sink counts.</td>
</tr>
<tr>
<td><strong>Sink Type</strong></td>
<td>Specifies the type of sink in the report:</td>
</tr>
<tr>
<td></td>
<td><strong>continued...</strong></td>
</tr>
</tbody>
</table>
### Option | Available Settings
--- | ---
- **Endpoint**—the nodes (usually registers) that terminate timing paths from a register.  
- **Immediate Fanout**—the immediately connected nodes of the register. For example, lookup tables, other registers, RAM, or DSP blocks.

- **From Clock**  
  Filters paths in the report to show only the launching clocks you specify.

- **Report number of registers**  
  Specifies the number of registers to display in the report. The default value for Report number of registers is 10.

- **Report panel name**  
  Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data.

- **Tcl command**  
  Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.

### Related Information


#### 2.5.1.6.1. Registers with High Timing Path Endpoint Tension

Timing path endpoints are the nodes (usually registers) that terminate timing paths from a register. The Timing path endpoint is equivalent to the nodes that the `get_fanouts` command returns, or the overall set of nodes that appear as a "From Node" after running the `report_timing` command. Register duplication is necessary, but not always sufficient, in helping to distribute the signal more efficiently. In addition, you may need to duplicate or restructure any intermediate logic before duplicating the register.

**Figure 58. **Register A has 4 Timing Path Endpoints

Tension is the sum over each sink of the distance from the sink to the centroid of all the sinks. The value of tension is therefore dependent on the number of sinks. Register duplication can help to break up these clouds, since they may be the result of the placement solution getting "warped" by the presence of the register.
2.5.1.6.2. Registers with High Immediate Fan-Out Tension

There are two Sink Type options: Endpoint and Immediate Fanout. The immediate fan-outs are the immediately connected nodes (lookup tables, other registers, RAM or DSP blocks, and others) of the register. This fan-out is equivalent to fan-outs that the Chip Planner displays, and in various high fan-out reports. Register duplication directly distributes the immediate fan-outs of a register among the duplicates.

2.5.1.7. Report Route Net of Interest

The Timing Analyzer’s Reports ➤ Design Metrics ➤ Report Route Net of Interest command reports the nets that require the most effort from the router. The report shows the percentage of total router effort for the nets reported. The equivalent scripting command is report_route_net_of_interest.

This report identifies nets that should not require significant router effort. For example, you might expect that low speed management interface nets are not timing critical, and therefore not require much router effort. However, if Report Route Net of Interest reports that some nets in the low speed management interface require significant effort from the router, you can investigate that further. The investigation can determine whether the timing constraints are correct, whether the fan-out is significant and can reduce through driver duplication, or whether the net passes through congested areas.
Table 13. Report Route Net of Interest Settings

<table>
<thead>
<tr>
<th>Option</th>
<th>Available Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nets</td>
<td>Specifies the Maximum number of nets to report. The default value is 50.</td>
</tr>
<tr>
<td>Report panel name</td>
<td>Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data.</td>
</tr>
<tr>
<td>Tcl command</td>
<td>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.</td>
</tr>
</tbody>
</table>

2.5.1.8. Report Hierarchical Retiming Restrictions

The Timing Analyzer's Reports ➤ Design Metrics ➤ Report Hierarchical Retiming Restrictions command reports a summary of the number of Power-up "Care" Restrictions and don’t touch information for each port. You can refer to this report to
improve the circuit and remove retiming restrictions that limit circuit performance. `report_hierarchical_retiming_restrictions` is the equivalent scripting command.

**Figure 63. Report Hierarchical Retiming Restrictions Report**

<table>
<thead>
<tr>
<th>Compilation Hierarchy Node</th>
<th>Power-up <em>Care</em> Restriction Asynchronous clear port Drives an asynchronous signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>384 [172]</td>
</tr>
<tr>
<td>1</td>
<td>LED</td>
</tr>
<tr>
<td>2</td>
<td>add_0</td>
</tr>
<tr>
<td>3</td>
<td>add_1</td>
</tr>
<tr>
<td>4</td>
<td>clk</td>
</tr>
</tbody>
</table>

For table entries with two number values, the number in parentheses indicates the number of retiming restrictions in the specific entity alone. The number listed outside of parentheses indicates the number of retiming restrictions in the specific entity and all of its sub-entities in the hierarchy.

### 2.5.1.9. Report Reset Statistics

The Timing Analyzer’s `Reports ➤ Design Metrics ➤ Report Reset Statistics` command reports the numbers of synchronous and asynchronous resets in the design. Minimizing FFs that need to be reset helps timing closure by reducing circuit dependencies and by reducing high fanout nets. This report helps you identify potential places to remove resets.

**Figure 64. Report Reset Statistics**

Shows the number of sync and async resets and total number of registers hierarchically

### 2.5.1.10. Report Pipelining Information

The Timing Analyzer’s `Reports ➤ Design Metrics ➤ Report Pipelining Information` command generates a report that can help you identify potential areas of over-pipelining in your design. Excessive pipelining unnecessarily consumes area. The equivalent scripting command is `report_pipelining_info`.
2. Using the Intel Quartus Prime Timing Analyzer

Figure 65. Report Pipelining Information Report

<table>
<thead>
<tr>
<th>Full Hierarchy Name</th>
<th>Clock Name</th>
<th>Recommended Pipeline Stage Adjustment Across Bus</th>
<th>Minimum Total Slack of One Bit Across Bus</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>GE100_2[0]</td>
<td>j11</td>
<td>1.3035</td>
<td>1.520</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>1.348</td>
<td>1.568</td>
<td></td>
</tr>
<tr>
<td>GE100_3[0]</td>
<td>j11</td>
<td>0.736</td>
<td>1.456</td>
<td></td>
</tr>
<tr>
<td>GE100_1[0]</td>
<td>j11</td>
<td>10.001</td>
<td>1.566</td>
<td></td>
</tr>
<tr>
<td>GE100_2[0]</td>
<td>j11</td>
<td>12.683</td>
<td>1.585</td>
<td></td>
</tr>
<tr>
<td>[2]_LPD[0]</td>
<td>j11</td>
<td>0.673</td>
<td>1.794</td>
<td></td>
</tr>
<tr>
<td>[0]_LPD[0]</td>
<td>j11</td>
<td>0.222</td>
<td>1.784</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>8.420</td>
<td>1.684</td>
<td></td>
</tr>
<tr>
<td>GE100_1[0]</td>
<td>j11</td>
<td>8.735</td>
<td>1.747</td>
<td></td>
</tr>
<tr>
<td>[1]_LPD[0]</td>
<td>j11</td>
<td>0.193</td>
<td>1.618</td>
<td></td>
</tr>
<tr>
<td>GE100_1[0]</td>
<td>j11</td>
<td>9.537</td>
<td>1.509</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>10.200</td>
<td>1.700</td>
<td></td>
</tr>
<tr>
<td>GE100_1[0]</td>
<td>j11</td>
<td>5.299</td>
<td>0.703</td>
<td></td>
</tr>
<tr>
<td>DOR4_0[0]</td>
<td>j11</td>
<td>4.216</td>
<td>1.205</td>
<td></td>
</tr>
<tr>
<td>DOR4_0[0]</td>
<td>j11</td>
<td>2.908</td>
<td>1.096</td>
<td></td>
</tr>
<tr>
<td>DOR4_0[0]</td>
<td>j11</td>
<td>4.717</td>
<td>1.572</td>
<td></td>
</tr>
<tr>
<td>DOR4_0[0]</td>
<td>j11</td>
<td>4.277</td>
<td>1.425</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>2.200</td>
<td>1.160</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>4.152</td>
<td>1.427</td>
<td></td>
</tr>
<tr>
<td>GE100_0[0]</td>
<td>j11</td>
<td>2.480</td>
<td>1.240</td>
<td></td>
</tr>
<tr>
<td>GE100_2[0]</td>
<td>j11</td>
<td>3.076</td>
<td>1.538</td>
<td></td>
</tr>
</tbody>
</table>

Figure 66. Report Detailed Pipelining
The detailed report shows every single register inside the bus chain in a tree structure. Over- or under-pipelining recommendations are in the main report. Shows every single register inside the bus chain in a tree structure.

To help identify potential over-pipelining, Report Pipelining Information reports:

- The recommended pipeline stage adjustment across bus
- The minimum total slack of one bit across bus
- The minimum average slack of one bit across bus
- The distance between the registers
- The width of buses in your design
- The number of sequential registers
- The number of registers on the bus

The Recommended Pipeline Stage Adjustment Across Bus reports the number of registers that you can remove from the bus for each bit.

The Average Distance Per Stage, Max Distance Per Stage, and Min Distance Per Stage columns report the Manhattan distance measured in logic array blocks (LABs). The Bus Average Depth, Bus Max Depth, and Bus Min Depth columns report the number of sequential, single fan-out registers.

For registers that have more than one clock source, the report lists the fastest one.

The \textbf{1+} sign under Recommended Pipeline Stage Adjustment Across Bus column means that the bus might need to add more registers to meet timing requirement. Refer to the Fast Forward Timing Closure Recommendations report.
If the report identifies a large register chain with multiple sequential registers, and the distance between registers is low, that condition can suggest over-pipelining. You may be able to remove some registers to recover some of the device area and reduce congestion.

The following options are available for this report:

**Table 14. Report Pipelining Information Settings**

<table>
<thead>
<tr>
<th>Option</th>
<th>Available Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pipeline</td>
<td>Specifies the thresholds for reporting a register pipeline. You can define the Minimum average bus depth, the Minimum bus width, and the Maximum number of rows that the report includes.</td>
</tr>
<tr>
<td>Report panel name</td>
<td>Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data.</td>
</tr>
<tr>
<td>Tcl command</td>
<td>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.</td>
</tr>
</tbody>
</table>

**Figure 68. Report Pipelining Information Dialog Box**

2.5.1.11. Report Asynchronous CDC

The Timing Analyzer’s **Reports ➤ Custom Reports ➤ Report Asynchronous CDC** command classifies and reports all asynchronous clock-domain-crossing (CDC) transfers in your design. Asynchronous CDCs include single-bit transfers, multibit transfers, and asynchronous reset CDCs. Designs often contain unintended CDCs or transfers that you intend to be CDCs but the Timing Analyzer does not recognize them. Use this report to ensure that the Timing Analyzer correctly detects all CDCs.
Figure 69. **Report Asynchronous CDC Dialog Box**

Table 15. **Report Asynchronous CDC Information Settings**

<table>
<thead>
<tr>
<th>Option</th>
<th>Available Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Clocks</strong></td>
<td>Filters the report to only show CDCs that originate from <strong>From clock</strong> and terminate at <strong>To clock</strong>.</td>
</tr>
<tr>
<td><strong>Targets</strong></td>
<td>Filters the report to only show CDCs that originate from <strong>From</strong> register and terminate at <strong>To</strong> register. Both the <strong>From</strong> and <strong>To</strong> must be registers. This option is optional with the <strong>Clocks</strong> option.</td>
</tr>
<tr>
<td><strong>Entries</strong></td>
<td>Limits the number of entries that are reported per CDC category</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Option</th>
<th>Available Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detail</td>
<td>Chooses whether to show a summary of all CDC’s or give detail on each individual CDC</td>
</tr>
<tr>
<td>CDC Categories</td>
<td>Specifies the CDC categories to be reported.</td>
</tr>
<tr>
<td>Report panel name</td>
<td>Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can overwrite or append the file with latest data.</td>
</tr>
<tr>
<td>Tcl command</td>
<td>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.</td>
</tr>
</tbody>
</table>

Figure 70. Report Asynchronous CDC summary view

<table>
<thead>
<tr>
<th>CDC Type</th>
<th>CDC Count</th>
<th>Total Transfer Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-bit CDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unsynchronized Transfer</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>Unconstrained Synchronizer</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Synchronizer Dri...le Clock Domains</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Intra-Clock False Path Synchronizer</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Synchronizer Not...ected for MTBF</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Compliant Synchronizer</td>
<td>11</td>
<td>11</td>
</tr>
<tr>
<td>Transfer Precede...binational Logic</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Multi-bit CDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unconstrained CE-type CDC Bus</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Compliant CE-type CDC Bus</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>Unconstrained MUX-type CDC Bus</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Compliant MUX-type CDC Bus</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Unsynchronized Synchronizer Bus</td>
<td>2</td>
<td>8</td>
</tr>
<tr>
<td>Unconstrained Synchronizer Bus</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Compliant Synchronizer Bus</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>Synchronizer Bu... Uneven Lengths</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Synchronizer afte...th Control Signal</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Asynchronous Reset CDC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unsynchronized Reset Synchronizer</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Unconstrained Reset Synchronizer</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Reset Synchroniz...Multiple Sources</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Inactive Reset Synchronizer</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The summary view of the Asynchronous CDC Report provides an overview of the number of CDC’s that fall into each category in your design. CDC Count gives the number of topologies detected for a category. Total Transfer Width shows the total number of CDC crossings for a category. This value is different than CDC Count for multibit CDC’s because each topology consists of multiple crossings.
Figure 71. Report Asynchronous CDC Full View

<table>
<thead>
<tr>
<th>CDC Type</th>
<th>Source Nodes</th>
<th>Destination Nodes</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Single-bit CDC</td>
<td>unsynct_chain[src_reg] unsynct_c...</td>
<td>unsynct_c...[synch_reg]</td>
<td>clk[4]</td>
</tr>
<tr>
<td>2 Unsynchronized Transfer (5)</td>
<td>chain_with...[out][src_reg] chain...</td>
<td>chain_with...[synch_reg]</td>
<td>clk[4]</td>
</tr>
<tr>
<td>4 Intra-Clock False Path Synchronizer (2)</td>
<td>intra_clock...[t_chains][rst1] intra_clock...[t_chains][rst2]</td>
<td>intra_clock...[t_chains][rst2]</td>
<td>clk[3]</td>
</tr>
<tr>
<td>6 Compliant Synchronizer (11)</td>
<td>Transfer Preceded by National Logic (0)</td>
<td>Multi-bit CDC</td>
<td></td>
</tr>
<tr>
<td>7 Multi-bit CDC</td>
<td>unconstrain...[e][bus_src[<em>]] unconstrain...[bus_dst[</em>]]</td>
<td>unconstrain...[bus_dst[*]]</td>
<td>clk[0]</td>
</tr>
<tr>
<td>2 Unconstrained CE-type CDC Bus (2)</td>
<td>unscons_one...[bus_src[<em>]] unscons_one...[bus_dst[</em>]]</td>
<td>unscons_one...[bus_dst[*]]</td>
<td>clk[0]</td>
</tr>
<tr>
<td>2 Compliant CE-type CDC Bus (2)</td>
<td>proper_ce[bus_src[<em>]] proper_ce[bus_dst[</em>]]</td>
<td>proper_ce[bus_dst[*]]</td>
<td>clk[0]</td>
</tr>
<tr>
<td>2 one_bit_ce...[bus_src] one_bit_ce...[bus_dst]</td>
<td>one_bit_ce...[bus_dst]</td>
<td>one_bit_ce...[bus_dst]</td>
<td>clk[0]</td>
</tr>
</tbody>
</table>

The full view of the Asynchronous CDC report shows the source and destination registers and clocks for each detected CDC topology in your design. You may click on any row of this report. Clicking on a row that contains the name of a CDC category brings up the description for that category and associated Design Assistant rules that check for such topologies. Clicking on a row that contains a CDC brings up detailed information on that CDC in the **CDC Statistics** table. The information available varies depending on the topology of the CDC.
Figure 72. Statistics table showing detailed information on each CDC

<table>
<thead>
<tr>
<th>Unsynchronized Transfer #4</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDC Statistics</td>
</tr>
<tr>
<td>Property</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

2.5.1.12. Report CDC Viewer

The Timing Analyzer’s **Reports ➤ Diagnostic ➤ Report CDC Viewer** command displays the Clock Domain Crossing (CDC) Viewer. The CDC Viewer graphically displays the setup, hold, recovery, or removal analysis of all clock transfers in your design. The equivalent scripting command is `report_cdc_viewer`.

You can specify the following options to customize CDC Viewer reporting:

Table 16. **Setup Transfers Report Controls**

<table>
<thead>
<tr>
<th>Control</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>From Clock: and To Clock:</td>
<td>Filters the display according to the clock names you specify. Click From Clock: or To Clock: to search for specific clock names.</td>
</tr>
<tr>
<td>Legend</td>
<td>Defines the status colors. A color coded grid displays the clock transfer status. The clock headers list each clock with transfers in the design. The GUI truncates long clock names, but you can view the full name in a tool tip or by resizing the clock header cell. The GUI...</td>
</tr>
<tr>
<td>Control</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td></td>
<td>represents the generated clocks as children of the parent clock. A ‘+’ icon next to a clock name indicates the presence of generated clocks. Clicking on the clock header displays the generated clocks associated with that clock.</td>
</tr>
</tbody>
</table>

**Toggle Data**

The text in each transfer cell contains data specific to each transfer. Turn on or off display of the following types of data:

- **Number of timed endpoints** between clocks— the number of timed, endpoint-unique paths in the transfer. A path being “timed” means that analysis occurs on that path. Only paths with unique endpoints count towards this total.
- **Number of cut endpoints** between clocks— the number of cut endpoint-unique paths, instead of timed paths. These paths are cut by either a false path or clock group assignment. Timing analysis skips such paths.
- **Worst-case slack** between clocks— the worst-case slack among all endpoint-unique paths in the transfer.
- **Total negative slack** between clocks— the sum of all negative slacks among all endpoint-unique paths in this transfer.
- **Tightest relationship** between clocks— the lowest-value setup, hold, recovery, or removal relationship between the two clocks in this transfer.

**Show Filters** and **Show Legend**

Turns on or off Filters and Legend.

---

**Figure 73. CDC Viewer Setup Transfers Report**

![CDC Viewer Setup Transfers Report](image)

Send Feedback
Each block in the grid is a transfer cell. Each transfer cell uses color and text to display important details of the paths in the transfer. The color coding represents the following states:

**Table 17. Transfer Cell Content**

<table>
<thead>
<tr>
<th>Cell Color</th>
<th>Color Legend</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black</td>
<td>Indicates no transfers. There are no paths crossing between the source and destination clock of this cell.</td>
</tr>
<tr>
<td>Green</td>
<td>Indicates passing timing. All timing paths in this transfer, that have not been cut, meet their timing requirements.</td>
</tr>
<tr>
<td>Red</td>
<td>Indicates failing timing. One or more of the timing paths in the transfer do not meet their timing requirements. If the transfer is between unrelated clocks, the paths likely require a synchronizer chain.</td>
</tr>
<tr>
<td>Blue</td>
<td>Indicates clock groups. The source and destination clocks of these transfers are cut by means of asynchronous clock groups.</td>
</tr>
<tr>
<td>Gray</td>
<td>Indicates a cut transfer. All paths in this transfer are cut by false paths. Therefore, timing analysis does not consider these paths.</td>
</tr>
<tr>
<td>Orange</td>
<td>Indicates inactive clocks. One of the clocks in the transfer is an inactive clock (with the set_active_clocks command). The Timing Analyzer ignores such transfers.</td>
</tr>
</tbody>
</table>

Right-click menus allow you to perform operations on transfer cells and clock headers. When the operation is a Timing Analyzer report or SDC command, a dialog box opens containing the contents of the transfer cell.

**Table 18. Transfer Cell Right-Click Menus**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copy</td>
<td>Copies the contents of the transfer cell or clock header to the clipboard.</td>
</tr>
<tr>
<td>Report Timing</td>
<td>Reports timing. Not available for transfer cells with no valid paths (gray or black cells).</td>
</tr>
<tr>
<td>Report Endpoints</td>
<td>Reports endpoints. Not available for transfer cells with no cut paths (gray or black cells).</td>
</tr>
<tr>
<td>Report False Path</td>
<td>Reports false paths. Not available for transfer cells with no valid paths (black cells).</td>
</tr>
<tr>
<td>Report Exceptions</td>
<td>Reports exceptions. Only available for clock group transfers (blue cells).</td>
</tr>
<tr>
<td>Report Exceptions (with clock groups)</td>
<td>Reports exceptions with clock groups. Only available for clock group transfers (blue cells).</td>
</tr>
<tr>
<td>Set False Path</td>
<td>Sets a false path constraint.</td>
</tr>
<tr>
<td>Set Multicycle Path</td>
<td>Sets a multicycle path exception.</td>
</tr>
<tr>
<td>Set Min Delay</td>
<td>Sets a min delay constraint.</td>
</tr>
<tr>
<td>Set Max Delay</td>
<td>Sets a max delay constraint.</td>
</tr>
<tr>
<td>Set Clock Uncertainty</td>
<td>Sets a clock uncertainty constraint.</td>
</tr>
</tbody>
</table>

**Table 19. Clock Header Right-Click Menus**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copy (include children)</td>
<td>Copies the name of the clock header, and the names of each of its derived clocks. This option only appears for clock headers with generated clocks.</td>
</tr>
<tr>
<td>Expand/Collapse All Rows/Columns</td>
<td>Shows or hides all derived clocks in the grid.</td>
</tr>
</tbody>
</table>
You can view CDC Viewer output in any of the following formats:

- A report panel in the Timing Analyzer
- Output in the Timing Analyzer Tcl console
- A plain-text file
- An HTML file you can view in a web browser.

### 2.5.1.13. Report Custom CDC Viewer Command

The Timing Analyzer’s **Report Custom CDC Viewer** command allows you to configure and display a custom clock domain crossing report. This report displays the results of setup, hold, recovery, and removal checks on clock domain crossing transfers. The equivalent scripting command is `report_cdc_viewer`.

The following options are available for this report:

**Table 20. Report Clock Domain Crossing Viewer Settings**

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clocks</td>
<td>From Clock and To Clock filter paths in the report to show only the launching or latching clocks you specify.</td>
</tr>
<tr>
<td>Analysis type</td>
<td>Options are Setup, Hold, Recovery, or Removal. The Timing Analyzer reports the results for the type of analysis you select.</td>
</tr>
<tr>
<td>Transfers</td>
<td>Specifies the type of clock transfers to include or exclude from the report, including Timed transfers, Fully cut transfers, Clock groups, Inactive clocks, and Non-crossing transfers. You can specify the Maximum slack limit and Grid options for the report.</td>
</tr>
<tr>
<td>Detail level</td>
<td>Full shows all details of the report and Summary filters the details and shows summary data.</td>
</tr>
<tr>
<td>Report panel name</td>
<td>Specifies the name of the report panel. You can optionally enable File name to write the information to a file. If you append .htm or .html as a suffix, the Timing Analyzer produces the report as HTML. If you enable File name, you can Overwrite or Append the file with latest data, and specify Grid or List format. Note: In grid format reports, clocks with non-crossing transfers always appear if they have transfers between other clocks.</td>
</tr>
<tr>
<td>Tcl command</td>
<td>Displays the Tcl syntax that corresponds with the GUI options you select. You can copy the command from the Console into a Tcl file.</td>
</tr>
</tbody>
</table>

### 2.5.1.14. Report Time Borrowing Data

You can run the Timing Analyzer’s **Report Time Borrowing Data** command to view time borrowing data. The equivalent scripting command is `report_timing` (with specific arguments).
The Timing Analyzer reports time borrowing data for the **Data Arrival Path** or **Data Required Path**, according to whether borrowing occurs at the destination or the source.

**Figure 74. Report for Time Borrowing At Destination**

The following report shows 100ps borrowed on the Data Required path. The setup slack improves on incoming paths, at the expense of worse setup slack for outgoing paths.

**Figure 75. Report for Time Borrowing At Source**

The following report shows 100ps borrowed on the Data Arrival Path, worsening the setup relationship for the outgoing path.

**Related Information**

[Timing Borrowing on page 17](#)

### 2.5.2. Cross-Probing with Design Assistant

The Intel Quartus Prime Design Assistant can automatically report any violations against a standard set of Intel FPGA-recommended design guidelines during stages of compilation. You can specify which rules you want the Design Assistant to check in your design, and customize the severity levels, thus eliminating or waiving rule checks that are not important for your design.

When you run Design Assistant during compilation, Design Assistant utilizes the in-flow (transient) data that generates during compilation to check for rule violations.

When you run Design Assistant in analysis mode from the Timing Analyzer, Design Assistant performs design rule checks using the static compilation snapshot data that you load.

Some Design Assistant rule violations allow cross-probing into the related timing analysis data. Cross-probing can help you to more quickly identify the root cause and resolve any Design Assistant rule violations. For example, for a path with a setup analysis violation, you can cross-probe into the Timing Analyzer to identify the edge that has delay added for hold time.

**Note:** You must run the Compiler through at least the Plan stage before you can cross-probe to Timing Analyzer.
2.5.2.1. Cross-Probing from Design Assistant to Timing Analyzer

Some Design Assistant rule violations allow cross-probing into Timing Analyzer. Follow these steps to cross-probe from such Design Assistant rule violations to the Timing Analyzer.

1. Compile the design through at least the Compiler’s Plan stage.
2. Locate a rule violation in the Design Assistant folder of the Compilation Report.
3. Right-click the rule violation to display any Report Timing commands available for the violation.

**Figure 76. Cross Probing from Design Assistant Rule TMC-20210 Violations to Timing Analyzer**

2.5.3. Launching Design Assistant from Timing Analyzer

You can run Design Assistant directly from the Timing Analyzer to assist when optimizing timing paths and other timing conditions. When you launch Design Assistant from the Timing Analyzer, Design Assistant is preset to check only rules that relate to timing analysis.

Follow these steps to run the Design Assistant from the Timing Analyzer:

1. Compile the design through at least the Compiler's Plan stage.
2. Open the Timing Analyzer for the Compiler stage from the Compilation Dashboard.
3. In the Timing Analyzer, click Reports ➤ Design Assistant ➤ Report DRC. The Report DRC (design rule check) dialog box opens.
4. Under Rules, disable any rules that are not important to your analysis by removing the check mark.
5. Consider whether to adjust rule parameter values in the Parameters field.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic Margin</td>
<td>-0.690</td>
</tr>
<tr>
<td>Max Fanout</td>
<td>1</td>
</tr>
<tr>
<td>Source/Destination Bounding Box</td>
<td>(225, 63) - (225, 63)</td>
</tr>
<tr>
<td>Cell Bounding Box</td>
<td>(225, 63) - (225, 63)</td>
</tr>
<tr>
<td>Interconnect Bounding Box</td>
<td>(225, 63) - (225, 63)</td>
</tr>
<tr>
<td>Source/Destination Relative Area</td>
<td>1.000</td>
</tr>
<tr>
<td>Cell Relative Area</td>
<td>1.000</td>
</tr>
<tr>
<td>Interconnect Relative Area</td>
<td>1.000</td>
</tr>
<tr>
<td>Retiming Restriction From Node</td>
<td>Node is in a block that cannot be retimed.</td>
</tr>
<tr>
<td>Retiming Restriction To Node</td>
<td>--</td>
</tr>
<tr>
<td>From Node is Po...Up &quot;Don't Care&quot;</td>
<td>Yes</td>
</tr>
<tr>
<td>To Node is Power-Up &quot;Don't Care&quot;</td>
<td>Yes</td>
</tr>
<tr>
<td>From Node is not fully-registered RAM with unregistered outputs</td>
<td>--</td>
</tr>
<tr>
<td>Max Borrow Time From Node</td>
<td>0.000</td>
</tr>
<tr>
<td>Route Stage Congestion Impact</td>
<td>--</td>
</tr>
<tr>
<td>Estimated Delay Added for Hold</td>
<td>0.000</td>
</tr>
</tbody>
</table>
6. Confirm the **Report panel name** and optionally specify an output **File name**.

7. Click **Run**. The Results reports generate and appear in the **Report** pane, as well as the main Compilation Report.

### Figure 79. Design Assistant Reports in Timing Analyzer Report Pane

#### 2.5.4. Locating Timing Paths in Other Tools

You can locate from paths and elements in the Timing Analyzer to other visualization tools in the Intel Quartus Prime software, such as the Chip Planner, Technology Map Viewer, or Resource Property Viewer.

You can right-click most paths or node names in the Timing Analyzer reports and click the **Locate Node** or **Locate Path** commands. Use these commands in the Timing Analyzer GUI or the `locate` command in the Tcl console to locate to that node in other Intel Quartus Prime tools.
The following examples show how to locate the ten paths with the worst timing slack from Timing Analyzer to the Technology Map Viewer, and locate all ports matching data* in the Chip Planner.

**Example 1. Locating from the Timing Analyzer**

```
# Locate in the Technology Map Viewer the ten paths with the worst slack
locate [get_timing_paths -npaths 10] -tmv
# locate all ports that begin with data in the Chip Planner
locate [get_ports data*] -chip
```

**2.5.5. Correlating Constraints to the Timing Report**

Understanding how timing constraints and violations appear in the timing analysis reports is critical to understanding the results. The following examples show how specific constraints impact the timing analysis reports. Most timing constraints only affect the clock launch and latch edges. Specifically, `create_clock` and `create_generated_clock` create clocks with default relationships. However, the `set_multicycle_path` exception modifies the default setup and hold relationships. The `set_max_delay` and `set_min_delay` constraints are low-level overrides that explicitly indicate the maximum and minimum delays for the launch and latch edges.

The figures show the results of running **Report Timing** on a particular path.

In the following example, the design includes a clock driving the source and destination registers with a period of 10 ns. This results in a setup relationship of 10 ns (launch edge = 0 ns, latch edge = 10ns) and hold relationship of 0 ns (launch edge = 0 ns, latch edge = 0 ns) from the command:

```
create_clock -name clocktwo -period 10.000 [get_ports {clk2}]
```
The `set_multicycle_path` constraint adds multicycles to relax the setup relationship, or open the window, making the setup relationship 20 ns while the hold relationship is still 0 ns:

```bash
set_multicycle_path -from clocktwo -to clocktwo -setup -end 2
set_multicycle_path -from clocktwo -to clocktwo -hold -end 1
```
The `set_max_delay` and `set_min_delay` constraints explicitly override the setup relationship. Note that the only thing changing for these different constraints are the launch edge time and latch edge times for setup and hold analysis. Every other line item comes from delays inside the FPGA and are static for a given fit. View these reports to analyze how your constraints affect the timing reports.

For I/O, you must add `set_input_delay` and `set_output_delay` constraints. These constraints describe delays on signals from outside of the FPGA design that connect to the design's I/O ports. The values of these constraints are the delays of the external signals between an external register and a port on the design. The `-clock` argument to the `set_input_delay` and `set_output_delay` specifies the clock domain that the external signal belongs to, or rather, the clock domain of the external register connected to the I/O port. The `-min` and `-max` options specify the worst-case or best-case delay; not specifying either option causes the worst- and best-case delays to be equal. I/O delays display as `iExt` or `oExt` in the Type column.
example is an output port with a `set_output_delay -max 1.0` and `set_output_delay -min -0.5`. Refer to "Creating Virtual Clocks" and "Creating I/O Constraints" for more information.

**Figure 84. Using `set_min_delay`**

A clock relationship, which is the difference between the launching and latching clock edge of a transfer, is determined by the clock waveform, multicycle constraints, and minimum and maximum delay constraints. The Timing Analyzer also adds the value of `set_output_delay` as an `oExt` value. For outputs this value is part of the **Data Required Path**, since this is the external part of the analysis. The setup report subtracts the `-max` value, making the setup relationship harder to meet, since the **Data Arrival Path** must be shorter than the **Data Required Path**. The Timing Analyzer also subtracts the `-min` value. This subtraction is why a negative number causes more restrictive hold timing. The **Data Arrival Path** must be longer than the **Data Required Path**.

**Related Information**
- Relaxing Setup with Multicycle (**set_multicycle_path**) on page 99
- Creating Virtual Clocks on page 79
- Creating I/O Constraints on page 90
2.6. Applying Timing Constraints

The following section describes correct application of SDC timing constraints that guide Fitter placement and allow accurate timing analysis. You can create an .sdc file with a set of initial recommended constraints, and then iteratively modify those constraints as the design progresses.

2.6.1. Recommended Initial SDC Constraints

Include the following basic SDC constraints in your initial .sdc file. The following example shows application of the recommended initial SDC constraints for a simple dual-clock design:

```
create_clock -period 20.00 -name adc_clk [get_ports adc_clk]
create_clock -period 8.00 -name sys_clk [get_ports sys_clk]
derive_pll_clocks
derive_clock_uncertainty
```

**Note:** Only Intel Arria 10 and Intel Cyclone® 10 GX devices support the Derive PLL Clocks (derive_pll_clocks) constraint. For all other supported devices, the Timing Analyzer automatically derives PLL clocks from constraints bound to the related IP.

**Create Clock (create_clock) on page 68**

**Derive PLL Clocks (derive_pll_clocks) on page 69**

**Derive Clock Uncertainty (derive_clock_uncertainty) on page 70**

**Set Clock Groups (set_clock_groups) on page 70**

2.6.1.1. Create Clock (create_clock)

The **Create Clock** (create_clock) constraint allows you to define the properties and requirements for a clock in the design. You must define clock constraints to determine the performance of your design and constrain the external clocks coming into the FPGA. You can enter the constraints in the Timing Analyzer GUI, or in the .sdc file directly.

You specify the **Clock name** (-name), clock **Period** (-period), rising and falling **Waveform edge** values (-waveform), and the target signal(s) to which the constraints apply.

The following command creates the sys_clk clock with an 8ns period, and applies the clock to the fpga_clk port:

```
create_clock -name sys_clk -period 8.0 \[get_ports fpga_clk]
```

**Note:** Tcl and .sdc files are case-sensitive. Ensure that references to pins, ports, or nodes match the case of names in your design.

By default, the clock has a rising edge at time 0 ns, a 50% duty cycle, and a falling edge at time 4 ns. If you require a different duty cycle, or to represent an offset, specify the -waveform option.
Typically you name a clock with the same name as the port you assign. In the example above, the following constraint accomplishes this:

```
create_clock -name fpga_clk -period 8.0 [get_ports fpga_clk]
```

There are now two unique objects called `fpga_clk`, a port in your design and a clock applied to that port.

**Note:**
In Tcl syntax, square brackets execute the command inside them. `[get_ports fpga_clk]` executes a command that finds and returns a collection of all ports in the design that match `fpga_clk`. You can enter the command without using the `get_ports` collection command, as shown in the following example:

```
create_clock -name sys_clk -period 8.0 fpga_clk
```

**Warning:**
Constraints that you define in the Timing Analyzer apply directly to the timing database, but do not automatically transfer to the `.sdc` file. Click **Write SDC File** on the Timing Analyzer **Tasks** pane to preserve constraints changes from the GUI in an `.sdc` file.

**Related Information**
Creating Base Clocks on page 77

### 2.6.1.2. Derive PLL Clocks (derive_pll_clocks)

The **Derive PLL Clocks** (`derive_pll_clocks`) constraint automatically creates clocks for each output of any PLL in your design.

**Note:**
Only Intel Arria 10 and Intel Cyclone 10 GX devices support the **Derive PLL Clocks** (`derive_pll_clocks`) constraint. For all other supported devices, the Timing Analyzer automatically derives PLL clocks from constraints bound to the related IP.

The constraint can generate multiple clocks for each output clock pin if the PLL is using clock switchover: one clock for the `inclk[0]` input clock pin, and one clock for the `inclk[1]` input clock pin. Specify the **Create base clocks** (`create_base_clocks`) option to create base clocks on the inputs of the PLLs by default. By default the clock name is the same as the output clock pin name, or specify the **Use net name as clock name** (`-use_net_name`) option to use the net name.

```
create_clock -period 10.0 -name fpga_sys_clk [get_ports fpga_sys_clk] \
    derive_pll_clocks
```

When you create PLLs, you must define the configuration of each PLL output. This definition allows the Timing Analyzer to automatically constrain the PLLs with the `derive_pll_clocks` command. This command also constrains transceiver clocks and adds multicycles between LVDS SERDES and user logic.

The `derive_pll_clocks` command prints an Info message to show each generated clock the command creates.

As an alternative to `derive_pll_clocks` you can copy-and-paste each `create_generated_clock` assignment into the `.sdc` file. However, if you subsequently modify the PLL setting, you must also change the generated clock
constraint in the .sdc file. Examples of this type of change include modifying an existing output clock, adding a new PLL output, or making a change to the PLL's hierarchy. Use of derive_pll_clocks eliminates this requirement.

**Related Information**
- Creating Base Clocks on page 77
- Deriving PLL Clocks on page 83

### 2.6.1.3. Derive Clock Uncertainty (derive_clock_uncertainty)

The **Derive Clock Uncertainty** (derive_clock_uncertainty) constraint applies setup and hold clock uncertainty for clock-to-clock transfers in the design. This uncertainty represents characteristics like PLL jitter, clock tree jitter, and other factors of uncertainty.

You can enable the **Add clock uncertainty assignment** (-add) to add clock uncertainty values from any **Set Clock Uncertainty** (set_clock_uncertainty) constraint. You can **Overwrite existing clock uncertainty assignments** (-overwrite) any set_clock_uncertainty constraints.

```bash
create_clock -period 10.0 -name fpga_sys_clk [get_ports fpga_sys_clk] 
   derive_clock_uncertainty -add -overwrite
```

The Timing Analyzer generates an information message if you omit derive_clock_uncertainty from the .sdc file.

**Related Information**
- Accounting for Clock Effect Characteristics on page 88

### 2.6.1.4. Set Clock Groups (set_clock_groups)

The **Set Clock Groups** (set_clock_groups) constraint allows you to specify which clocks in the design are unrelated. By default, the Timing Analyzer assumes that all clocks with a common base or parent clock are related, and that all transfers between those clock domains are valid for timing analysis. You can exclude transfers between specific clock domains from timing analysis by cutting clock groups.

Conversely, clocks without a common parent or base clock are always unrelated, but timing analysis includes the transfers between such clocks, unless those clocks are in different clock groups (or if all of their paths are cut with false path constraints).

You define the clock signals to include in each Group (-group), then specify the relationship between different groups, Then specify whether the groups are **Logically exclusive** (-logically_exclusive), **Physically exclusive** (-physically_exclusive), or **Asynchronous** (-asynchronous) from one another.

```bash
set_clock_groups -asynchronous -group {<clock1>...<clockn>} ... 
   -group {<clocka>...<clockn>}
```
• **-logically_exclusive**—defines clocks that are logically exclusive and not active at the same time, such as multiplexed clocks

• **-physically_exclusive**—defines clocks that that cannot be physically on the device at the same time.

• The **-asynchronous**—defines completely unrelated clocks that have different ideal clock sources. This flag means the clocks are both switching, but not in a way that can synchronously pass data.

For example, if there are paths between an 8ns clock and 10ns clock, even if the clocks are completely asynchronous, the Timing Analyzer attempts to meet a 2ns setup relationship between these clocks, unless you specify that they are not related.

Although the Set Clock Groups dialog box only permits two clock groups, you can specify an unlimited number of -group {<group of clocks>} options in the .sdc file. If you omit an unrelated clock from the assignment, the Timing Analyzer acts conservatively and analyzes that clock in context with all other domains to which the clock connects.

The Timing Analyzer does not currently analyze crosstalk explicitly. Instead, the timing models use extra guard bands to account for any potential crosstalk-induced delays. The Timing Analyzer treats the -asynchronous and -exclusive options the same for crosstalk-related analysis, but treats asynchronous and exclusive clock groups differently for things like max skew reporting and synchronizer detection.

A clock cannot be within multiple groups (-group) in a single assignment; however, you can have multiple set_clock_groups assignments.

Another way to cut timing between clocks is to use set_false_path. To cut timing between sys_clk and dsp_clk, you can use:

```
set_false_path -from [get_clocks sys_clk] -to [get_clocks dsp_clk]
set_false_path -from [get_clocks dsp_clk] -to [sys_clk]
```

This technique is effective if there are only a few clocks, but can become unmanageable with a large number of constraints. In a simple design with three PLLs that have multiple outputs, the set_clock_groups can cut timing between clocks with less than ten lines, but the set_false_path command may require more than 50 lines.

**Related Information**

• Creating Generated Clocks (create_generated_clock) on page 80

• Relaxing Setup with Multicycle (set_multicycle_path) on page 99

• Accounting for a Phase Shift (-phase) on page 100

### 2.6.2. SDC File Precedence

You must add any .sdc file that you create to the project to be read during fitting and timing analysis. The Fitter and the Timing Analyzer process .sdc files in the order they appear in the .qsf. If no .sdc appears in the .qsf, the Intel Quartus Prime software searches for an .sdc with the name <current revision>.sdc in the project directory.
Click Settings ➤ Timing Analyzer to add, remove, or change the processing order of .sdc files in the project, as Step 1: Specify Timing Analyzer Settings on page 23 describes.

If you use the Intel Quartus Prime Text Editor to create an .sdc file, the option to Add file to the project enables by default when you save the file. If you use any other editor to create an .sdc file, you must add the file to the project.

The .sdc file must contain only timing constraint commands. Tcl commands to manipulate the timing netlist or control the compilation must be in a separate Tcl script.

Note: If you type the read_sdc command at the command line without any arguments, the Timing Analyzer reads constraints embedded in HDL files, then reads the .sdc files following the .sdc file precedence order.

2.6.3. Modifying Iterative Constraints

Iteratively modify .sdc constraints and reanalyze the timing results to ensure that you have the optimum constraints for your design.

1. Click Tools ➤ Timing Analyzer.
2. Generate the reports you want to analyze. Double-click Report All Summaries under Macros to generate setup, hold, recovery, and removal summaries, summaries for supported reports, and a list of all the defined clocks in the design. These summaries cover all paths you constrain in your design. Whenever modifying or correcting constraints, generate the Diagnostic reports to identify unconstrained parts of your design, or ignored constraints.
3. Analyze the results in the reports. When you are modifying constraints, rerun the reports to find any unexpected results. For example, a cross-domain path might indicate that you forgot to cut a transfer by including a clock in a clock group.
4. Create or edit the appropriate constraints in your .sdc file and save the file.
5. Double-click Reset Design in the Tasks pane. This removes all constraints from your design. Removing all constraints from your design allows rereading the .sdc files, including your changes.
6. Regenerate the reports you want to analyze.
7. Reanalyze the results.
8. Repeat steps 4-7 as necessary.

This method performs timing analysis using new constraints, without any change to logic placement. While the Fitter uses the original constraints for place and route, the Timing Analyzer applies the new constraints. If you see any failing timing against the new constraints, run place-and-route again.

**Related Information**
Relaxing Setup with Multicycle (set_multicycle_path) on page 99

### 2.6.4. Using Entity-bound SDC Files

The Intel Quartus Prime Pro Edition Timing Analyzer supports the assignment of a Synopsys Design Constraints (.sdc) file to a specific design entity (module) in your project.

Normally, timing constraints that you specify in an .sdc file apply globally in your project, rather than to any particular design entity. However, you can use the Properties dialog box or SDC_ENTITY_FILE assignment to bind an .sdc file to a design entity. Entity-bound constraints make timing constraints more portable, and allow you to specify constraints with higher precision.

- **Timing constraint portability**—all design partitions that contain the assigned entity automatically include entity-bound .sdc constraints. You can optionally specify export of these constraints with a partition you export with the Include entity-bound SDC files (--include_sdc_entity_in_partition) option. This allows you to hand-off synthesized or final design blocks or IP packaged with timing constraints.
- **Timing constraint precision**—Apply timing constraints only to specific entities rather than globally, simplifying constraint entry. This method avoids unintended side effects of global constraints that apply to more than you intend, especially when using wildcard (*) timing constraints. By default, entity-bound .sdc constraints apply automatically to all instances of the assigned entity in the project. Alternatively, you can apply all of the constraints globally by default, and choose which of its constraints target only the current entity, by using the get_current_instance command, as Entity-bound Constraint Scope on page 75 describes.
- **Note:** All Intel Stratix 10 FPGA IP cores use entity-bound .sdc constraints automatically.

Follow these steps to create or modify an entity-bound .sdc file:

1. Create an .sdc file, click Project ➤ Add/Remove files in project, and add the .sdc file. The .sdc file appears in the Files list.
2. In the Files list, select the .sdc file and click the Properties button.
3. For Type, select Synopsys Design Constraints File with entity binding.
4. For **Entity**, select the entity you want to bind to the `.sdc`.

5. Click **OK**.

Alternatively, add the following assignment to the `.qsf` to bind the entity you specify to the `.sdc` file you specify:

**QSF Assignment Syntax:**

```plaintext
set_instance_assignment -entity <entity_name> -name \ 
  SDC_ENTITY_FILE <sdc_file_name> -no_sdc_promotion -no_auto_inst_discovery
```

For an `SDC_ENTITY_FILE` assignment, you must specify a `-library` parameter that matches the `-library` argument of the referenced entity. If you specify no library, the software uses the default `altera_work` library.

Both the entity and the library must match the target RTL module for the `SDC_ENTITY_FILE` to be applied.

The following options apply to the `SDC_ENTITY_FILE` assignment:

- **No options**—enable automatic constraint scoping. The Timing Analyzer reads in entity `.sdc` files once for each bound instance, and `get_current_instance` returns a value. The collection filters (except for clock and top-level port filters) get prepended with the hierarchy path of the current instance (that is, the return value of `get_current_instance`).

- **-no_sdc_promotion**—turns on manual promotion. The Timing Analyzer reads in entity `.sdc` files once for each bound instance, and `get_current_instance` returns a value. The Timing Analyzer does not modify the collection filters.

- **-no_sdc_promotion -no_auto_inst_discovery**—turns off constraint scoping. The Timing Analyzer reads in each entity `.sdc` file once, and does not modify the collection filters. `get_current_instance` returns an empty string.
### 2.6.4.1. Entity-bound Constraint Scope

Entity-bound `.sdc` files can have an automatic or manual scope in your project. The scope determines how widely the constraints apply. Automatic scoping applies by default.

#### Table 21. Entity-bound Constraint Scope

<table>
<thead>
<tr>
<th>Constraint Scope Type</th>
<th>Constraints Apply</th>
<th>To Enable Instance-bound Scoping</th>
</tr>
</thead>
<tbody>
<tr>
<td>Automatic</td>
<td>To all instances of the assigned entity throughout the project, except for top-level ports (<code>get_ports</code>) and clock names (<code>get_clocks</code>).</td>
<td>Default mode for <code>SDC_ENTITY_FILE</code>. No additional steps required.</td>
</tr>
<tr>
<td>Manual</td>
<td>To the current instance of the assigned entity, except for top-level ports and clock names, which have a global scope. Collection filters also have global scope, unless you prepend them with <code>get_current_instance</code>, which sets the instance scope.</td>
<td>Prepend the collection filter with <code>get_current_instance</code>.</td>
</tr>
</tbody>
</table>

The following example constraint shows use of `get_current_instance` to return the hierarchical path to the current entity for manual constraint scoping:

```
set_false_path -from [get_registers "reg_a"] -to \
    [get_pins "[get_current_instance]|*reset"]
```

**Note:** If you use the `-from *` or `-to *` options without using one of the `get_` commands (such as `get_keepers`), no constraint scoping occurs on those filters (that is to say, scoping is not done on from/to collection filters of `*`, but scoping can still occur on other collection filters in the same SDC command).

### 2.6.4.2. Entity-bound Constraint Examples

The following examples show the automatic and manual scope of entity-bound constraints.

#### Figure 87. Automatic Scope Example

The following table illustrates the automatic scope of constraints as they apply to Figure 87 on page 75.
Table 22. Automatic Constraint Scoping Examples

| Constraint Example | Auto-Scope Constraint Interpretation for Instance X|Y |
|--------------------|--------------------------------------------------|
| set_false_path -from [get_keepers a] | set_false_path -from [get_keepers X|Y|a] |
| set_false_path -from [get_registers a] -to "*" | set_false_path -from [get_registers X|Y|a] |
| set_false_path -from [get_clocks clk_1] -to [get_clocks clk_2] | set_false_path -from [get_clocks clk_1] -to [get_clocks clk_2] |
| set_max_delay -from [get_ports in] -to [get_registers A] 2.0 | set_max_delay -from [get_ports in] -to [get_registers X|Y|A] 2.0 |
| get_ports * | get_ports * |
| get_clocks * | get_clocks * |
| get_ports a | get_ports a |
| get_clocks a | get_clocks a |

**Note:** In table, get_ports a and get_clocks a are simply examples that use an arbitrary name for the collection filter. These examples show that collection filters for get_ports and get_clocks are not subject to automatic constraint scoping because the ports and clocks are global, top-level objects that are never in the scope of an instance.

Figure 88. Manual Scope Example

The following table illustrates the manual scope of constraints as they apply to Figure 88 on page 76.
2.6.5. Creating Clocks and Clock Constraints

You must define all clocks and any associated clock characteristics, such as uncertainty, latency or skew. The Timing Analyzer supports .sdc commands that accommodate various clocking schemes, such as:

- Base clocks
- Virtual clocks
- Multifrequency clocks
- Generated clocks

2.6.5.1. Creating Base Clocks

Base clocks are the primary input clocks to the device. The Create Clock (create_clock) constraint allows you to define the properties and requirements for clocks in the design. Unlike clocks that are generated in the device (such as an on-chip PLL), base clocks are generated by off-chip oscillators or forwarded from an external device. Define base clocks at the top of your .sdc file, because generated clocks and other constraints often reference base clocks. The Timing Analyzer ignores any constraints that reference an undefined clock.

The following examples show common use of the create_clock constraint:

create_clock Command

The following specifies a 100 MHz requirement on a clk_sys input clock port:

```create_clock -period 10 -name clk_sys [get_ports clk_sys]```

100 MHz Shifted by 90 Degrees Clock Creation

The following creates a 10 ns clock, with a 50% duty cycle, that is phase shifted by 90 degrees, and applies to port clk_sys. This type of clock definition commonly refers to source synchronous, double-rate data that is center-aligned with respect to the clock.

```create_clock -period 10 -waveform { 2.5 7.5 } [get_ports clk_sys]```
Two Oscillators Driving the Same Clock Port

You can apply multiple clocks to the same target with the -add option. For example, to specify that you can drive the same clock input at two different frequencies, enter the following commands in your .sdc file:

```
create_clock -period 10 -name clk_100 [get_ports clk_sys]
create_clock -period 5 -name clk_200 [get_ports clk_sys] -add
```

Although uncommon to define more than two base clocks for a port, you can define as many as are appropriate for your design, making sure you specify -add for all clocks after the first.

Creating Multifrequency Clocks

You must create a multifrequency clock if your design has more than one clock source feeding a single clock node. The additional clock may act as a low-power clock, with a lower frequency than the primary clock. If your design uses multifrequency clocks, use the set_clock_groups command to define clocks that are exclusive.

Use the create_clock command with the -add option to create multiple clocks on a clock node. You can create a 10 ns clock applied to clock port clk, and then add an additional 15 ns clock to the same clock port. The Timing Analyzer analyzes both clocks.

```
create_clock -period 10 -name clock_primary -waveform { 0 5 } [get_ports clk]
create_clock -period 15 -name clock_secondary -waveform { 0 7.5 } [get_ports clk] -add
```

Related Information

Accounting for Clock Effect Characteristics on page 88

2.6.5.1.1. Automatic Clock Detection and Constraint Creation

Use the derive_clocks command to automatically create base clocks in your design. The derive_clocks command is equivalent to using the create_clock command for each register or port feeding the clock pin of a register. The derive_clocks command creates clock constraints on ports or registers to ensure every register in your design has a clock constraints, and it applies one period to all base clocks in your design.

The following command specifies a base clock with a 100 MHz requirement for unconstrained base clock nodes.

```
derive_clocks -period 10
```

Caution: If your design has more than a single clock, the derive_clocks command constrains all the clocks to the same specified frequency. To achieve a realistic analysis of your design's timing requirements, do not use derive_clocks command for final timing sign-off. Instead, use create_clock and create_generated_clock commands to make individual clock constraints for all clocks in your design.

If you want to create some base clocks automatically, use the create_base_clocks option to derive_pll_clocks. With this option, the derive_pll_clocks command automatically creates base clocks for each PLL,
based on the input frequency information that you specify when you generate the PLL. This feature works for simple port-to-PLL connections. Base clocks do not automatically generate for complex PLL connectivity, such as cascaded PLLs. You can also use the command `derive_pll_clocks -create_base_clocks` to create the input clocks for all PLL inputs automatically.

### 2.6.5.2. Creating Virtual Clocks

A virtual clock is a clock without a real source in the design, or a clock that does not interact directly with the design. You can use virtual clocks in I/O constraints to represent clocks that drive external devices connected to the FPGA.

To create virtual clocks, use the `create_clock` constraint with no value for the `<targets>` option.

This following example defines a 100 MHz virtual clock because the command includes no `<targets>`.

```
create_clock -period 10 -name my_virt_clk
```

### I/O Constraints with Virtual Clocks

You can use a base clock to constrain the circuit in the FPGA and a virtual clock to represent the clock driving the external device.

#### Figure 89. Virtual Clock Board Topology

The figure shows the base clock (`system_clk`), virtual clock (`virt_clk`), and output delay for the virtual clock constraints example.

The following example creates the 10 ns `virt_clk` virtual clock, with a 50% duty cycle, with the first rising edge occurring at 0 ns. The virtual clock can then become the clock source for an output delay constraint.

#### Example 2. Virtual Clock Constraints

```
# create base clock for the design
create_clock -period 5 [get_ports system_clk]
# create the virtual clock for the external register
create_clock -period 10 -name virt_clk
# set the output delay referencing the virtual clock
set_output_delay -clock virt_clk -max 1.5 [get_ports dataout]
set_output_delay -clock virt_clk -min 0.0 [get_ports dataout]
```
2.6.5.2.1. Specifying I/O Interface Uncertainty

Virtual clocks are recommended for I/O constraints because they most accurately represent the clocking topology of the design. An additional benefit is that you can specify different uncertainty values on clocks that interface with external I/O ports and clocks that feed register-to-register paths inside the FPGA.

2.6.5.2.2. I/O Interface Clock Uncertainty Example

To specify I/O interface uncertainty, you must create a virtual clock and constrain the input and output ports with the set_input_delay and set_output_delay commands that reference the virtual clock.

When the set_input_delay or set_output_delay commands reference a clock port or PLL output, the virtual clock allows the derive_clock_uncertainty command to apply separate clock uncertainties for internal clock transfers and I/O interface clock transfers.

Create the virtual clock with the same properties as the original clock that is driving the I/O port, as the following example shows:

Example 3. SDC Commands to Constrain the I/O Interface

```
# Create the base clock for the clock port
create_clock -period 10 -name clk_in [get_ports clk_in]
# Create a virtual clock with the same properties of the base clock
# driving the source register
create_clock -period 10 -name virt_clk_in
# Create the input delay referencing the virtual clock and not the base
# clock
# DO NOT use set_input_delay -clock clk_in <delay value>
# [get_ports data_in]
set_input_delay -clock virt_clk_in <delay value> [get_ports data_in]
```

2.6.5.3. Creating Generated Clocks (create_generated_clock)

The Create Generate Clock (create_generated_clock) constraint allows you to define the properties and constraints of an internally generated clock in the design. You specify the Clock name (-name), the Source node (-source) from which clock derives, and the Relationship to the source properties. Define generated clocks for any node that modifies the properties of a clock signal, including modifying the phase, frequency, offset, or duty cycle.

You apply generated clocks most commonly on the outputs of PLLs, on register clock dividers, clock muxes, and clocks forwarded to other devices from an FPGA output port, such as source synchronous and memory interfaces. In the .sdc file, enter generated clocks after the base clocks definitions. Generated clocks automatically account for all clock delays and clock latency to the generated clock target.

The -source option specifies the name of a node in the clock path that you use as reference for your generated clock. The source of the generated clock must be a node in your design netlist, and not the name of a clock you previously define. You can use any node name on the clock path between the input clock pin of the target of the generated clock and the target node of its reference clock as the source node.
Specify the input clock pin of the target node as the source of your new generated clock. By accepting a node as the generated clock's source clock, the generated clock constraint decouples from the source clock. If you change the source clock for the generated clock and the source node is the same, you do not have to edit the generated clock constraint.

If you have multiple base clocks feeding a node that is the source for a generated clock, you must define multiple generated clocks. You associate each generated clock with one base clock using the -master_clock option in each generated clock statement. In some cases, generated clocks generate with combinational logic.

Depending on how your clock-modifying logic synthesizes, the source or target node can change from one compilation to the next. If the name changes after you write the generated clock constraint, the Compiler ignores the generated clock because that target name no longer exists in the design. To avoid this problem, use a synthesis attribute or synthesis assignment to retain the final combinational node name of the clock-modifying logic. Then use the kept name in your generated clock constraint.

Figure 90. Example of clock-as-data

When you create a generated clock on a node that ultimately feeds the data input of a register, this creates a special case of "clock-as-data." The Timing Analyzer treats clock-as-data differently. For example, if you use clock-as-data with DDR, you must consider both the rise and the fall of this clock, and the Timing Analyzer reports both rise and fall. With clock-as-data, the Compiler treats the From Node as the target of the generated clock, and the Launch Clock as the generated clock.

In Figure 90 on page 81, the first path is from toggle_clk (INVERTED) to clk, and the second path is from toggle_clk to clk. The slack in both cases is slightly different due to the difference in rise and fall times along the path. The Data Delay column reports the ~5 ps difference. Only the path with the lowest slack value requires consideration. The Timing Analyzer only reports the worst-case path between the two (rise and fall). In this example, if you do not define the generated clock on the register output, then timing analysis reports only one path with the lowest slack value.

You can use the derive_pll_clocks command to automatically generate clocks for all PLL clock outputs. The properties of the generated clocks on the PLL outputs match the properties you define for the PLL.
2.6.5.3.1. Clock Divider Example (-divide_by)

A common form of generated clock is the divide-by-two register clock divider. The following example constraint creates a half-rate clock on the divide-by-two register.

```plaintext
create_clock -period 10 -name clk_sys [get_ports clk_sys]
create_generated_clock -name clk_div_2 -divide_by 2 -source [get_ports clk_sys] [get_pins reg|q]
```

To specify the clock pin of the register as the clock source:

```plaintext
create_clock -period 10 -name clk_sys [get_ports clk_sys]
create_generated_clock -name clk_div_2 -divide_by 2 -source [get_pins reg|clk] [get_pins reg|q]
```

**Figure 91.  Clock Divider**

![Clock Divider Diagram](image)

**Figure 92.  Clock Divider Waveform**

<table>
<thead>
<tr>
<th>Edges</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_sys</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>clk_div_2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**2.6.5.3.2. Clock Multiplexer Example**

The output of a clock multiplexer (mux) is a form of generated clock. Each input clock requires one generated clock on the output. The following .sdc example also includes the `set_clock_groups` command to indicate that the two generated clocks can never be active simultaneously in the design. Therefore, the Timing Analyzer does not analyze cross-domain paths between the generated clocks on the output of the clock mux.
2.6.5.4. Deriving PLL Clocks

The Derive PLL Clocks (\texttt{derive_pll_clocks}) constraint automatically creates clocks for each output of any PLL in your design. \texttt{derive_pll_clocks} detects your current PLL settings and automatically creates generated clocks on the outputs of every PLL by calling the \texttt{create_generated_clock} command.

\textbf{Note:} Only Intel Arria 10 and Intel Cyclone 10 GX devices support the Derive PLL Clocks (\texttt{derive_pll_clocks}) constraint. For all other supported devices, the Timing Analyzer automatically derives PLL clocks from constraints bound to the related IP.

Create Base Clock for PLL input Clock Ports

If your design contains transceivers, LVDS transmitters, or LVDS receivers, use the \texttt{derive_pll_clocks} to constrain this logic in your design and create timing exceptions for those blocks.

\begin{verbatim}
create_clock -period 10.0 -name fpga_sys_clk [get_ports fpga_sys_clk] \ derive_pll_clocks
\end{verbatim}

Include the \texttt{derive_pll_clocks} command in your .sdc file after any \texttt{create_clock} command. Each time the Timing Analyzer reads the .sdc file, the appropriate generated clock is created for each PLL output clock pin. If a clock exists on a PLL output before running \texttt{derive_pll_clocks}, the pre-existing clock has precedence, and an auto-generated clock is not created for that PLL output.

The following shows a simple PLL design with a register-to-register path:

\begin{verbatim}
create_clock -name clock_a -period 10 [get_ports clk_a]
create_clock -name clock_b -period 10 [get_ports clk_b]
create_generated_clock -name clock_a_mux -source [get_ports clk_a]\ [get_pins clk_mux|mux_out]
create_generated_clock -name clock_b_mux -source [get_ports clk_b]\ [get_pins clk_mux|mux_out] -add
set_clock_groups -logically_exclusive -group clock_a_mux -group clock_b_mux
\end{verbatim}

The Timing Analyzer generates messages like the following example when you use the \texttt{derive_pll_clocks} command to constrain the PLL.
Example 4. **derive_pll_clocks Command Messages**

```
Info: Deriving PLL Clocks:
Info: create_generated_clock -source pll_inst|altpll_component|pll|inclk[0] -
divide_by 2 -name
pll_inst|altpll_component|pll|clk[0] pll_inst|altpll_component|pll|clk[0]
Info:
```

The input clock pin of the PLL is the node `pll_inst|altpll_component|pll|inclk[0]` which is the `-source` option. The name of the output clock of the PLL is the PLL output clock node, `pll_inst|altpll_component|pll|clk[0]`.

If the PLL is in clock switchover mode, multiple clocks generate for the output clock of the PLL; one for the primary input clock (for example, `inclk[0]`), and one for the secondary input clock (for example, `inclk[1]`). Create exclusive clock groups for the primary and secondary output clocks since they are not active simultaneously.

**Related Information**

Creating Clock Groups (set_clock_groups) on page 84

### 2.6.5.5. Creating Clock Groups (set_clock_groups)

The **Set Clock Groups** (`set_clock_groups`) constraint allows you to specify which clocks in the design are unrelated.

The `set_clock_groups` command allows you to cut timing between unrelated clocks in different groups. The Timing Analyzer performs the same analysis regardless of whether you specify `-exclusive` or `-asynchronous` groups. You define a clock group with the `-group` option. The Timing Analyzer excludes the timing paths between clocks for each of the separate groups.

The following tables show the impact of `set_clock_groups`.

**Table 24.** `set_clock_groups -group A`

<table>
<thead>
<tr>
<th>Dest\Source</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>B</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>C</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>D</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
</tbody>
</table>

**Table 25.** `set_clock_groups -group {A B}`

<table>
<thead>
<tr>
<th>Dest\Source</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Analyzed</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>B</td>
<td>Analyzed</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>C</td>
<td>Cut</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>D</td>
<td>Cut</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
</tbody>
</table>
Table 26.  `set_clock_groups -group A -group B`

<table>
<thead>
<tr>
<th>Dest\Source</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>B</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>C</td>
<td>Cut</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>D</td>
<td>Cut</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
</tbody>
</table>

Table 27.  `set_clock_groups -group \{A C\} -group \{B D\}`

<table>
<thead>
<tr>
<th>Dest\Source</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
</tr>
<tr>
<td>B</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
</tr>
<tr>
<td>C</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
</tr>
<tr>
<td>D</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
</tr>
</tbody>
</table>

Table 28.  `set_clock_groups -group \{A C D\}`

<table>
<thead>
<tr>
<th>Dest\Source</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>B</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Cut</td>
</tr>
<tr>
<td>C</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
<tr>
<td>D</td>
<td>Analyzed</td>
<td>Cut</td>
<td>Analyzed</td>
<td>Analyzed</td>
</tr>
</tbody>
</table>

Related Information
set_clock_groups Command, Intel Quartus Prime Help

2.6.5.5.1. Exclusive Clock Groups (\-logically\_exclusive or \-physically\_exclusive)

You can use the \-logically\_exclusive or \-physically\_exclusive option to declare that two clocks are mutually exclusive.

If you define multiple clocks for the same node, you can use clock group assignments with the \-logically\_exclusive or \-physically\_exclusive options to declare clocks as mutually exclusive. This technique can be useful for multiplexed clocks.
For example, consider an input port that is clocked by either a 100-MHz or 125-MHz clock. You can use the `-logically_exclusive` or `-physically_exclusive` options to declare that the clocks are mutually exclusive and eliminate clock transfers between the 100-MHz and 125-MHz clocks, as the following diagrams and example SDC constraints show:

![Figure 95. Synchronous Path with Clock Mux Internal to FPGA](image1)

**Example SDC Constraints for Internal Clock Mux**

```plaintext
# Create a clock on each port
create_clock -name clk_100 -period 10 [get_ports clkA]
create_clock -name clk_125 -period 8 [get_ports clkB]
# Set the two clocks as exclusive clocks
set_clock_groups -logically_exclusive -group {clk_100} -group {clk_125}
```

![Figure 96. Synchronous Path with Clock Mux External to FPGA](image2)

**Example SDC Constraints for External Clock Mux**

```plaintext
# Create two clocks on the port clk
create_clock -name clkA -period 10 [get_ports clk]
create_clock -name clkB -period 8 [get_ports clk] -add
# Set the two clocks as exclusive clocks
set_clock_groups -logically_exclusive -group {clkA} -group {clkB}
```

### 2.6.5.5.2. Asynchronous Clock Groups (-asynchronous)

Use the `-asynchronous` option to create asynchronous clock groups. You can use asynchronous clock groups to break the timing relationship when data transfers through a FIFO between clocks running at different rates.
### 2.6.5.3. `set_clock_groups` Constraint Tips

When you use `derive_pll_clocks` to create clocks, it can be time consuming to determine all the clock names to include in `set_clock_groups` constraints. However, you can use the following technique to somewhat automate clock constraint creation, even if you do not know all of the clock names.

1. Create a basic `.sdc` file that contains the Recommended Initial SDC Constraints on page 68, except omit the `set_clock_groups` constraint for now.
2. To add the `.sdc` to the project, click **Assignments ➤ Settings ➤ Timing Analyzer**. Specify the `.sdc` file under **SDC files to include in the project**.
3. To open the Timing Analyzer, click **Tools ➤ Timing Analyzer**.
4. In the **Task** pane, double-click **Report Clocks**. The Timing Analyzer reads your `.sdc`, applies the constraints (including `derive_pll_clocks`), and reports all the clocks.
5. From the Clocks Summary report, copy all the clock names that appear in the first column. The report lists the clock names in the correct format for recognition in the Timing Analyzer.
6. Open `.sdc` file and paste the clock names into the file, one clock name per line.
7. Format the list of clock names list into the `set_clock_groups` command by cutting and pasting clock names into appropriate groups. Next, paste the following template into the `.sdc` file:

```tcl
set_clock_groups -asynchronous -group { 
  } 
-group { 
  } 
-group { 
  } 
-group { 
  }
```
8. Cut and paste the clock names into groups to define their relationship, adding or removing groups as necessary. Format the groups to make the code readable.

**Note:** This command can be difficult to read on a single line. You can use the Tcl line continuation character `\` to make this more readable. Place a space after the last character, and then place the `\` character at the end of the line. Be careful not to include any spaces after the escape character. Otherwise, the space becomes the escape character, rather than the end-of-line character.

```tcl
set_clock_groups -asynchronous \
 -group {adc_clk \ 
  the_adc_pll|altpll_component_autogenerated|pll|clk[0] \ 
  the_adc_pll|altpll_component_autogenerated|pll|clk[1] \ 
  the_adc_pll|altpll_component_autogenerated|pll|clk[2] \ 
  } \ 
 -group {sys_clk \ 
  the_system_pll|altpll_component_autogenerated|pll|clk[0] \ 
  the_system_pll|altpll_component_autogenerated|pll|clk[1] \ 
  } \ 
 -group {the_system_pll|altpll_component_autogenerated|pll|clk[2] \ 
  }
```
Note: The last group has a PLL output `system_pll..|clk[2]` while the input clock and other PLL outputs are in different groups. If you use PLLs, and the input clock frequency does not relate to the frequency of the PLL's outputs, you must treat the PLLs asynchronously. Usually most outputs of a PLL relate and are in the same group, but this is not a requirement.

For designs with complex clocking, creating clock groups can be an iterative process. For example, a design with two DDR3 cores and high-speed transceivers can have thirty or more clocks. In such cases, you start by adding the clocks that you manually create. Timing Analyzer assumes that the clocks not appearing in the clock groups command relate to every clock and conservatively groups the known clocks. If the design still has re failing paths between unrelated clock domains, you can add the new clock domains as necessary. In this case, a large number of the clocks are not in the `set_clock_groups` command, because they are either cut in the `.sdc` file for the IP (such as the `.sdc` files that the DDR3 cores generate), or they connect only to related clock domains.

For many designs, that is all that's necessary to constrain the IP.

**Related Information**

*Multicycle Paths* on page 98

### 2.6.5.6. Accounting for Clock Effect Characteristics

The clocks you create with the Timing Analyzer are ideal clocks that do not account for any board effects. You can account for clock effect characteristics with clock latency and clock uncertainty constraints.

#### 2.6.5.6.1. Set Clock Latency (`set_clock_latency`)

The **Set Clock Latency** (`set_clock_latency`) constraint allows you to specify additional delay (that is, latency) in a clock network. This delay value represents the external delay from a virtual (or ideal) clock through the longest **Late** (`-late`) or shortest **Early** (`-early`) path, with reference to the **Rise** (`-rise`) or **Fall** (`-fall`) of the clock transition.

When calculating setup analysis, the Timing Analyzer uses the late clock latency for the data arrival path and the early clock latency for the clock arrival path. When calculating hold analysis, the Timing Analyzer uses the early clock latency for the data arrival time and the late clock latency for the clock arrival time.

There are two forms of clock latency: clock source latency, and clock network latency. Source latency is the propagation delay from the origin of the clock to the clock definition point (for example, a clock port). Network latency is the propagation delay from a clock definition point to a register's clock pin. The total latency at a register's clock pin is the sum of the source and network latencies in the clock path.

To specify source latency to any clock ports in your design, use the `set_clock_latency` command.

*Note:* The Timing Analyzer automatically computes network latencies. Therefore, you can only characterize source latency with the `set_clock_latency` command using the `-source` option.
2.6.5.6.2. Clock Uncertainty

By default, the Timing Analyzer creates clocks that are ideal and have perfect edges. To mimic clock-level effects like jitter, you can add uncertainty to those clock edges. The Timing Analyzer automatically calculates appropriate setup and hold uncertainties and applies those uncertainties to all clock transfers in your design, even if you do not include the `derive_clock_uncertainty` command in your .sdc file. Setup and hold uncertainties are a critical part of constraining your design correctly.

The Timing Analyzer subtracts setup uncertainty from the data required time for each applicable path and adds the hold uncertainty to the data required time for each applicable path. This slightly reduces the setup and hold slack on each path.

The Timing Analyzer accounts for uncertainty clock effects for three types of clock-to-clock transfers: intraclock transfers, interclock transfers, and I/O interface clock transfers.

- Intraclock transfers occur when the register-to-register transfer takes place in the device and the source and destination clocks come from the same PLL output pin or clock port.
- Interclock transfers occur when a register-to-register transfer takes place in the core of the device and the source and destination clocks come from a different PLL output pin or clock port.
- I/O interface clock transfers occur when data transfers from an I/O port to the core of the device or from the core of the device to the I/O port.

To manually specify clock uncertainty, use the `set_clock_uncertainty` command. You can specify the uncertainty separately for setup and hold. You can also specify separate values for rising and falling clock transitions. You can override the value that the `derive_clock_uncertainty` command automatically applies.

The `derive_clock_uncertainty` command accounts for PLL clock jitter, if the clock jitter on the input to a PLL is within the input jitter specification for PLL's in the target device. If the input clock jitter for the PLL exceeds the specification, add additional uncertainty to your PLL output clocks to account for excess jitter with the `set_clock_uncertainty -add` command. Refer to the device handbook for your device for jitter specifications.

You can also use `set_clock_uncertainty -add` to account for peak-to-peak jitter from a board when the jitter exceeds the jitter specification for that device. In this case you add uncertainty to both setup and hold equal to 1/2 the jitter value:

```
set_clock_uncertainty -setup -to <clock name> \ -setup -add <p2p jitter/2>
```

```
set_clock_uncertainty -hold -enable_same_physical_edge -to <clock name> \ -add <p2p jitter/2>
```
There is a complex set of precedence rules for how the Timing Analyzer applies values from `derive_clock_uncertainty` and `set_clock_uncertainty`, which depend on the order of commands and options in your `.sdc` files. The Help topics below contain complete descriptions of these rules. These precedence rules are easier to implement if you follow these recommendations:

- To assign your own clock uncertainty values to any clock transfers, put your `set_clock_uncertainty` exceptions after the `derive_clock_uncertainty` command in the `.sdc` file.
- When you use the `-add` option for `set_clock_uncertainty`, the value you specify is additive to the `derive_clock_uncertainty` value. If you do not specify `-add`, the value you specify replaces the value from `derive_clock_uncertainty`.

**Related Information**
- `set_clock_uncertainty`, Intel Quartus Prime Help
- `derive_clock_uncertainty`, Intel Quartus Prime Help
- `remove_clock_uncertainty`, Intel Quartus Prime Help

### 2.6.6. Creating I/O Constraints

The Timing Analyzer reviews setup and hold relationships for designs in which an external source interacts with a register internal to the design. The Timing Analyzer supports input and output external delay modeling with the `set_input_delay` and `set_output_delay` commands. You can specify the clock and minimum and maximum arrival times relative to the clock.

Specify internal and external timing requirements before you fully analyze a design. With external timing requirements specified, the Timing Analyzer verifies the I/O interface, or periphery of the device, against any system specification.

#### 2.6.6.1. Input Constraints (set_input_delay)

Input constraints specify delays for all external signals feeding the FPGA. Specify input requirements for all input ports in your design.

```
set_input_delay -clock { clock } -clock_fall -fall -max 20 foo
```

Use the **Set Input Delay** (`set_input_delay`) constraint to specify external input delay requirements. Specify the **Clock name** (`-clock`) to reference the virtual or actual clock. You can specify a clock to allow the Timing Analyzer to correctly derive clock uncertainties for interclock and intraclock transfers. The clock defines the launching clock for the input port. The Timing Analyzer automatically determines the latching clock inside the device that captures the input data, because all clocks in the device are defined.
Figure 97. Input Delay Diagram

![Input Delay Diagram](image)

Figure 98. Input Delay Calculation

\[
\begin{align*}
\text{input delay}_{\text{MAX}} &= (\text{cd}_{\text{ext}}_{\text{MAX}} - \text{cd}_{\text{altr}}_{\text{MIN}}) + \text{tco}_{\text{ext}}_{\text{MAX}} + \text{dd}_{\text{MAX}} \\
\text{input delay}_{\text{MIN}} &= (\text{cd}_{\text{ext}}_{\text{MIN}} - \text{cd}_{\text{altr}}_{\text{MAX}}) + \text{tco}_{\text{ext}}_{\text{MIN}} + \text{dd}_{\text{MIN}}
\end{align*}
\]

If your design includes partition boundary ports, you can use the `-blackbox` option with `set_input_delay` to assign input delays. The `-blackbox` option creates a new keeper timing node with the same name as the boundary port. This new node permits the propagation of timing paths through the original boundary port and acts as a `set_input_delay` constraint. The new keeper timing nodes display when you use the `get_keepers` command. You can remove these black box constraints with `remove_input_delay -blackbox`.

2.6.6.2. Output Constraints (set_output_delay)

Output constraints specify all external delays from the device for all output ports in your design.

```
set_output_delay -clock { clock } -clock_fall -rise -max 2 foo
```

Use the Set Output Delay (set_output_delay) constraint to specify external output delay requirements. Specify the Clock name (-clock) to reference the virtual or actual clock. When specifying a clock, the clock defines the latching clock for the output port. The Timing Analyzer automatically determines the launching clock inside the device that launches the output data, because all clocks in the device are defined. The following figure is an example of an output delay referencing a virtual clock.

Figure 99. Output Delay Diagram

![Output Delay Diagram](image)
Figure 100. Output Delay Calculation

\[
\text{output delay}_{\text{MAX}} = dd_{\text{MAX}} + tsu_{\text{ext}} + (cd_{\text{altr}}_{\text{MAX}} - cd_{\text{ext}}_{\text{MIN}}) \\
\text{output delay}_{\text{MIN}} = (dd_{\text{MIN}} - th_{\text{ext}} + (cd_{\text{altr}}_{\text{MIN}} - cd_{\text{ext}}_{\text{MAX}}))
\]

If your design includes partition boundary ports, you can use the -blackbox option with set_output_delay to assign output delays. The -blackbox option creates a new keeper timing node with the same name as the boundary port. This new node permits the propagation of timing paths through the original boundary port and acts as a set_output_delay constraint. The new keeper timing nodes display when you use the get_keepers command.

You can remove blackbox constraints with remove_output_delay -blackbox.

Related Information
- set_input_delay Command, Intel Quartus Prime Help
- set_output_delay Command, Intel Quartus Prime Help

2.6.7. Creating Delay and Skew Constraints

You can specify skew and delays to model external device timing and board timing parameters.

2.6.7.1. Advanced I/O Timing and Board Trace Model Delay

The Timing Analyzer can use advanced I/O timing and board trace model constraints to model I/O buffer delays in your design.

If you change any advanced I/O timing settings or board trace model assignments, recompile your design before you analyze timing, or use the -force_dat option to force delay annotation when you create a timing netlist.

Example 5. Forcing Delay Annotation

```bash
create_timing_netlist -force_dat
```

2.6.7.2. Maximum Skew (set_max_skew)

The **Set Max Skew** (set_max_skew) constraint specifies the maximum allowable skew between the sets of registers or ports you specify. In order to constrain skew across multiple paths, you must constrain all such paths within a single set_max_skew constraint.

```bash
set_max_skew -from_clock { clock } -to_clock { * } -from foo -to blat 2
```

The set_max_delay, set_min_delay, and set_multicycle_path constraints do not affect the set_max_skew timing constraint. However, the set_false_path and set_clock_groups constraints do impact the set_max_skew constraint.

The Timing Analyzer does not analyze paths cut by a false path for skew, and does not compare two paths for skew if their clocks are exclusive to each other. However, the Timing Analyzer does analyze for skew paths whose clocks are asynchronous.
Table 29.  set_max_skew Options

<table>
<thead>
<tr>
<th>Arguments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-h</td>
<td>-help</td>
</tr>
<tr>
<td>-long_help</td>
<td>Long help with examples and possible return values.</td>
</tr>
<tr>
<td>-fall_from_clock &lt;names&gt;</td>
<td>Valid source clocks (Tcl matches string patterns). Analysis only considers paths from falling clock edges.</td>
</tr>
<tr>
<td>-fall_to_clock &lt;names&gt;</td>
<td>Valid destination clocks (Tcl matches string patterns). Analysis only considers paths from falling clock edges.</td>
</tr>
<tr>
<td>-from &lt;names&gt;</td>
<td>Valid sources (Tcl matches string patterns).</td>
</tr>
<tr>
<td>-from_clock &lt;names&gt;</td>
<td>Valid source clocks (Tcl matches string patterns).</td>
</tr>
<tr>
<td>-get_skew_value_from_clock_period &lt;src_clock_period</td>
<td>&lt;dst_clock_period</td>
</tr>
<tr>
<td>-rise_from_clock &lt;names&gt;</td>
<td>Valid source clocks (Tcl matches string patterns). Analysis only considers paths from rising clock edges.</td>
</tr>
<tr>
<td>-rise_to_clock &lt;names&gt;</td>
<td>Valid destination clocks (Tcl matches string patterns). Analysis only considers paths to rising clock edges.</td>
</tr>
<tr>
<td>-skew_value_multiplier &lt;multiplier&gt;</td>
<td>Value by which the clock period multiplies to compute skew requirement.</td>
</tr>
<tr>
<td>-to &lt;names&gt;</td>
<td>Valid destinations (Tcl matches string patterns)</td>
</tr>
<tr>
<td>-to_clock &lt;names&gt;</td>
<td>Valid destination clocks (Tcl matches string patterns).</td>
</tr>
<tr>
<td>&lt;skew&gt;</td>
<td>The value of the skew you require.</td>
</tr>
</tbody>
</table>

Applying maximum skew constraints between clocks applies the constraint from all register or ports driven by the clock you specify (with the -from option) to all registers or ports driven by the clock you specify (with the -to option).

Maximum skew analysis can include data arrival times, clock arrival times, register micro parameters, clock uncertainty, on-die variation, and ccpp removal. Among these, the Fitter only disables ccpp removal by default. When you use -include, the default analysis includes those in the inclusion list.

Use -get_skew_value_from_clock_period to set the skew as a multiple of the launching or latching clock period, or whichever of the two has a smaller period. If you use this option, set -skew_value_multiplier, and you may not set the positional skew option. If more than one clock clocks the set of skew paths, Timing Analyzer uses the clock with smallest period to compute the skew constraint.

Click Report Max Skew (report_max_skew) to view the max skew analysis. Since skew occurs between two or more paths, no results display if the -from/-from_clock and -to/-to_clock filters satisfy less than two paths.

**Related Information**

report_max_skew Command, Intel Quartus Prime Help

(2) Legal values for the -from and -to options are collections of clocks, registers, ports, pins, cells or partitions in a design.
2.6.7.3. Net Delay (set_net_delay)

Use the `set_net_delay` command to set the net delays and perform minimum or maximum timing analysis across nets.

The `-from` and `-to` options can be string patterns or pin, port, register, or net collections. When you use pin or net collection, include output pins or nets in the collection.

```
set_net_delay -from reg_a -to reg_c -max 20
```

<table>
<thead>
<tr>
<th>Table 30. set_net_delay Options</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Arguments</strong></td>
</tr>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>-h</td>
</tr>
<tr>
<td>-long_help</td>
</tr>
<tr>
<td>-from &lt;names&gt;</td>
</tr>
<tr>
<td>-get_value_from_clock_period &lt;src_clock_period</td>
</tr>
<tr>
<td>-max</td>
</tr>
<tr>
<td>-min</td>
</tr>
<tr>
<td>-to &lt;names&gt;</td>
</tr>
<tr>
<td>-value_multiplier &lt;multiplier&gt;</td>
</tr>
<tr>
<td>&lt;delay&gt;</td>
</tr>
</tbody>
</table>

If you use the `-min` option, the Timing Analyzer calculates slack by determining the minimum delay on the edge. If you use `-max` option, the Timing Analyzer calculates slack by determining the maximum edge delay.

Use `-get_value_from_clock_period` to set the net delay requirement as a multiple of the launching or latching clock period, or whichever of the two has a smaller or larger period. If you use this option, you must not set the positional delay option. If more than one clock clocks the set of nets, the Timing Analyzer uses the net with the smallest period to compute the constraint for a `-max` constraint, and the largest period for a `-min` constraint. If no clocks are clocking the endpoints of the net (that is, if the endpoints of the nets are not registers or constraint ports), the Timing Analyzer ignores the net delay constraint.

**Related Information**

- `report_net_delay Command, Intel Quartus Prime Help`

---

(3) If no option, or if option is a wildcard ("*") character, all the output pins and registers on timing netlist become valid destination points.

(4) If no option, or if option is a wildcard ("*") character, all the output pins and registers on timing netlist become valid destination points.
2.6.7.4. Create Timing Netlist

You can configure or load the timing netlist that the Timing Analyzer uses to calculate path delay data.

You must generate the timing netlist before running timing analysis. You can use the Create Timing Netlist dialog box or the Create Timing Netlist command in the Tasks pane. Create Timing Netlist also generates Advanced I/O Timing reports if you turn on Enable Advanced I/O Timing in the Timing Analyzer page of the Settings dialog box.

Note: The Compiler creates the timing netlist during compilation. The timing netlist does not reflect any configuration changes that occur after the device enters user mode, such as dynamic transceiver reconfiguration. This applies to all device families except transceivers on Intel Arria 10 devices with the Multiple Reconfiguration Profiles feature.

The following diagram shows how the Timing Analyzer interprets and classifies timing netlist data for a sample design.

![Figure 101. Division of Simple Design Schematic Elements in Timing Netlist](image)

2.6.8. Creating Timing Exceptions

Timing exceptions modify (or provide exception to) the default timing analysis behavior to account for your specific design conditions. Specify timing exceptions after specifying clocks and input and output delay constraints, because timing exceptions modify the default analysis.

2.6.8.1. Timing Exception Precedence

If the same clock or node names occur in multiple timing exceptions, the Timing Analyzer observes the following order of timing exception precedence:
1. **Set False Path** (`set_false_path`) is the first priority.

2. **Set Minimum Delay** (`set_min_delay`) and **Set Maximum Delay** (`set_max_delay`) are the second priority.

3. **Set Multicycle Path** (`set_multicycle_path`) is the third priority.

The false path timing exception has the highest precedence. Within each category, assignments to individual nodes have precedence over assignments to clocks. For exceptions of the same type:

1. `-from <node>` is the first priority.
2. `-to <node>` is the second priority.
3. `-thru <node>` is the third priority.
4. `-from <clock>` is the fourth priority.
5. `-to <clock>` is the fifth priority.

An asterisk wildcard (*) for any of these options applies the same precedence as not specifying the option at all. For example, `-from a -to *` is treated identically to `-from a` with regards precedence.

Precedence example:

1. `set_max_delay 1 -from x -to y`
2. `set_max_delay 2 -from x`
3. `set_max_delay 3 -to y`

The first exception has higher priority than either of the other two, since the first exception specifies a `-from` (while #3 doesn't) and specifies a `-to` (while #2 doesn't). In the absence of the first exception, the second exception has higher priority than the third, since the second exception specifies a `-from`, which the third does not. Finally, the remaining order of precedence for additional exceptions is order-dependent, such that the assignments most recently created overwrite, or partially overwrite, earlier assignments.

The `set_net_delay` and `set_max_skew` constraints analyze independently of minimum or maximum delays, or multicycle path constraints.

- The `set_net_delay` exception applies regardless the existence of a `set_false_path` exception, or `set_clock_groups` exception, on the same nodes applies on a net regardless of whether a `set_false_path` exception covers the net or whether a `set_clock_groups` command cuts the launching and latching clocks.

- The `set_max_skew` exception applies on paths that an asynchronous clock group cuts, but any exclusive clock group or false path exception overrides a `set_max_skew` constraint.

### 2.6.8.2. False Paths (set_false_path)

The **Set False Path** (`set_false_path`) constraint allows you to exclude a path from timing analysis, such as test logic or any other path not relevant to the circuit's operation. You can specify the source (`-from`), common through elements (`-thru`), and destination (`-to`) elements of that path.
The following SDC command makes false path exceptions from all registers starting with A, to all registers starting with B:

\[ \text{set\_false\_path \ -from } \{\text{get\_pins A*}\} \ -to \{\text{get\_pins B*}\} \]

You can specify either a point-to-point or clock-to-clock path as a false path. A false path’s -from and -to targets can be either nodes or clocks. However, the -thru targets can only be combinational nodes. For example, you can specify a false path for a static configuration register that writes once during power-up initialization, but does not change state again.

Although signals from static configuration registers often cross clock domains, you may not want to make false path exceptions to a clock-to-clock path, because some data may transfer across clock domains. However, you can selectively make false path exceptions from the static configuration register to all endpoints.

The Timing Analyzer assumes all clocks are related unless you specify otherwise. Use clock groups to more efficiently make false path exceptions between clocks, rather than writing multiple `set\_false\_path` exceptions between each clock transfer you want to eliminate.

**Related Information**
- Creating Clock Groups (`set\_clock\_groups`) on page 84
- `set\_false\_path` Command, Intel Quartus Prime Help

### 2.6.8.3. Minimum and Maximum Delays

To specify an absolute minimum or maximum delay for a path, use the **Set Minimum Delay** (`set\_min\_delay`) or the **Set Maximum Delay** (`set\_max\_delay`) constraints, respectively. Specifying minimum and maximum delay directly overwrites existing setup and hold relationships with the minimum and maximum values.

Use the `set\_max\_delay` and `set\_min\_delay` constraints for asynchronous signals that do not have a specific clock relationship in your design, but require a minimum and maximum path delay. You can create minimum and maximum delay exceptions for port-to-port paths through the device without a register stage in the path. If you use minimum and maximum delay exceptions to constrain the path delay, specify both the minimum and maximum delay of the path; do not constrain only the minimum or maximum value.

If the source or destination node is clocked, the Timing Analyzer takes into account the clock paths, allowing more or less delay on the data path. If the source or destination node has an input or output delay, the minimum or maximum delay check also includes that delay.

If you specify a minimum or maximum delay between timing nodes, the delay applies only to the path between the two nodes. If you specify a minimum or maximum delay for a clock, the delay applies to all paths where the clock clocks the source node or destination node.

You can create a minimum or maximum delay exception for an output port that does not have an output delay constraint. You cannot report timing for the paths that relate to the output port; however, the Timing Analyzer reports any slack for the path in the setup summary and hold summary reports. Because there is no clock that relates to the output port, the Timing Analyzer reports no clock for timing paths of the output port.
**Note:** To report timing with clock filters for output paths with minimum and maximum delay constraints, you can set the output delay for the output port with a value of zero. You can use an existing clock from the design or a virtual clock as the clock reference.

**Related Information**
- `set_max_delay` Command, Intel Quartus Prime Help
- `set_min_delay` Command, Intel Quartus Prime Help

### 2.6.8.4. Multicycle Paths

By default, the Timing Analyzer performs a single-cycle analysis, which is the most restrictive type of analysis. When analyzing a path without a multicycle constraint, the Timing Analyzer determines the setup launch and latch edge times by identifying the closest two active edges in the respective waveforms.

![Figure 102. Default Setup and Hold Relationship (No Multicycle)](default_setup_hold.png)

For hold time analysis, the timing analyzer analyzes the path for two timing conditions for every possible setup relationship, not just the worst-case setup relationship. Therefore, the hold launch and latch times can be unrelated to the setup launch and latch edges.

A multicycle constraint adjusts this default setup or hold relationship by the number of clock cycles you specify, based on the source (`-start`) or destination (`-end`) clock. A setup multicycle constraint of 2 extends the worst-case setup latch edge by one destination clock period. If you do not specify `-start` and `-end` values, the default constraint is `-end`.

![Figure 103. Setup and Hold Relationship with Multicycle = 2](setup_hold_multicycle.png)

Hold multicycle constraints derive from the default hold position (the default value is 0). An end hold multicycle constraint of 1 effectively subtracts one destination clock period from the default hold latch edge.

When the objects are timing nodes, the multicycle constraint only applies to the path between the two nodes. When an object is a clock, the multicycle constraint applies to all paths where the source node (`-from`) or destination node (`-to`) is clocked by the clock. When you adjust a setup relationship with a multicycle constraint, the default hold relationship adjusts automatically.

You can use timing constraints to modify either the launch or latch edge times that the Timing Analyzer uses to determine a setup relationship or hold relationship.
2.6.8.4.1. Common Multicycle Applications

Multicycle exceptions adjust the timing requirements for a register-to-register path, allowing the Fitter to optimally place and route a design. Two common multicycle applications are relaxing setup to allow a slower data transfer rate, and altering the setup to account for a phase shift.

2.6.8.4.2. Relaxing Setup with Multicycle (set_multicycle_path)

You can use a multicycle exception when the data transfer rate is slower than the clock cycle. Relaxing the setup relationship increases the window when timing analysis accepts data as valid.

In the following example, the source clock has a period of 10 ns, but the clock enable signal controls a group of latching registers, so the registers only enable every other cycle. The 10 ns clock feeds registers, so the Timing Analyzer reports a setup of 10 ns and a hold of 0 ns. However, the data is transferring every other cycle, so the Timing Analyzer must analyze the relationships as if the clock is operating at 20 ns. The result is a setup of 20 ns, while the hold remains 0 ns, thus extending the window for data recognition.

The following pair of multicycle assignments relax the setup relationship by specifying the -setup value of N and the -hold value as N-1. You must specify the hold relationship with a -hold assignment to prevent a positive hold requirement.

**Constraint to Relax Setup and Maintain Hold**

```
set_multicycle_path -setup -from src_reg* -to dst_reg* 2
set_multicycle_path -hold -from src_reg* -to dst_reg* 1
```
You can extend this pattern to create larger setup relationships to ease timing closure requirements. A common use for this exception is when writing to asynchronous RAM across an I/O interface. The delay between address, data, and a write enable may be several cycles. A multicycle exception to I/O ports allows extra time for the address and data to resolve before the enable occurs.

The following constraint relaxes the setup by three cycles:

**Three Cycle I/O Interface Constraint**

```
set_multicycle_path -setup -to [get_ports {SRAM_ADD[*] SRAM_DATA[*]}] 3
set_multicycle_path -hold -to [get_ports {SRAM_ADD[*] SRAM_DATA[*]}] 2
```

### 2.6.8.4.3. Accounting for a Phase Shift (-phase)

In the following example, the design contains a PLL that performs a phase-shift on a clock whose domain exchanges data with domains that do not experience the phase shift. This occurs when the destination clock phase-shifts forward, and the source clock does not shift. The default setup relationship becomes that phase-shift, thus shifting the window when data is valid.

For example, the following code phase-shifts one output of a PLL forward by a small amount, in this case 0.2 ns.

**Cross Domain Phase-Shift**

```
create_generated_clock -source pll|inclk[0] -name pll|clk[0] pll|clk[0]
```
The default setup relationship for this phase-shift is 0.2 ns, shown in Figure A, creating a scenario where the hold relationship is negative, which makes achieving timing closure nearly impossible.

**Figure 105. Phase-Shifted Setup and Hold**

-10 ns  0 ns  10 ns  20 ns

No Multicycles
(Default Relationship)

- Setup = 0.2 ns
- Hold = -9.8 ns

-10 ns  0 ns  10 ns  20 ns

Setup = 2

- Setup = 10.2 ns
- Hold = 0.2 ns

The following constraint allows the data to transfer to the following edge:

```plaintext
set_multicycle_path -setup -from [get_clocks clk_a] -to [get_clocks clk_b] 2
```

The hold relationship derives from the setup relationship, making a multicycle hold constraint unnecessary.

**Related Information**
- Same Frequency Clocks with Destination Clock Offset on page 111
- set_multicycle_path Command, Intel Quartus Prime Help

### 2.6.8.5. Multicycle Exception Examples

The examples in this section illustrate how the multicycle exceptions affect the default setup and hold analysis in the Timing Analyzer. The multicycle exceptions apply to a simple register-to-register circuit. Both the source and destination clocks are set to 10 ns.

#### 2.6.8.5.1. Default Multicycle Analysis

By default, the Timing Analyzer performs a single-cycle analysis to determine the setup and hold checks. Also, by default, the Timing Analyzer sets the end multicycle setup assignment value to one and the end multicycle hold assignment value to zero.

The source and the destination timing waveform for the source register and destination register, respectively where HC1 and HC2 are hold checks 1 and 2 and SC is the setup check.
**Figure 106. Default Timing Diagram**

The timing waveforms show the source and destination registers of a data transfer. HC1 and HC2 are the hold checks that Timing Analyzer performs. SC is the setup check that Timing Analyzer performs.

**Figure 107. Setup Check Calculation**

Setup check = current latch edge – closest previous launch edge

= 10 ns – 0 ns

= 10 ns

The most restrictive default single-cycle setup relationship, with an implied end multicycle setup assignment of one, is 10 ns.
Figure 108. Default Setup Report

<table>
<thead>
<tr>
<th>Path Summary</th>
<th>Statistics</th>
<th>Data Path</th>
<th>Waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Arrival Path</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Total</td>
<td>Incr</td>
<td>RF</td>
</tr>
<tr>
<td>1</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>2.603</td>
<td>2.603</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>2.603</td>
<td>2.603</td>
<td>R</td>
</tr>
<tr>
<td>2</td>
<td>2.603</td>
<td>0.000</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3.770</td>
<td>1.167</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>2.832</td>
<td>0.229</td>
<td>RR</td>
</tr>
<tr>
<td>2</td>
<td>2.991</td>
<td>0.159</td>
<td>RR</td>
</tr>
<tr>
<td>3</td>
<td>3.770</td>
<td>0.779</td>
<td>RR</td>
</tr>
<tr>
<td>4</td>
<td>3.770</td>
<td>0.000</td>
<td>RR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Data Required Path

|               | Total      | Incr      | RF       | Type    | Element          |
| 1             | 10.000     | 10.000    |          |         | latch edge time  |
| 2             | 10.000     | 0.000     |          | borrow  | time borrowed   |
| 3             | 11.983     | 1.983     |          |         | clock path      |
| 1             | 11.983     | 1.983     | R        |         | clock network delay |
| 4             | 11.953     | -0.030    |          |         | clock uncertainty |
| 5             | 11.996     | 0.043     | uTsu     |         | dst              |

Figure 109. Hold Check Calculation

The figure shows the setup timing report with the launch and latch edge times highlighted.

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 0 \text{ ns} \\
= 0 \text{ ns}
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 10 \text{ ns} - 10 \text{ ns} \\
= 0 \text{ ns}
\]

The most restrictive default single-cycle hold relationship, with an implied end multicycle hold assignment of zero, is 0ns.
Figure 110. Default Hold Report

The figure shows the hold timing report with the launch and latch edge times highlighted.

<table>
<thead>
<tr>
<th>Path #1: Hold slack is 0.230</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path Summary</td>
</tr>
<tr>
<td>Data Arrival Path</td>
</tr>
<tr>
<td>Total</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Data Required Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
</tbody>
</table>

2.6.8.5.2. End Multicycle Setup = 2 and End Multicycle Hold = 0

In this example, the end multicycle setup assignment value is two, and the end multicycle hold assignment value is zero.

Multicycle Constraint

```
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \
 -setup -end 2
```
The Timing Analyzer does not require an end multicycle hold value because the default end multicycle hold value is zero.

In this example, the setup relationship relaxes by a full clock period by moving the latch edge to the next latch edge. The hold analysis is does not change from the default settings. The following shows the setup timing diagram for the analysis that the Timing Analyzer performs. The latch edge is a clock cycle later than in the default single-cycle analysis.

**Figure 111. Setup Timing Diagram**

The figure shows the setup timing diagram for the analysis that the Timing Analyzer performs. Without the multicycle constraint the latching edge is edge 1. However, with the multicycle constraint the latching edge is edge 2.

**Figure 112. Setup Check Calculation**

setup check = current latch edge – closest previous launch edge
= 20 ns – 0 ns
= 20 ns

The most restrictive setup relationship with an end multicycle setup assignment of two is 20 ns. The following shows the setup report in the Timing Analyzer and highlights the launch and latch edges.
Figure 113. Setup Report with Setup Multicycle Exception

### Data Arrival Path

<table>
<thead>
<tr>
<th>Total</th>
<th>Incr</th>
<th>RF</th>
<th>Type</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
<td>launch edge time</td>
</tr>
<tr>
<td>2</td>
<td>0.000</td>
<td>0.000</td>
<td>borrow</td>
<td>time borrowed</td>
</tr>
<tr>
<td>3</td>
<td>2.603</td>
<td>2.603</td>
<td></td>
<td>clock path</td>
</tr>
<tr>
<td>1</td>
<td>2.603</td>
<td>2.603</td>
<td>R</td>
<td>clock network delay</td>
</tr>
<tr>
<td>2</td>
<td>2.603</td>
<td>0.000</td>
<td>src</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>3.770</td>
<td>1.167</td>
<td></td>
<td>data path</td>
</tr>
<tr>
<td>1</td>
<td>2.832</td>
<td>0.229</td>
<td>RR</td>
<td>uTco</td>
</tr>
<tr>
<td>2</td>
<td>2.991</td>
<td>0.159</td>
<td>RR</td>
<td>CELL</td>
</tr>
<tr>
<td>3</td>
<td>3.770</td>
<td>0.779</td>
<td>RR</td>
<td>IC</td>
</tr>
<tr>
<td>4</td>
<td>3.770</td>
<td>0.000</td>
<td>RR</td>
<td>CELL</td>
</tr>
</tbody>
</table>

### Data Required Path

<table>
<thead>
<tr>
<th>Total</th>
<th>Incr</th>
<th>RF</th>
<th>Type</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>20.000</td>
<td>20.000</td>
<td></td>
<td>latch edge time</td>
</tr>
<tr>
<td>2</td>
<td>20.000</td>
<td>0.000</td>
<td>borrow</td>
<td>time borrowed</td>
</tr>
<tr>
<td>3</td>
<td>21.983</td>
<td>1.983</td>
<td></td>
<td>clock path</td>
</tr>
<tr>
<td>1</td>
<td>21.983</td>
<td>1.983</td>
<td>R</td>
<td>clock network delay</td>
</tr>
<tr>
<td>4</td>
<td>21.953</td>
<td>-0.030</td>
<td></td>
<td>clock uncertainty</td>
</tr>
<tr>
<td>5</td>
<td>21.996</td>
<td>0.043</td>
<td>uTsu</td>
<td>dst</td>
</tr>
</tbody>
</table>

Because the multicycle hold latch and launch edges are the same as the results of hold analysis with the default settings, the multicycle hold analysis in this example is equivalent to the single-cycle hold analysis. The hold checks are relative to the setup check. Normally, the Timing Analyzer performs hold checks on every possible setup check, not only on the most restrictive setup check edges.
Figure 114. Hold Timing Diagram
The figure shows the hold latching edges are now at 10 and 20 ns, instead of 0 and 10 ns.

Figure 115. Hold Report with Setup Multicycle Exception
Path #1: Hold slack is -9.770 (VIOLATED)

<table>
<thead>
<tr>
<th>Data Arrival Path</th>
<th>Total</th>
<th>Incr</th>
<th>RF</th>
<th>Type</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
<td>launch edge time</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0.000</td>
<td>0.000</td>
<td></td>
<td>borrow</td>
<td>time borrowed</td>
</tr>
<tr>
<td>3</td>
<td>1.012</td>
<td>1.012</td>
<td></td>
<td>clock path</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1.012</td>
<td>1.012</td>
<td>R</td>
<td>clock network delay</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1.012</td>
<td>0.000</td>
<td></td>
<td>src</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1.529</td>
<td>0.517</td>
<td></td>
<td>data path</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1.113</td>
<td>0.101</td>
<td>RR</td>
<td>uTco</td>
<td>src</td>
</tr>
<tr>
<td>2</td>
<td>1.175</td>
<td>0.062</td>
<td>RR</td>
<td>CELL</td>
<td>src~la_lab/laboutb[16]</td>
</tr>
<tr>
<td>3</td>
<td>1.529</td>
<td>0.354</td>
<td>RR</td>
<td>IC</td>
<td>dst</td>
</tr>
<tr>
<td>4</td>
<td>1.529</td>
<td>0.000</td>
<td>RR</td>
<td>CELL</td>
<td>dst</td>
</tr>
</tbody>
</table>

Data Required Path

<table>
<thead>
<tr>
<th>Total</th>
<th>Incr</th>
<th>RF</th>
<th>Type</th>
<th>Element</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>10.000</td>
<td>10.000</td>
<td>latch edge time</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>10.000</td>
<td>0.000</td>
<td>borrow</td>
<td>time borrowed</td>
</tr>
<tr>
<td>3</td>
<td>11.134</td>
<td>1.134</td>
<td>clock path</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>11.134</td>
<td>1.134</td>
<td>R</td>
<td>clock network delay</td>
</tr>
<tr>
<td>4</td>
<td>11.164</td>
<td>0.030</td>
<td>clock uncertainty</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>11.299</td>
<td>0.135</td>
<td>uTh</td>
<td>dst</td>
</tr>
</tbody>
</table>
Figure 116. Hold Check Calculation

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 10 \text{ ns} \\
= -10 \text{ ns} \\
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 10 \text{ ns} - 20 \text{ ns} \\
= -10 \text{ ns} \\
\]

2.6.8.5.3. End Multicycle Setup = 2 and End Multicycle Hold = 1

In this example, the end multicycle setup assignment value is two, and the end multicycle hold assignment value is one.

Multicycle Constraint

\[
\text{set_multicycle_path} \text{-from [get_clocks clk_src] -to [get_clocks clk_dst]} \text{-setup -end 2} \\
\text{set_multicycle_path} \text{-from [get_clocks clk_src] -to [get_clocks clk_dst]} \text{-hold -end 1} \\
\]

In this example, the setup relationship relaxes by one clock period by moving the latching edge to the right of the default latching edge by 1 clock period. The hold relationship relaxes by one clock period by moving the latch edges to the left of the default latching edges by one.

The following shows the setup timing diagram for the analysis that the Timing Analyzer performs:

Figure 117. Setup Timing Diagram

Figure 118. Setup Check Calculation

\[
\text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \\
= 20 \text{ ns} - 0 \text{ ns} \\
= 20 \text{ ns} \\
\]
The most restrictive hold relationship with an end multicycle setup assignment value of two is 20 ns.

The following shows the setup report for this example in the Timing Analyzer and highlights the launch and latch edges.

**Figure 119. Setup Report with Setup and Hold Multicycle Exception**

<table>
<thead>
<tr>
<th>Path #1: Setup slack is 18.226</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path Summary</td>
</tr>
<tr>
<td>Data Arrival Path</td>
</tr>
<tr>
<td>Total</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
</tbody>
</table>

| Data Required Path | | | |
|------------------|--------|--------|
| Total | Incr | RF | Type | Element |
| 1 | 20.000 | 20.000 | | latch edge time |
| 2 | 20.000 | 0.000 | | borrow time borrowed |
| 3 | 21.983 | 1.983 | | clock path |
| 1 | 21.983 | 1.983 | R | clock network delay |
| 4 | 21.953 | -0.030 | | clock uncertainty |
| 5 | 21.996 | 0.043 | | uTs dst |

The following shows the timing diagram for the hold checks for this example. The hold checks are relative to the setup check.
**Figure 120. Hold Timing Diagram**

![Hold Timing Diagram](image)

**Figure 121. Hold Check Calculation**

\[
\begin{align*}
\text{hold check 1} &= \text{current launch edge} - \text{previous latch edge} \\
&= 0 \text{ ns} - 0 \text{ ns} \\
&= 0 \text{ ns}
\end{align*}
\]

\[
\begin{align*}
\text{hold check 2} &= \text{next launch edge} - \text{current latch edge} \\
&= 10 \text{ ns} - 10 \text{ ns} \\
&= 0 \text{ ns}
\end{align*}
\]

The most restrictive hold relationship with an end multicycle setup assignment value of two and an end multicycle hold assignment value of one is 0 ns.

The following shows the hold report for this example in the Timing Analyzer and highlights the launch and latch edges.
Figure 122. Hold Report with Setup and Hold Multicycle Exception

<table>
<thead>
<tr>
<th>Path Summary</th>
<th>Statistics</th>
<th>Data Path</th>
<th>Waveform</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Arrival Path</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0.000</td>
<td>0.000</td>
<td>launch edge time</td>
</tr>
<tr>
<td>2</td>
<td>0.000</td>
<td>0.000</td>
<td>borrow</td>
</tr>
<tr>
<td>3</td>
<td>▼ 1.012</td>
<td>1.012</td>
<td>clock path</td>
</tr>
<tr>
<td>1</td>
<td>1.012</td>
<td>1.012</td>
<td>R</td>
</tr>
<tr>
<td>2</td>
<td>1.012</td>
<td>0.000</td>
<td>src</td>
</tr>
<tr>
<td>4</td>
<td>▼ 1.529</td>
<td>0.517</td>
<td>data path</td>
</tr>
<tr>
<td>1</td>
<td>1.113</td>
<td>0.101</td>
<td>RR</td>
</tr>
<tr>
<td>2</td>
<td>1.175</td>
<td>0.062</td>
<td>RR</td>
</tr>
<tr>
<td>3</td>
<td>1.529</td>
<td>0.354</td>
<td>RR</td>
</tr>
<tr>
<td>4</td>
<td>1.529</td>
<td>0.000</td>
<td>RR</td>
</tr>
</tbody>
</table>

| Data Required Path | | | |
| 1 | 0.000 | 0.000 | latch edge time |
| 2 | 0.000 | 0.000 | borrow | time borrowed |
| 3 | ▼ 1.134 | 1.134 | clock path |
| 1 | 1.134 | 1.134 | R | clock network delay |
| 4 | 1.164 | 0.030 | clock uncertainty |
| 5 | 1.299 | 0.135 | uTh | dst |

2.6.8.5.4. Same Frequency Clocks with Destination Clock Offset

In this example, the source and destination clocks have the same frequency, but the destination clock is offset with a positive phase shift. Both the source and destination clocks have a period of 10 ns. The destination clock has a positive phase shift of 2 ns with respect to the source clock.

The following example shows a design with the same frequency clocks and a destination clock offset.
Figure 123. Same Frequency Clocks with Destination Clock Offset Diagram

The following timing diagram shows the default setup check analysis that the Timing Analyzer performs.

Figure 124. Setup Timing Diagram

Figure 125. Setup Check Calculation

\[
\text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \\
= 2 \text{ ns} - 0 \text{ ns} \\
= 2 \text{ ns}
\]

The setup relationship shown is too pessimistic and is not the setup relationship required for typical designs. To adjust the default analysis, you assign an end multicycle setup exception of two. The following shows a multicycle exception that adjusts the default analysis:

**Multicycle Constraint**

```
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \ 
-setup -end 2
```
The following timing diagram shows the preferred setup relationship for this example:

**Figure 126. Preferred Setup Relationship**

![Preferred Setup Relationship Diagram]

The following timing diagram shows the default hold check analysis that the Timing Analyzer performs with an end multicycle setup value of two.

**Figure 127. Default Hold Check**

![Default Hold Check Diagram]

**Figure 128. Hold Check Calculation**

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 2 \text{ ns} \\
= -2 \text{ ns}
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 10 \text{ ns} - 12 \text{ ns} \\
= -2 \text{ ns}
\]

In this example, the default hold analysis returns the preferred hold requirements and no multicycle hold exceptions are required.
The associated setup and hold analysis if the phase shift is -2 ns. In this example, the default hold analysis is correct for the negative phase shift of 2 ns, and no multicycle exceptions are required.

**Figure 129. Negative Phase Shift**

The figure shows an example of the setup and hold analysis for a negative phase shift of -2 ns. In this example, the default setup and hold analysis are correct, and no multicycle exceptions are required.

---

**2.6.8.5.5. Destination Clock Frequency is a Multiple of the Source Clock Frequency**

In this example, the destination clock frequency value of 5 ns is an integer multiple of the source clock frequency of 10 ns. The destination clock frequency can be an integer multiple of the source clock frequency when a PLL generates both clocks with a phase shift on the destination clock.

The following example shows a design in which the destination clock frequency is a multiple of the source clock frequency.

**Figure 130. Destination Clock is Multiple of Source Clock**
The following timing diagram shows the default setup check analysis that the Timing Analyzer performs:

**Figure 131. Setup Timing Diagram**

![Setup Timing Diagram](image)

**Figure 132. Setup Check Calculation**

\[
\text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \\
= 5 \text{ ns} - 0 \text{ ns} \\
= 5 \text{ ns}
\]

The setup relationship demonstrates that the data requires capture at edge two; therefore, you can relax the setup requirement. To correct the default analysis, you shift the latch edge by one clock period with an end multicycle setup exception of two. The following multicycle exception assignment adjusts the default analysis in this example:

**Multicycle Constraint**

```
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \
    -setup -end 2
```

The following timing diagram shows the preferred setup relationship for this example:

**Figure 133. Preferred Setup Analysis**

![Preferred Setup Analysis](image)
The following timing diagram shows the default hold check analysis the Timing Analyzer performs with an end multicycle setup value of two.

**Figure 134. Default Hold Check**

![Timing Diagram](image)

**Figure 135. Hold Check Calculation**

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 5 \text{ ns} \\
= -5 \text{ ns}
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 10 \text{ ns} - 10 \text{ ns} \\
= 0 \text{ ns}
\]

In this example, hold check one is too restrictive. The data is launched by the edge at 0 ns and must check against the data captured by the previous latch edge at 0 ns, which does not occur in hold check one. To correct the default analysis, you must use an end multicycle hold exception of one.

**2.6.8.5.6. Destination Clock Frequency is a Multiple of the Source Clock Frequency with an Offset**

This example is a combination of the previous two examples. The destination clock frequency is an integer multiple of the source clock frequency, and the destination clock has a positive phase shift. The destination clock frequency is 5 ns, and the source clock frequency is 10 ns. The destination clock also has a positive offset of 2 ns with respect to the source clock. The destination clock frequency can be an integer multiple of the source clock frequency. The destination clock frequency can be with an offset when a PLL generates both clocks with a phase shift on the destination clock.

The following example shows a design in which the destination clock frequency is a multiple of the source clock frequency with an offset.
2. Using the Intel Quartus Prime Timing Analyzer

Figure 136. Destination Clock is Multiple of Source Clock with Offset

![Diagram of circuitry with REG1, REG2, Combinational Logic, SET, and D Q]

The timing diagram for the default setup check analysis the Timing Analyzer performs.

Figure 137. Setup Timing Diagram

![Diagram showing REG1.CLK and REG2.CLK with launch and latch edges]

Figure 138. Setup Check Calculation

\[
\text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \\
= 2 \text{ ns} - 0 \text{ ns} \\
= 2 \text{ ns}
\]

The setup relationship in this example demonstrates that the data does not require capture at edge one, but rather requires capture at edge three; therefore, you can relax the setup requirement. To adjust the default analysis, you shift the latch edge by two clock periods, and specify an end multicycle setup exception of three.

The multicycle exception adjusts the default analysis in this example:

**Multicycle Constraint**

```
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \ 
-setup -end 3
```

The timing diagram for the preferred setup relationship for this example.
The following timing diagram shows the default hold check analysis that the Timing Analyzer performs with an end multicycle setup value of three:

In this example, the hold check one is too restrictive. The data is launched by the edge at 0 ns, and must check against the data that the previous latch edge at 2ns captures. You can use the multicycle hold assignment of 1 to correct this.
**2.6.8.5.7. Source Clock Frequency is a Multiple of the Destination Clock Frequency**

In this example, the source clock frequency value of 5 ns is an integer multiple of the destination clock frequency of 10 ns. The source clock frequency can be an integer multiple of the destination clock frequency when a PLL generates both clocks and uses different multiplication and division factors.

In the following example the source clock frequency is a multiple of the destination clock frequency:

**Figure 142. Source Clock Frequency is Multiple of Destination Clock Frequency:**

![Timing Diagram](image)

The following timing diagram shows the default setup check analysis the Timing Analyzer performs:

**Figure 143. Default Setup Check Analysis**

![Setup Check Diagram](image)

**Figure 144. Setup Check Calculation**

\[
\text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \\
= 10 \text{ ns} - 5 \text{ ns} \\
= 5 \text{ ns}
\]

The setup relationship demonstrates that the data launched at edge one does not require capture, and the data launched at edge two requires capture; therefore, you can relax the setup requirement. To correct the default analysis, you shift the launch edge by one clock period with a start multicycle setup exception of two. The following multicycle exception adjusts the default analysis in this example:

**Multicycle Constraint**

```bash
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \\
-setup -start 2
```
The following timing diagram shows the preferred setup relationship for this example:

**Figure 145. Preferred Setup Check Analysis**

The following timing diagram shows the default hold check analysis the Timing Analyzer performs for a start multicycle setup value of two:

**Figure 146. Default Hold Check**

**Figure 147. Hold Check Calculation**

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 0 \text{ ns} \\
= 0 \text{ ns}
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 5 \text{ ns} - 10 \text{ ns} \\
= -5 \text{ ns}
\]

In this example, the hold check two is too restrictive. The data is launched next by the edge at 10 ns and must check against the data captured by the current latch edge at 10 ns, which does not occur in hold check two. To correct the default analysis, you use a start multicycle hold exception of one.
2.6.8.5.8. Source Clock Frequency is a Multiple of the Destination Clock Frequency with an Offset

In this example, the source clock frequency is an integer multiple of the destination clock frequency and the destination clock has a positive phase offset. The source clock frequency is 5 ns and destination clock frequency is 10 ns. The destination clock also has a positive offset of 2 ns with respect to the source clock. The source clock frequency can be an integer multiple of the destination clock frequency with an offset when a PLL generates both clocks with different multiplication.

Figure 148. Source Clock Frequency is Multiple of Destination Clock Frequency with Offset

The following timing diagram shows the default setup check analysis the Timing Analyzer performs:

Figure 149. Setup Timing Diagram

Figure 150. Setup Check Calculation

\[ \text{setup check} = \text{current latch edge} - \text{closest previous launch edge} \]
\[ = 12 \text{ ns} - 10 \text{ ns} \]
\[ = 2 \text{ ns} \]

The setup relationship in this example demonstrates that the data is not launched at edge one, and the data that is launched at edge three must be captured; therefore, you can relax the setup requirement. To correct the default analysis, you shift the launch edge by two clock periods with a start multicycle setup exception of three.
The following multicycle exception adjusts the default analysis in this example:

**Multicycle Constraint**

```
set_multicycle_path -from [get_clocks clk_src] -to [get_clocks clk_dst] \
   -setup -start 3
```

The following timing diagram shows the preferred setup relationship for this example:

**Figure 151. Preferred Setup Check Analysis**

![Diagram showing preferred setup relationship](image)

The Timing Analyzer performs the following calculation to determine the hold check:

**Figure 152. Hold Check Calculation**

\[
\text{hold check 1} = \text{current launch edge} - \text{previous latch edge} \\
= 0 \text{ ns} - 2 \text{ ns} \\
= -2 \text{ ns}
\]

\[
\text{hold check 2} = \text{next launch edge} - \text{current latch edge} \\
= 5 \text{ ns} - 12 \text{ ns} \\
= -7 \text{ ns}
\]
The following timing diagram shows the default hold check analysis the Timing Analyzer performs for a start multicycle setup value of three:

**Figure 153. Default Hold Check Analysis**

![Timing Diagram](image)

In this example, the hold check two is too restrictive. The data is launched next by the edge at 10 ns and must check against the data captured by the current latch edge at 12 ns, which does not occur in hold check two. To correct the default analysis, you must specify a multicycle hold exception of one.

### 2.6.8.6. Delay Annotation

To modify the default delay values used during timing analysis, use the `set_annotated_delay` and `set_timing_derate` commands. You must update the timing netlist to apply these commands.

To specify different operating conditions in a single `.sdc` file, rather than having multiple `.sdc` files that specify different operating conditions, use the `set_annotated_delay -operating_conditions` command.

**Related Information**
- `set_timing_derate` Command, Intel Quartus Prime Help
- `set_annotated_delay` Command, Intel Quartus Prime Help

### 2.6.8.7. Constraining Design Partition Ports

You can assign clock definitions and SDC exceptions to design partition ports. The block-based design and partial reconfiguration design flows require the use of design partitions.

The Compiler represents design partition ports in your timing netlist as combinational nodes with persistent names that the Compiler cannot optimize away. You can safely refer to these ports as clock sources or -through points in SDC constraints. You can also use design partition port names as -to and -from points in the `report_path` command.

If a port on `partition_a` has the name `clk_divide` the SDC constraint is:

```plaintext
create_generated_clock -source clock -divide_by 2 \
   top|partition_a|clk_divide
```
If a set of ports on `partition_b` has the name `data_input[0..7]` the SDC constraint is:

```
set_multicycle_path -from top|partition_a|data_reg* \
   -through top|partition_b|data_input* 2
```

You can use multiple `-through` clauses. This allows you to specify paths that go through output ports of one design partition and through the input ports of another, downstream design partition.

To add constraints to partition ports:

1. Run Analysis & Synthesis or run full compilation on a design containing design partitions.
2. To open the RTL Viewer and locate the partition ports of interest, click `Tools ➤ Netlist Viewers ➤ RTL Viewer`.
3. Using the same names as the RTL Viewer, add clock and other SDC constraints to the `.sdc` file for your project. You can use wildcards to refer to more than one port.
4. Recompile the design to apply the new definitions and constraints.

Aside from block-based and PR flows, this technique also aids in emulation of ASICs using FPGAs. In this type of design, clock networks often span multiple hierarchies of partitions. Typically designers remove the clock-dividing circuitry from the netlist, since they cannot easily emulate this circuitry on Intel FPGAs. For such clock networks, this technique allows you to define different versions of the clock signal in places where the circuitry is removed.

You must design and place your partitions strategically, and then define the appropriate ports on these partitions. Ensure that your ports and partitions coincide with the part of the clock network which contains the special circuitry. You can manually edit the emulated ASIC netlist to annotate appropriate clock definitions and clock relationships. You can also use this technique in any projects where arbitrary locations on paths require constrained timing or defined clock sources.

**Related Information**
- [Output Constraints (set_output_delay)](page 91)
- [Input Constraints (set_input_delay)](page 90)
- Intel Quartus Prime Pro Edition User Guide: Block-Based Design

### 2.6.9. Using Fitter Overconstraints

Fitter overconstraints are timing constraints that you adjust to overcome modeling inaccuracies, mis-correlation, or other deficiencies in logic optimization. You can overconstrain setup and hold paths in the Fitter to force more aggressive timing optimization of specific paths.

**Overconstraints for Intel Stratix 10 Designs**

When designing for Intel Stratix 10 devices, you can target specific nodes with Fitter overconstraints to prevent the Compiler from retiming and optimizing these paths (nodes may have multiple timing requirements and the Compiler treats as “don’t
If the constraint targets specific nodes, use the `is_post_route` Tcl function. This function allows you to apply overconstraints and adjust slack for modules of the Fitter (Plan, Place, Route), while allowing post-route retiming and not affecting sign-off timing analysis.

```tcl
# Example Fitter overconstraint targeting specific nodes (allows for post-route retiming)
if [ ! [is_post_route]] {
    set_max_delay -from ${my_src_regs} -to ${my_dst_regs} 1ns
}
```

**Note:** The `is_post_route` function is inclusive. To exclude the function, use the negation syntax (`!`).

### Overconstraints for Designs that Target All Other Device Families

You can assign Fitter overconstraints that check the name of the current executable, (either `quartus_fit` or `quartus_sta`) to apply different constraints for Fitter optimization and sign-off timing analysis.

```tcl
set fit_flow 0
if { $::TimingAnalyzerInfo(nameofexecutable) == "quartus_fit" } {
    set fit_flow 1
}
if {$fit_flow} {
    # Example Fitter overconstraint targeting specific nodes (restricts retiming)
    set_max_delay -from ${my_src_regs} -to ${my_dst_regs} 1ns
}
```

## 2.6.10. Example Circuit and SDC File

The following circuit and corresponding `.sdc` file demonstrates constraining a design that includes two clocks, a phase-locked loop (PLL), and other common synchronous design elements.
The .sdc file contains basic constraints for the example circuit.

Example 6. Basic .sdc Constraints Example

```vhdl
# Create clock constraints
create_clock -name clockone -period 10.000 [get_ports {clk1}]
create_clock -name clocktwo -period 10.000 [get_ports {clk2}]
# Create virtual clocks for input and output delay constraints
create_clock -name clockone_ext -period 10.000
create_clock -name clocktwo_ext -period 10.000
derive_pll_clocks
# derive clock uncertainty
derive_clock_uncertainty
# Specify that clockone and clocktwo are unrelated by assigning
# them to separate asynchronous groups
set_clock_groups \
  -asynchronous \n  -group {clockone} \n  -group {clocktwo altp110|altp11_component|auto_generated|pll1|clk[0]}
# set input and output delays
set_input_delay -clock { clockone_ext } -max 4 [get_ports {data1}]
set_input_delay -clock { clockone_ext } -min -1 [get_ports {data1}]
set_input_delay -clock { clocktwo_ext } -max 4 [get_ports {data2}]
set_input_delay -clock { clocktwo_ext } -min -1 [get_ports {data2}]
set_output_delay -clock { clocktwo_ext } -max 6 [get_ports {dataout}]
set_output_delay -clock { clocktwo_ext } -min -3 [get_ports {dataout}]
```
The .sdc file contains the following basic constraints that you typically include for most designs:

- Definitions of `clockone` and `clocktwo` as base clocks, and assignment of those constraints to nodes in the design.
- Definitions of `clockone_ext` and `clocktwo_ext` as virtual clocks, which represent clocks driving external devices interfacing with the FPGA.
- Automated derivation of generated clocks on PLL outputs.
- Derivation of clock uncertainty.
- Specification of two clock groups, the first containing `clockone` and its related clocks, the second containing `clocktwo` and its related clocks, and the third group containing the output of the PLL. This specification overrides the default analysis of all clocks in the design as related to each other.
- Specification of input and output delays for the design.

**Related Information**

Asynchronous Clock Groups (-asynchronous) on page 86

### 2.7. Timing Analyzer Tcl Commands

You can optionally use Tcl commands from the Intel Quartus Prime software Tcl Application Programming Interface (API) to constrain, analyze, and collect timing information for your design. This section describes running the Timing Analyzer and setting constraints using Tcl commands. You can alternatively perform these same functions in the Timing Analyzer GUI. Tcl .sdc extensions provide additional methods for controlling timing analysis and reporting. The following Tcl packages support the Tcl timing analysis commands this chapter describes:

- `::quartus::sta`
- `::quartus::sdc`
- `::quartus::sdc_ext`

**Related Information**

- `::quartus::sta`
  For more information about Timing Analyzer Tcl commands and a complete list of commands, refer to Intel Quartus Prime Help.
- `::quartus::sdc`
  For more information about standard SDC commands and a complete list of commands, refer to Intel Quartus Prime Help.
- `::quartus::sdc_ext`
  For more information about Intel FPGA extensions of SDC commands and a complete list of commands, refer to Intel Quartus Prime Help.

### 2.7.1. The `quartus_sta` Executable

The `quartus_sta` executable allows you to run timing analysis without running the full Intel Quartus Prime software GUI. The following methods are available:
To run the Timing Analyzer as a stand-alone GUI application, type the following at the command prompt:

```
quartus_staw
```

To run the Timing Analyzer in interactive command-shell mode, type the following at the command prompt:

```
quartus_sta -s
```

To run timing analysis from a system command prompt, type the following command:

```
quartus_sta <options><project_name>
```

You can optionally use command line options available to perform iterative timing analysis on large designs. You can perform a less intensive analysis with `quartus_sta --mode=implement`. In this mode, the Intel Quartus Prime software performs a reduced-corner timing analysis. When you achieve the desired result, you can use `quartus_sta --mode=finalize` to perform final Fitter optimizations and a full multi-corner timing analysis under all operating conditions.

### Table 32. quartus_sta Command-Line Options

<table>
<thead>
<tr>
<th>Command-Line Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-h</td>
<td>--help</td>
</tr>
<tr>
<td>-t &lt;script file&gt;</td>
<td>--script=&lt;script file&gt;</td>
</tr>
<tr>
<td>-s</td>
<td>--shell</td>
</tr>
<tr>
<td>--tcl_eval &lt;tcl command&gt;</td>
<td>Evaluates the Tcl command &lt;tcl command&gt;.</td>
</tr>
<tr>
<td>--do_report_timing</td>
<td>For all clocks in the design, run the following commands:</td>
</tr>
<tr>
<td></td>
<td>report_timing -paths 1 -to_clock $clock</td>
</tr>
<tr>
<td></td>
<td>report_timing -setup -paths 1 -to_clock $clock</td>
</tr>
<tr>
<td></td>
<td>report_timing -hold -paths 1 -to_clock $clock</td>
</tr>
<tr>
<td></td>
<td>report_timing -recovery -paths 1 -to_clock $clock</td>
</tr>
<tr>
<td></td>
<td>report_timing -removal -paths 1 -to_clock $clock</td>
</tr>
<tr>
<td>--force_dat</td>
<td>Forces an update of the project database with new delay information.</td>
</tr>
<tr>
<td>--lower_priority</td>
<td>Lowers the computing priority of the quartus_sta process.</td>
</tr>
<tr>
<td>--post_map</td>
<td>Uses the post-map database results.</td>
</tr>
<tr>
<td>--sdc=&lt;SDC file&gt;</td>
<td>Specifies the .sdc file to use.</td>
</tr>
<tr>
<td>--report_script=&lt;custom script&gt;</td>
<td>Specifies a custom report script to call.</td>
</tr>
<tr>
<td>--speed=&lt;value&gt;</td>
<td>Specifies the device speed grade used for timing analysis.</td>
</tr>
<tr>
<td>-f &lt;argument file&gt;</td>
<td>Specifies a file containing additional command-line arguments.</td>
</tr>
<tr>
<td>-c &lt;revision name&gt;</td>
<td>--rev=&lt;revision name&gt;</td>
</tr>
<tr>
<td></td>
<td>Settings File (.qsf) to use.</td>
</tr>
<tr>
<td>--multicorner</td>
<td>Specifies that the Timing Analyzer generates all slack summary reports for</td>
</tr>
<tr>
<td></td>
<td>both slow- and fast-corners.</td>
</tr>
<tr>
<td>--multicorner=[on</td>
<td>off]</td>
</tr>
</tbody>
</table>

continued...
### Command-Line Option

<table>
<thead>
<tr>
<th>Command-Line Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--voltage=&lt;value_in_mV&gt;</td>
<td>Specifies the device voltage, in mV used for timing analysis.</td>
</tr>
<tr>
<td>--temperature=&lt;value_in_C&gt;</td>
<td>Specifies the device temperature in degrees Celsius, used for timing analysis.</td>
</tr>
<tr>
<td>--parallel [=num_processors&gt;]</td>
<td>Specifies the number of computer processors to use on a multiprocessor system.</td>
</tr>
<tr>
<td>--mode=implement</td>
<td>finalize</td>
</tr>
</tbody>
</table>

### 2.7.2. Collection Commands

The Timing Analyzer supports collection commands that provide easy access to ports, pins, cells, or nodes in the design. Use collection commands with any constraints or Tcl commands specified in the Timing Analyzer.

#### Table 33. Collection Commands

<table>
<thead>
<tr>
<th>Command</th>
<th>Collection Returned</th>
</tr>
</thead>
<tbody>
<tr>
<td>all_clocks</td>
<td>All clocks in the design</td>
</tr>
<tr>
<td>all_inputs</td>
<td>All input ports in the design.</td>
</tr>
<tr>
<td>all_outputs</td>
<td>All output ports in the design.</td>
</tr>
<tr>
<td>all_registers</td>
<td>All registers in the design.</td>
</tr>
<tr>
<td>get_cells</td>
<td>Cells in the design. All cell names in the collection match the specified pattern. Wildcards can be used to select multiple cells at the same time.</td>
</tr>
<tr>
<td>get_clocks</td>
<td>Lists clocks in the design. When used as an argument to another command, such as the -from or -to of set_multicycle_path, each node in the clock represents all nodes clocked by the clocks in the collection. The default uses the specific node (even if the node is a clock) as the target of a command. The -of_objects option takes a node like a register and returns the clocks that drive it.</td>
</tr>
<tr>
<td>get_nets</td>
<td>Nets in the design. All net names in the collection match the specified pattern. You can use wildcards to select multiple nets at the same time.</td>
</tr>
<tr>
<td>get_pins</td>
<td>Pins in the design. All pin names in the collection match the specified pattern. You can use wildcards to select multiple pins at the same time.</td>
</tr>
<tr>
<td>get_ports</td>
<td>All ports (design inputs and outputs) in the design.</td>
</tr>
<tr>
<td>get_registers</td>
<td>Gets the specified registers in the design.</td>
</tr>
<tr>
<td>get_keepers</td>
<td>Gets the specified keepers in the design. Keepers are I/O ports or registers.</td>
</tr>
</tbody>
</table>

You can also examine collections and experiment with collections using wildcards in the Timing Analyzer by clicking Name Finder from the View menu.

#### 2.7.2.1. Wildcard Characters

To apply constraints to many nodes in a design, use the "*" and "?" wildcard characters. The "*" wildcard character matches any string; the "?" wildcard character matches any single character.
If you apply a constraint to node `reg*`, the Timing Analyzer searches for and applies the constraint to all design nodes that match the prefix `reg` with any number of following characters, such as `reg`, `reg1`, `reg[2]`, `regbank`, and `reg12bank`.

If you apply a constraint to a node specified as `reg?`, the Timing Analyzer searches and applies the constraint to all design nodes that match the prefix `reg` and any single character following; for example, `reg1`, `rega`, and `reg4`.

### 2.7.2.2. Adding and Removing Collection Items

Wildcards that you use with collection commands define collection items that the command identifies. For example, if a design contains registers with the name `src0`, `src1`, `src2`, and `dst0`, the collection command `[get_registers src*]` identifies registers `src0`, `src1`, and `src2`, but not register `dst0`. To identify register `dst0`, you must use an additional command, `[get_registers dst*]`. To include `dst0`, you can also specify a collection command `[get_registers {src* dst*}]`.

To modify collections, use the `add_to_collection` and `remove_from_collection` commands. The `add_to_collection` command allows you to add additional items to an existing collection.

**add_to_collection Command**

```
add_to_collection <first collection> <second collection>
```

*Note:* The `add_to_collection` command creates a new collection that is the union of the two collections you specify.

The `remove_from_collection` command allows you to remove items from an existing collection.

**remove_from_collection Command**

```
remove_from_collection <first collection> <second collection>
```

The following example shows use of `add_to_collection` to add items to a collection.

**Adding Items to a Collection**

```
# Setting up initial collection of registers
set regs1 [get_registers a*]
# Setting up initial collection of keepers
set kprs1 [get_keepers b*]
# Creating a new set of registers of $regs1 and $kprs1
set regs_union [add_to_collection $kprs1 $regs1]
# OR
# Creating a new set of registers of $regs1 and b*
# Note that the new collection appends only registers with name b*
# not all keepers
set regs_union [add_to_collection $regs1 b*]
```

In the Intel Quartus Prime software, keepers are I/O ports or registers. An .sdc file that includes `get_keepers` is incompatible with third-party timing analysis flows.

**Related Information**

- `add_to_collection Command`, Intel Quartus Prime Help
2.7.2.3. Query of Collections

You can display the contents of a collection with the `query_collection` command. Use the `-report_format` option to return the contents in a format of one element per line. The `-list_format` option returns the contents in a Tcl list.

```
query_collection -report_format -all $regs_union
```

Use the `get_collection_size` command to return the number of items the collection contains. If your collection is in a variable with the name `col`, use `set num_items [get_collection_size $col]` rather than `set num_items [llength [query_collection -list_format $col]]` for more efficiency.

2.7.2.4. Using the get_pins Command

The `get_pins` command supports options that control the matching behavior of the wildcard character (*). Depending on the combination of options you use, you can make the wildcard character (*) respect or ignore individual levels of hierarchy. The pipe character (|) indicates levels of hierarchy. By default, the wildcard character (*) matches only a single level of hierarchy.

These examples filter the following node and pin names to illustrate function:

- `lvl` (a hierarchy level with the name `lvl`)
- `lvl|dataa` (an input pin in the instance `lvl`)
- `lvl|datab` (an input pin in the instance `lvl`)
- `lvl|cnod` (a combinational node with the name `cnod` in the `lvl` instance)
- `lvl|cnod|datac` (an input pin to the combinational node with the name `cnod`)
- `lvl|cnod|datad` (an input pin to the combinational node `cnod`)

**Table 34. Sample Search Strings and Search Results**

<table>
<thead>
<tr>
<th>Search String</th>
<th>Search Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>get_pins *</td>
<td>dataa</td>
</tr>
<tr>
<td>get_pins *</td>
<td>datac</td>
</tr>
<tr>
<td>get_pins *</td>
<td>*</td>
</tr>
<tr>
<td>get_pins lvl*</td>
<td>*</td>
</tr>
<tr>
<td>get_pins -hierarchical *</td>
<td>*</td>
</tr>
<tr>
<td>get_pins -hierarchical lvl*</td>
<td>lvl</td>
</tr>
<tr>
<td>get_pins -hierarchical *</td>
<td>datac</td>
</tr>
</tbody>
</table>

(5) The search result is `<empty>` because the wildcard character (*) does not match more than one hierarchy level, that a pipe character (|) indicates, by default. This command matches any pin with the name `datac` in instances at the top level of the design.
The default method separates hierarchy levels of instances from nodes and pins with the pipe character (|). A match occurs when the levels of hierarchy match, and the string values including wildcards match the instance or pin names. For example, the command `get_pins <instance_name>|*|datac` returns all the `datac` pins for registers in a given instance. However, the command `get_pins *|datac` returns an empty collection because the levels of hierarchy do not match.

Use the `--hierarchical` matching scheme to return a collection of cells or pins in all hierarchies of your design.

For example, the command `get_pins --hierarchical *|datac` returns all the `datac` pins for all registers in your design. However, the command `get_pins --hierarchical *|*|datac` returns an empty collection because more than one pipe character (|) is not supported.

The `--compatibility_mode` option returns collections matching wildcard strings through any number of hierarchy levels. For example, an asterisk can match a pipe character when using `--compatibility_mode`.

### 2.8. Timing Analysis of Imported Compilation Results

You can preserve the compilation results for your design as a version-compatible Quartus database file (.qdb) that you can open in a later version of the Intel Quartus Prime software without compatibility issues.

When you import and open the .qdb in a later version of software, you can run timing analysis on the imported compilation results without re-running the Compiler.

**Related Information**

Exporting a Version-Compatible Compilation Database

---

(6) When you use `--compatibility_mode`, the Timing Analyzer does not treat pipe characters (|) as special characters when you use the characters with wildcards.
### 2.9. Using the Intel Quartus Prime Timing Analyzer Document Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2021.04.05       | 21.1                       | • Added:  
|                  |                            |   — "Report Reset Statistics"  
|                  |                            |   — "Report Asynchronous CDC"  
|                  |                            |   — Two new fields to "Report Pipelining Information".  
|                  |                            |   — New screenshots to "Report Logic Depth" and "Report Neighbor Paths"  
|                  |                            |   — get_registers and get_keepers to "Collection Commands".  
|                  |                            |   • Removed -include and -exclude options from "Maximum Skew"  
| 2021.02.22       | 20.3                       | Added extra SDC_ENTITY_FILE info to "Using Entity-bound SDC Files"  
| 2020.09.28       | 20.3                       | • Added "Cross Probing with Design Assistant" section.  
|                  |                            | • Updated "Step 3: Run the Timing Analyzer" for multiple methods.  
|                  |                            | • Updated "Step 1: Specify Timing Analyzer Settings for new tabbed dialog box and options.  
|                  |                            | • Updated "Report Clock Transfers" topic for new data columns.  
|                  |                            | • Updated "Report Timing" topic for Extra Info tab data.  
| 2020.04.13       | 20.1                       | • Added details and Intel Agilex device examples to "Setting the Operating Conditions" topic.  
|                  |                            | • Added "Report Logic Level Depth" topic.  
|                  |                            | • Added "Report Neighbor Paths" topic.  
|                  |                            | • Added "Enabling Time Borrowing Optimization" topic.  
|                  |                            | • Added "Report Time Borrowing Data" topic.  
| 2019.07.15       | 19.2                       | • Updated "Setting Operating Conditions" for SmartVID timing models.  
|                  |                            | • Added step for setting operating conditions to "Step 4: Run Timing Analysis."  
|                  |                            | • Added details about exclusive paths to "Maximum Skew" topic.  
|                  |                            | • Added GUI steps for creating entity-bound SDC files to "Using Entity-bound SDC Files" topic.  
|                  |                            | • Corrected typo in "Maximum Skew" topic.  
|                  |                            | • Updated "Viewing Design Assistant Recommendations" for latest GUI changes.  
| 2018.11.07       | 18.1                       | • Improved description and diagram for "Exclusive Clock Groups" topic.  
| 2018.09.24       | 18.1                       | • Added "Using Entity-bound SDC Files" topic.  
|                  |                            | • Added "Scoping Entity-bound Constraints" topic.  
|                  |                            | • Added "Entity-bound Constraint Examples" topic.  
|                  |                            | • Revised "Basic Timing Analysis Flow" section to add sequential step organization, update steps, and add supporting screenshots.  
|                  |                            | • Added Timing Analyzer screenshot to "Using the Timing Analyzer" topic.  
|                  |                            | • Removed "Creating a Constraint File from Templates with the Text Editor" topic due to limitations of this feature in this version of the software.  
|                  |                            | • Retitled "SDC Constraint Creation Summary" to "Dual Clock SDC Example."  

*continued...*
<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.05.07       | 18.0                       | • Retitled "Default Settings" to "Default Multicycle Analysis."
|                  |                            | • Retitled "SDC (Clock and Exception) Assignments on Blackbox Ports" to "Constraining Design Partition Ports."
|                  |                            | • Added "Viewing Design Assistant Recommendations" topic. |
| 2017.11.27       | 17.1.0                     | • First release as part of the stand-alone Timing Analyzer User Guide |
|                  |                            | • Removed outdated figure: Design Flow with the Timing Analyzer. |
|                  |                            | • Updated Performing an Initial Analysis and Synthesis topic with Intel Quartus Prime Pro Edition commands. |
| 2017.11.06       | 17.1                       | • Updated Using Fitter Overconstraints topic for Intel Stratix 10 support. |
| 2017.05.08       | 17.0                       | • Added Using Fitter Overconstraints topic. |
|                  |                            | • Added Clock Domain Crossing report topics. |
| 2016.10.31       | 16.1                       | • Implemented Intel rebranding. |
|                  |                            | • Added support for -blackbox option with set_input_delay, set_output_delay, remove_input_delay, remove_output_delay. |
| 2016.05.03       | 16.0                       | Added new topic: SCDS (Clock and Exception) Assignments on Blackbox Ports |
| 2015.11.02       | 15.1.0                     | • Changed instances of Quartus II to Quartus Prime. |
|                  |                            | • Added a description of running three- and four-corner analysis with --mode=implement|finalize. |
|                  |                            | • Added description for new set_operating_conditions UI. |
| 2015.05.04       | 15.0.0                     | Added and updated contents in support of new timing algorithms for Arria 10: |
|                  |                            | • Enhanced Timing Analysis for Arria 10 |
|                  |                            | • Maximum Skew (set_max_skew command) |
|                  |                            | • Net Delay (set_net_delay command) |
|                  |                            | • Create Generated Clocks (clock-as-data example) |
| 2014.12.15       | 14.1                       | Major reorganization. Revised and added content to the following topic areas: |
|                  |                            | • Timing Constraints |
|                  |                            | • Create Clocks and Clock Constraints |
|                  |                            | • Creating Generated Clocks |
|                  |                            | • Creating Clock Groups |
|                  |                            | • Clock Uncertainty |
|                  |                            | • Running the Timing Analyzer |
|                  |                            | • Generating Timing Reports |
|                  |                            | • Understanding Results |
|                  |                            | • Constraining and Analyzing with Tcl Commands |
| August 2014      | 14.0a10.0                  | Added command line compilation requirements for Arria 10 devices. |
| June 2014        | 14.0                       | • Minor updates. |
|                  |                            | • Updated format. |
| November 2013    | 13.1                       | • Removed HardCopy device information. |

*continued...*
2. Using the Intel Quartus Prime Timing Analyzer


If the table does not list a software version, the user guide for the previous software version applies.

<table>
<thead>
<tr>
<th>Intel Quartus Prime Version</th>
<th>User Guide</th>
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A. Intel Quartus Prime Pro Edition User Guides

Refer to the following user guides for comprehensive information on all phases of the Intel Quartus Prime Pro Edition FPGA design flow.

Related Information

- **Intel Quartus Prime Pro Edition User Guide: Getting Started**
  Introduces the basic features, files, and design flow of the Intel Quartus Prime Pro Edition software, including managing Intel Quartus Prime Pro Edition projects and IP, initial design planning considerations, and project migration from previous software versions.

  Describes creating and optimizing systems using Platform Designer, a system integration tool that simplifies integrating customized IP cores in your project. Platform Designer automatically generates interconnect logic to connect intellectual property (IP) functions and subsystems.

  Describes best design practices for designing FPGAs with the Intel Quartus Prime Pro Edition software. HDL coding styles and synchronous design practices can significantly impact design performance. Following recommended HDL coding styles ensures that Intel Quartus Prime Pro Edition synthesis optimally implements your design in hardware.

- **Intel Quartus Prime Pro Edition User Guide: Design Compilation**
  Describes set up, running, and optimization for all stages of the Intel Quartus Prime Pro Edition Compiler. The Compiler synthesizes, places, and routes your design before generating a device programming file.

  Describes Intel Quartus Prime Pro Edition settings, tools, and techniques that you can use to achieve the highest design performance in Intel FPGAs. Techniques include optimizing the design netlist, addressing critical chains that limit retiming and timing closure, optimizing device resource usage, device floorplanning, and implementing engineering change orders (ECOs).

  Describes operation of the Intel Quartus Prime Pro Edition Programmer, which allows you to configure Intel FPGA devices, and program CPLD and configuration devices, via connection with an Intel FPGA download cable.

- **Intel Quartus Prime Pro Edition User Guide: Block-Based Design**
  Describes block-based design flows, also known as modular or hierarchical design flows. These advanced flows enable preservation of design blocks (or logic that comprises a hierarchical design instance) within a project, and reuse of design blocks in other projects.
• Intel Quartus Prime Pro Edition User Guide: Partial Reconfiguration
  Describes Partial Reconfiguration, an advanced design flow that allows you to
  reconfigure a portion of the FPGA dynamically, while the remaining FPGA
  design continues to function. Define multiple personas for a particular design
  region, without impacting operation in other areas.

• Intel Quartus Prime Pro Edition User Guide: Third-party Simulation
  Describes RTL- and gate-level design simulation support for third-party
  simulation tools by Aldec*, Cadence*, Mentor Graphics*, and Synopsys that
  allow you to verify design behavior before device programming. Includes
  simulator support, simulation flows, and simulating Intel FPGA IP.

• Intel Quartus Prime Pro Edition User Guide: Third-party Synthesis
  Describes support for optional synthesis of your design in third-party synthesis
  tools by Mentor Graphics*, and Synopsys. Includes design flow steps,
  generated file descriptions, and synthesis guidelines.

• Intel Quartus Prime Pro Edition User Guide: Third-party Logic Equivalence
  Checking Tools
  Describes support for optional logic equivalence checking (LEC) of your design
  in third-party LEC tools by OneSpin*.

• Intel Quartus Prime Pro Edition User Guide: Debug Tools
  Describes a portfolio of Intel Quartus Prime Pro Edition in-system design
  debugging tools for real-time verification of your design. These tools provide
  visibility by routing (or “tapping”) signals in your design to debugging logic.
  These tools include System Console, Signal Tap logic analyzer, system
  debugging toolkits, In-System Memory Content Editor, and In-System Sources
  and Probes Editor.

  Explains basic static timing analysis principals and use of the Intel Quartus
  Prime Pro Edition Timing Analyzer, a powerful ASIC-style timing analysis tool
  that validates the timing performance of all logic in your design using an
  industry-standard constraint, analysis, and reporting methodology.

  Describes the Intel Quartus Prime Pro Edition Power Analysis tools that allow
  accurate estimation of device power consumption. Estimate the power
  consumption of a device to develop power budgets and design power supplies,
  voltage regulators, heat sink, and cooling systems.

• Intel Quartus Prime Pro Edition User Guide: Design Constraints
  Describes timing and logic constraints that influence how the Compiler
  implements your design, such as pin assignments, device options, logic
  options, and timing constraints. Use the Interface Planner to prototype
  interface implementations, plan clocks, and quickly define a legal device
  floorplan. Use the Pin Planner to visualize, modify, and validate all I/O
  assignments in a graphical representation of the target device.

  Describes support for optional third-party PCB design tools by Mentor
  Graphics* and Cadence*. Also includes information about signal integrity
  analysis and simulations with HSPICE and IBIS Models.

• Intel Quartus Prime Pro Edition User Guide: Scripting
  Describes use of Tcl and command line scripts to control the Intel Quartus
  Prime Pro Edition software and to perform a wide range of functions, such as
  managing projects, specifying constraints, running compilation or timing
  analysis, or generating reports.