Intel® Quartus® Prime Pro Edition User Guide

Platform Designer

Updated for Intel® Quartus® Prime Design Suite: 20.3
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1. Creating a System with Platform Designer

The Intel® Quartus® Prime software includes the Platform Designer system integration tool. Platform Designer simplifies the task of defining and integrating custom IP components (IP cores) into your FPGA design.

Platform Designer automatically creates interconnect logic from high-level connectivity that you specify. The interconnect automation eliminates the time-consuming task of specifying system-level HDL connections.

Figure 1. Platform Designer GUI

Platform Designer allows you to specify interface requirements and integrate IP components within a graphical representation of the system. The Intel Quartus Prime software installation includes the Intel FPGA IP library available from the IP Catalog in Platform Designer.
You can integrate optimized and verified Intel FPGA IP cores into a design to shorten design cycles and maximize performance. Platform Designer also supports integration of IP cores from third-parties, or custom components that you define.

Platform Designer supports a hierarchical framework that offers fast response times for interconnecting large systems and blackbox entities. Platform Designer supports a variety of design entry methods, such as register transfer level (RTL) and schematic entry. Platform Designer supports the creation of your own custom components, as well as generic components that define only the interface and signal connections to the rest of the system.

Platform Designer provides support for the following:

- Create and reuse components—define and reuse custom parameterizable components in a Hardware Component Definition File (\_hw.tcl) that describes and packages IP components.
- Define generic IP components—instantiate generic IP components without an HDL implementation.
- Incremental generation—optimize and generate IP components incrementally.
- Avalon® AXI interconnect—Platform Designer generates appropriate types of interconnect logic to handle protocol differences.
- Hierarchical system support—generates a separate .ip file that isolates the system from the IP component parameterization. Change parameters of a single IP component without regeneration of other IP components.
- Command-line support—optionally use command-line utilities and scripts to perform functions available in the Platform Designer GUI.
- Up to 64-bit addressing.
- Optimization of interconnect and pipelining within the system and auto-adaptation of data widths and burst characteristics.
- Inter-operation between standard protocols.

**Related Information**

- Platform Designer Command-Line Utilities on page 375
- Introduction to Intel FPGA IP Cores
- Platform Designer System Design Flow on page 13

**1.1. Platform Designer Interface Support**

Platform Designer is most effective when you use standard interfaces available in the IP Catalog to design custom IP. Standard interfaces operate efficiently with Intel FPGA IP components, and you can take advantage of the bus functional models (BFMs), monitors, and other verification IP that the IP Catalog provides.

Platform Designer also supports connections between Avalon and AXI interfaces by generating the interconnect logic. This logic enables you to handle the protocol difference. Platform Designer creates the interconnect logic by converting all the protocols to a proprietary packet format. Then, the tool routes the packet through network switches to the appropriate slaves. Here, the packet converts to the slave's protocol.
Platform Designer supports the following interface specifications:

- Intel FPGA Avalon Memory-Mapped and Streaming
- Arm* AMBA* 3 AXI (version 1.0)
- Arm AMBA 4 AXI (version 2.0)
- Arm AMBA 4 AXI-Lite (version 2.0)
- Arm AMBA 4 AXI-Stream (version 1.0)
- Arm AMBA 3 APB (version 1.0)

IP components (IP Cores) can have any number of interfaces in any combination. Each interface represents a set of signals that you can connect within a Platform Designer system, or export outside of a Platform Designer system.

Platform Designer IP components can include the following interface types:

Table 1.  **IP Component Interface Types**

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<th>Interface Type</th>
<th>Description</th>
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<tr>
<td>Memory-Mapped</td>
<td>Connects memory-referencing master devices with slave memory devices. Master devices can be processors and DMAs, while slave memory devices can be RAMs, ROMs, and control registers. Data transfers between Avalon Memory Mapped master and slave may be unidirectional (read only or write only), or bi-directional (read and write).</td>
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<td>Streaming</td>
<td>Connects Avalon Streaming sources and sinks that stream unidirectional data, as well as high-bandwidth, low-latency IP components. Streaming creates datapaths for unidirectional traffic, including multichannel streams, packets, and DSP data. The Avalon interconnect is flexible and can implement on-chip interfaces for industry standard telecommunications and data communications cores, such as Ethernet, Interlaken, and video. You can define bus widths, packets, and error conditions.</td>
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<tr>
<td>Interrupts</td>
<td>Connects interrupt senders to interrupt receivers. Platform Designer supports individual, single-bit interrupt requests (IRQs). In the event that multiple senders assert their IRQs simultaneously, the receiver logic (typically under software control) determines which IRQ has highest priority, then responds appropriately.</td>
</tr>
<tr>
<td>Clocks</td>
<td>Connects clock output interfaces with clock input interfaces. Clock outputs can fan-out without the use of a bridge. A bridge is required only when a clock from an external (exported) source connects internally to more than one source.</td>
</tr>
<tr>
<td>Resets</td>
<td>Connects reset sources with reset input interfaces. If your system requires a particular positive-edge or negative-edge synchronized reset, Platform Designer inserts a reset controller to create the appropriate reset signal. If you design a system with multiple reset inputs, the reset controller ORs all reset inputs and generates a single reset output.</td>
</tr>
<tr>
<td>Conduits</td>
<td>Connects point-to-point conduit interfaces, or represent signals that you export from the Platform Designer system. Platform Designer uses conduits for component I/O signals that are not part of any supported standard interface. You can connect two conduits directly within a Platform Designer system as a point-to-point connection. Alternatively, you can export conduit interfaces and bring the interfaces to the top-level of the system as top-level system I/O. You can use conduits to connect to external devices, for example external DDR SDRAM memory, and to FPGA logic defined outside of the Platform Designer system.</td>
</tr>
</tbody>
</table>

**Related Information**

- Avalon Interface Specifications
- AMBA Protocol Specifications
1.2. Platform Designer System Design Flow

You can use the Platform Designer GUI to quickly create and customize a Platform Designer system for integration with an Intel Quartus Prime project. Alternatively, you can perform many of the functions available in the Platform Designer GUI at the command-line, as Platform Designer Command-Line Utilities on page 375 describes.

When you create a system in the GUI, Platform Designer creates a .qsys file that represents the system in your Intel Quartus Prime software project.

Figure 2. Platform Designer System Design Flow

The circled numbers in the diagram correspond with the following topics in this chapter:
1. Creating or Opening a Platform Designer System on page 14
2. Adding IP Components to a System on page 29
3. Connecting System Components on page 39
1.3. Creating or Opening a Platform Designer System

You can launch Platform Designer from the Intel Quartus Prime software to create or open a Platform Designer system.

When you create or open a system, Platform Designer requires that you specify the Intel Quartus Prime project to contain this system. If this project does not yet exist, you can define a new project from within Platform Designer. Alternatively, you can specify an existing project. When you launch Platform Designer with an Intel Quartus Prime project open, Platform Designer automatically specifies that project by default.

After specifying the project, you select an existing system to open, or specify the name of a new system to create.

Follow these steps to create or open a Platform Designer system:

1. In the Intel Quartus Prime software, click File ➤ Open Project to open the Intel Quartus Prime project that you want to include the Platform Designer system. You can optionally skip this step and launch Platform Designer in view-only mode without opening a project.(1)

2. Click Tools ➤ Platform Designer. Platform Designer launches and displays the Open Project dialog box automatically.

3. Specify the Quartus project. If you have a project open, this project name appears automatically. Otherwise, browse for an existing project, or click the Create New Quartus Project button and specify a new project name. Selecting None for Quartus project opens Platform Designer in view-only mode.
4. Specify any of the following options:
   - **Revision**—optionally select a specific revision of your project, or click the Create New Revision button and define a new project revision.
   - **Device family**—when defining a new project, allows you to specify the target Intel FPGA device family. Otherwise this field is non-editable and displays the Quartus project target device family. Click Retrieve Values to populate the fields.
   - **Device part**—when defining a new project, allows you to specify the target Intel FPGA device part number. Otherwise this field is non-editable and displays the Quartus project target device part number.

5. Select the Platform Designer system, or click the Create New Platform Designer System button and specify the name of a new system.

6. Change the project associated with a Platform Designer system at any time by clicking File ➤ Select Quartus Project in Platform Designer.

### 1.3.1. Specifying the Target Intel FPGA Device for a System

You can specify the target device when you create a new project or system. The generation output is specific to the target Intel FPGA **Device family** that you specify. The available IP components, parameters, and output options for your system vary according to the **Device family** that you specify.

---

(1) View-only mode does not allow creating new systems or IP, adding or removing IP, or executing system scripts.
You can modify the target **Device family** setting for your system at any time on the Platform Designer **Device Family** tab. If you specify a target **Device family** that is different from the project target device family, Platform Designer updates the target device family for the project to match the **Device family** specification.

Platform Designer prompts you to upgrade any IP components that are incompatible with the **Device family** that you specify.

**Related Information**
Upgrading Outdated IP Components in Platform Designer on page 59

### 1.3.2. Specifying Additional Application Memory

If your Platform Designer system requires more than the default memory to run efficiently, you can increase the amount of application memory allocated to run Platform Designer.

- If you are using Platform Designer from within the Intel Quartus Prime software, increase memory for your Platform Designer system, by clicking **Tools ➤ Options ➤ IP Settings**, and then specifying the amount of memory with the **Maximum Platform Designer memory usage** option.

- If you are using Platform Designer from the command-line, you can add an option to increase the memory. For example, the following `qsys-edit` command allows you to open Platform Designer with 2 gigabytes of memory.

```
qsys-edit --jvm-max-heap-size=2g
```
1.3.3. Synchronizing IP File References

When you open a system containing IP components, Platform Designer confirms that the list of IP files in your Platform Designer system matches the list of IP files included in the corresponding Intel Quartus Prime project.

The **IP Synchronization Result** dialog box automatically displays any discrepancies between these IP file references in the system.

To manually start a check for IP reference mismatches between the system and corresponding Intel Quartus Prime project:

1. In Platform Designer, click **File ➤ Synchronize IP File References**.
2. View the results of the synchronization. Platform Designer identifies the following types of mismatches with the IP synchronization:

<table>
<thead>
<tr>
<th>Mismatch Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Duplicate IP files</strong></td>
<td>The IP files references in the Platform Designer system and the associated Intel Quartus Prime project match. These IP files contain the same name, but are present in different locations. In such cases, the IP files referenced in the Intel Quartus Prime project takes precedence. Platform Designer replaces the IP file reference in the system with the one in the Intel Quartus Prime project during compilation. <strong>Note:</strong> If the Intel Quartus Prime project contains more than one IP of the same file name, Platform Designer retains the first instance and removes all other occurrences of the IP file with the specific name.</td>
</tr>
<tr>
<td><strong>Missing IP files</strong></td>
<td>Lists the IP file references missing from Platform Designer system and the corresponding Intel Quartus Prime project. In such cases, Platform Designer allows you to specify the active IP file.</td>
</tr>
<tr>
<td><strong>Missing Platform Designer IP files</strong></td>
<td>Lists the IP file references missing from your Platform Designer system that the Intel Quartus Prime project references. If Platform Designer locates a valid reference in the Intel Quartus Prime project, it replaces the missing reference in the Platform Designer system with IP file reference from the Intel Quartus Prime project.</td>
</tr>
<tr>
<td><strong>Missing Quartus IP files</strong></td>
<td>Lists the IP file references missing from your Intel Quartus Prime project that the Platform Designer system references. Platform Designer adds the missing IP file reference to the Intel Quartus Prime project. If the project’s .qsf file already contains reference to the missing IP file, but the file cannot be located in the specified path, Platform Designer removes the reference in the .qsf file, and adds the reference to the IP file in the Platform Designer system.</td>
</tr>
</tbody>
</table>

1.3.4. Converting Incompatible Components

If you open a Platform Designer system with incompatible components, Platform Designer prompts you to convert these components to the current Platform Designer format. On conversion, the **Platform Designer Conversion Results** dialog box appears, listing all the converted system and IP source files.

Platform Designer stores the converted .ip files inside an **ip** folder, relative to the Platform Designer system file (.qsys) location. Platform Designer prefixes the system name to the .ip file name. Platform Designer automatically adds these converted files to the associated Intel Quartus Prime project. Ensure that you maintain these .ip files, along with your system files.
1.4. Viewing a Platform Designer System

Platform Designer allows you to visualize all aspects of your system. By default, Platform Designer displays the contents of your system in the System View whenever you open a system. You can also access other panels that allow you to view and modify various elements of the system.

When you select or edit an item in one Platform Designer tab, all other tabs update to reflect your selection or edit. For example, if you select the `cpu_0` in the Hierarchy tab, the Parameters tab immediately updates to display `cpu_0` parameters.

Figure 6. Platform Designer GUI

Click the View menu to interact with the elements of your system in various tabs.

- The **System View**, Address Map, Interconnect Requirements, and Details tabs display in the main frame.
- By default, the **IP Catalog**, Hierarchy, and the Device Family tabs appear to the left of the main frame.
- **Parameters**, System Info, and Component Instantiation tabs appear to the right of the main frame.
- The **System Messages** and Generation Messages tabs display in the lower portion of Platform Designer.
The Platform Designer GUI is fully customizable. You can arrange and display Platform Designer GUI elements that you most commonly use, and then save and reuse useful GUI layouts.

### 1.4.1. Viewing the System Hierarchy

The **Hierarchy** tab hierarchically displays the modules, connections, and exported signals in the current system. You can expand and traverse through the system hierarchy, zoom in for detail, and locate to elements in other Platform Designer panes.

The **Hierarchy** tab provides the following information and functionality:

- Lists connections between components.
- Lists names of signals in exported interfaces.
- Right-click to connect, edit, add, remove, or duplicate elements in the hierarchy.
- Displays internal connections of Platform Designer subsystems that you include as IP components. By contrast, the **System View** tab displays only the exported interfaces of Platform Designer subsystems.

#### Expanding the System Hierarchy

Click the + icon to expand any interface in the **Hierarchy** tab to view sub-components, associated elements, and signals for the interface. The **Hierarchy** tab displays a unique icon for each element type in the system. In the example below, the `ram_master` selection appears selected in both the **System View** and **Hierarchy** tabs.

**Figure 7. Expanding System View in the Hierarchy Tab**

![Expanding System View in the Hierarchy Tab](image)
1.4.2. Filtering the System View

You can easily filter the display of your system in the System View by component, interface type, instance name, or other properties. Filtering the view allows you to simplify the display and focus only on the items you want.

For example, you can click any of the following basic filter controls at the top of the System View to display or hide various elements in the system:

**Figure 8. System View Filter Controls**

<table>
<thead>
<tr>
<th>System View Filter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Show exported connections</td>
<td>Shows or hides the exported connections of the exported interface in the System View.</td>
</tr>
<tr>
<td>Show submodule connections</td>
<td>Shows or hides the submodules that have connections in the System View.</td>
</tr>
<tr>
<td>Show connected modules</td>
<td>Shows or hides the modules that have connections in the System View.</td>
</tr>
<tr>
<td>Hide unconnectable interfaces</td>
<td>Shows or hides the modules that are not available for connection in the System View.</td>
</tr>
<tr>
<td>Remove Dangling Exports</td>
<td>Removes unconnected exported connections from the System View.</td>
</tr>
</tbody>
</table>

In addition, you can click the Filter button to display only instances that include memory-mapped interfaces, or display only instances that connect to a particular Nios® II processor. Conversely, you can temporarily hide clock and reset interfaces to further simplify the display.
Figure 9. **Filter Icon and Filters Dialog Box**

Select one or more components on the **Filter** tab (View ➤ Filter) to display only the selected component in the **System View** tab.

Figure 10. **Filter Tab**

Related Information
Filters Dialog Box
1.4.3. Viewing System Connections

The **Connections** tab allows you to connect or un-connect every connection in the Platform Designer system.

Click **View ▶ Connections** to display this tab.

If you connect or unconnect modules on the **Connections** tab, the connection immediately updates in the **System View** tab. You can also make connections in the **System View** tab directly.

**Figure 11. Connections tabs in Platform Designer**

1.4.4. Viewing Clock and Reset Domains

The Platform Designer **Clock Domains** and **Reset Domains** tabs list the clock and reset domains in the Platform Designer system, respectively.

Click **View ▶ Clock Domains** or click **View ▶ Reset Domains** to display these tabs.

Platform Designer determines clock and reset domains by the associated clocks and resets. This information displays when you hover over interfaces in your system.
Clock Domains, Reset Domains, and System View Tabs

The Clock Domains and Reset Domains tabs also allow you to locate system performance bottlenecks. The tabs indicate connection points where Platform Designer automatically inserts clock-crossing adapters and reset synchronizers during system generation. View the following information on these tabs to create optimal connections between interfaces:

- The number of clock and reset domains in the system
- The interfaces and modules that each clock or reset domain contains
- The locations of clock or reset crossings
- The connection point of automatically inserted clock or reset adapters
- The proper location for manual insertion of a clock or reset adapter

1.4.4.1. Viewing Clock Domains in a System

On the Clock Domains tab, you can filter the System View tab to display a single clock domain, or multiple clock domains. You can further filter your view with the Filter control. When you select an element in the Clock Domains tab, the corresponding selection appears highlighted in the System View tab.

Follow these steps to filter and highlight clock domains in the System View:

1. Click View ➤ Clock Domains.
2. Select any clock or reset domain in the list to view associated interfaces. The corresponding selection appears in the System View tab.
3. To highlight clock domains in the System View tab, click Show clock domains in the system table or at the bottom of the System View tab.
4. To view a single clock domain, or multiple clock domains and their modules and connections, select the clock name or names in the Clock Domains tab. The modules for the selected clock domain or domains and connections highlight in the System View tab. Detailed information for the current selection appears in the clock domain details pane.

5. To view interfaces that cross clock domains, expand the Clock Domain Crossings icon in the Clock Domains tab, and select each element to view its details in the System View tab. Platform Designer lists the interfaces that cross clock domains under Clock Domain Crossings. As you click through the elements, detailed information appears in the clock domain details pane. Platform Designer also highlights the selection in the System View tab.

1.4.4.2. Viewing Reset Domains in a System

On the Reset Domains tab, you can filter the System View tab to display a single reset domain, or multiple reset domains. When you select an element in the Reset Domains tab, the corresponding selection appears in the System View tab.

Follow these steps to filter and highlight reset domains in the System View:

Note: If a connection crosses a clock domain, the connection circle appears as a red dot in the System View tab.
1. To open the Reset Domains tab, click View ➤ Reset Domains.
2. To show reset domains in the System View tab, click the Show reset domains in the system table icon in the System View tab.

**Figure 15. Show Reset Domains in the System Table**

3. To view a single reset domain, or multiple reset domains and their modules and connections, click the reset names in the Reset Domain tab.

**Figure 16. Selected Reset Signal in Reset Domains and System View Tabs**

Platform Designer displays your selection according to the following rules:

- When you select multiple reset domains, the System View tab shows interfaces and modules in both reset domains.
- When you select a single reset domain, the other reset domains are grayed out, unless the two domains have interfaces in common.
- Reset interfaces appear black when connected to multiple reset domains.
- Reset interfaces appear gray when they are not connected to all of the selected reset domains.
- If an interface is contained in multiple reset domains, the interface is grayed out.

Detailed information for your selection appears in the reset domain details pane.
Note: Red dots in the Connections column between reset sinks and sources indicate auto insertions by Platform Designer during system generation, for example, a reset synchronizer. Platform Designer decides when to display a red dot with the following protocol, and ends the decision process at first match.

- Multiple resets fan into a common sink.
- Reset inputs are associated with different clock domains.
- Reset inputs have different synchronicity.

1.4.5. Viewing Avalon Memory-Mapped Domains in a System

The Domains tab displays a list of all the Avalon memory mapped domains in the system, allowing you to specify interconnect parameters. When you select a domain in the Domains tab, the corresponding selection highlights in the System View tab.

Click View ➤ Domains to display this tab.

Figure 17. Domains Tab
• Filter the **System View** tab to display a single Avalon domain, or multiple domains. Further filter your view with selections in the **Filters** dialog box.

• To rename an Avalon memory-mapped domain, double-click the domain name. Detailed information for the current selection appears in the Avalon domain details pane.

• On the **Domain** tab, specify interconnect parameters, as [Specifying Interconnect Parameters on page 50](#).

• To enable and disable the highlighting of the Avalon domains in the **System View** tab, click the domain control tool at the bottom of the **System View** tab.

### 1.4.6. Viewing the System Schematic

The **Schematic** tab displays a schematic representation of the current Platform Designer system. You can zoom into a component or connection to view more details. You can use the image handles in the right panel to resize the schematic image.

Click View ➤ Schematic to display this tab.

If your selection is a subsystem, you can use the **Move to the top of the hierarchy**, **Move up one level of hierarchy**, and **Drill into a subsystem to explore its contents** buttons to traverse the schematic of a hierarchical system.

---

**Figure 18. Schematic Tab**

[Diagram of schematic]

**Related Information**

- [Editing a Subsystem](#) on page 82

### 1.4.7. Customizing the Platform Designer Layout
You can arrange your workspace by dragging and dropping, and then grouping tabs in an order appropriate to your design development, or close or dock tabs that you are not using.

Dock tabs in the main frame as a group, or individually by clicking the tab control in the upper-right corner of the main frame. Tool tips on the upper-right corner of the tab describe possible workspace arrangements, for example, restoring or disconnecting a tab to or from your workspace.

When you save your system, Platform Designer also saves the current workspace configuration. When you re-open a saved system, Platform Designer restores the last saved workspace.

The **Reset to System Layout** command on the View menu restores the workspace to its default configuration for Platform Designer system design. The **Reset to IP Layout** command restores the workspace to its default configuration for defining and generating single IP cores.

Follow these steps to customize and save the Platform Designer layout:

1. Click items on the View menu to display and then optionally dock the tabs. Rearrange the tabs to suit your preferences.

2. To save the current Platform Designer window configuration as a custom layout, click **View ➤ Custom Layouts ➤ Save**. Platform Designer saves your custom layout in your project directory, and adds the layout to the custom layouts list, and the `layouts.ini` file. The `layouts.ini` file determines the order of layouts in the list.

3. Use any of the following methods to revert to another layout:
   - To revert the layout to the default system design layout, click **View ➤ Reset to System Layout**. This layout displays the System View, Address Map, Interconnect Requirements, and Messages tabs in the main pane, and the IP Catalog and Hierarchy tabs along the left pane.
   - To revert the layout to the default system design layout, click **View ➤ Reset to IP Layout**. This layout displays the Parameters and Messages tabs in the main pane, and the Details, Block Symbol, and Presets tabs along the right pane.
   - To reset your Platform Designer window configuration to a previously saved layout, click **View ➤ Custom Layouts**, and then select the custom layout.
   - Press Ctrl+3 to quickly change the Platform Designer layout.

4. To manage your saved custom layouts, click **View ➤ Custom Layouts**. The **Manage Custom Layouts** dialog box opens and allows you to apply a variety of functions that facilitate custom layout management. For example, you can import or export a layout from or to a different directory.
1.5. Adding IP Components to a System

You can quickly add Intel FPGA IP components to a system from the IP Catalog in Platform Designer. The IP Catalog launches a parameter editor that allows you to specify options and add the component to your system. Your Platform Designer system can contain a single instance of an IP component, or multiple, individually parameterized variations of multiple or the same IP components.

When you first add an Intel FPGA IP components to a system from the IP Catalog, Platform Designer automatically adds the IP as a generic component for all IP except the Intel FPGA HPS IP components. Generic components allow you to define only the interface and signal connections to the rest of the system, without immediately defining the HDL implementation.

Follow these steps to locate, parameterize, and instantiate an IP component in a Platform Designer system:

1. To locate a component by name, type some or all of the component’s name in the IP Catalog search box. For example, type memory to locate memory-mapped IP components. You can also find components by category.

2. Double-click any component to launch the component's parameter editor and specify options for the component. The Parameterization Messages tab displays any parameterization errors.

For some IP components, you can select and Apply a pre-defined set of parameters values for specific applications from the Presets list.
3. After you specify all parameters, click **Finish** to instantiate the component in the system. The IP component appears in the **System View** and **Component Instantiation** tabs. Platform Designer creates a corresponding .ip file for the IP component on instantiation, and stores the file in the <ip> folder in the project directory.

Platform Designer instantiates a generic component in place of the actual IP core with a reference to the HDL entity name, module and interface assignments, compilation library, HDL ports, interfaces, and system-info parameters.

### 1.5.1. Modifying IP Parameters

The **Parameters** tab allows you to view and edit the current parameter settings for IP components in your system.

To display a components parameters on the **Parameters** tab:

1. click **View ➤ Parameters**.
2. Select the component in the **System View** or **Hierarchy** tabs.
The **Parameters** tab provides the following functionality:

- **Parameters** field—adjust the parameters to align with your design requirements, including changing the name of the top-level instance.
- Component Banner—displays the hierarchical path for the component and allows you to enable display of internal names. Below the hierarchical path, the parameter editor shows the HDL entity name and the IP file path for the selected IP component. Right-click in the banner to display internal parameter names for use with scripted flows.
- **Details**—displays links to detailed information about the component.
- **Parameterization Messages**—displays parameter warning and error messages about the IP component.

**Figure 22. Platform Designer Parameters Tab**

Changes that you make in the **Parameters** tab affect your entire system, and dynamically update other open tabs in Platform Designer. Any change that you make on the **Parameters** tab, automatically updates the corresponding .ip file that stores the component's parameterization.

If you create your own custom IP components, you can use the Hardware Component Description File (\_hw.tcl) to specify configurable parameters.

**Note:** If you use the ip-deploy or qsys-script commands rather than the Platform Designer GUI, you must use internal parameter names with these parameters.
1.5.1.1. Viewing Component or Parameter Details

The Details tab provides information for a component or parameter that you select. Platform Designer updates the information in the Details tab as you select different components.

To view a component's details:
1. Click the parameters for a component in the parameter editor, Platform Designer displays the description of the parameter in the Details tab.
2. To return to the complete description for the component, click the header in the Parameters tab.

1.5.1.2. Viewing a Component's Block Symbol

The Block Symbol tab displays a symbolic representation of any component you select in the Hierarchy or System View tabs. The block symbol shows the component's port interfaces and signals. The Show signals option allows you to turn on or off signal graphics.

Figure 23. Block Symbol Tab

The Block Symbol tab appears by default in the parameter editor when you add a component to your system. When the Block Symbol tab is open in your workspace, it reflects changes that you make in other tabs.

1.5.2. Applying Preset Parameters for Specific Applications

The Preset tab displays the names of any available preset settings for an IP component. The preset preserves a collection of parameter setting that may be appropriate for a specific protocol or application. Not all IP components include preset parameters. Double-click the preset parameter name to apply the preset parameter values to a component you are defining.
1. Creating a System with Platform Designer

1.5.2.1. Creating IP Custom Preset Parameters Settings

You can optionally define and save a custom set of parameter settings for an IP component, and then apply the preset settings whenever you add an instance of the IP component to any system.

Follow these steps to save custom preset parameter settings:

1. In IP Catalog, double-click any component to launch the parameter editor.
2. To search for a specific preset for the initial settings, type a partial preset name in the search box.
3. In the Presets tab, click New to specify the Preset name and Preset description.
4. Under Select parameters to include in the preset, enable or disable the parameters you want to include in the preset.
5. Specify the path for the Preset file that preserves the collection of parameter settings.
If the file location that you specify is not already in the IP search path, Platform Designer adds the location of the new preset file to the IP search path.

6. Click **Save**.

7. To apply the preset to an IP component, click **Apply**. Preset parameter values that match the current parameter settings appear in bold.

### 1.5.3. Adding Third-Party IP Components

You can add third-party IP components created by Intel partners to your Platform Designer system. Third-party partner IP components have interfaces that Platform Designer supports, such as Avalon memory mapped or AMBA AXI. Third-party partner IP components can also include timing and placement constraints, software drivers, simulation models, and reference designs.

To locate supported third-party IP components on the Intel web page, follow these steps:

1. From the Intel website, navigate to the **Find IP** page, and then click Find IP on the tool.
2. Use the **Search** box and the **End Market, Technology, Devices** or **Provider** filters to locate the IP that you want to use.
3. Click **Enter**.
4. Sort the table of results for the **Platform Designer Compliant** column. You cannot use non-compliant components in Platform Designer.
5. Click the IP name to view information, request evaluation, or request download.
6. After you download the IP files, add the IP location to the IP search path to add the IP to IP Catalog, as **IP Search Path Recursive Search** on page 35 describes.

**Related Information**

Find Intel FPGA and Partner IP
1.5.3.1. IP Search Path Recursive Search

The Intel Quartus Prime software automatically searches and identifies IP components in the IP search path. The search is recursive for some directories, and only to a specific depth for others. During a recursive descent search, whenever search finds a _hw.tcl or .ipx file, search does not descend further.

In the following list of search locations, ** indicates a recursive descent.

### Table 4. IP Search Locations

<table>
<thead>
<tr>
<th>Location</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROJECT_DIR/*</td>
<td>Finds IP components and index files in the Intel Quartus Prime project directory.</td>
</tr>
<tr>
<td>PROJECT_DIR/ip/**/*</td>
<td>Finds IP components and index files in any subdirectory of the /ip subdirectory of the Intel Quartus Prime project directory.</td>
</tr>
</tbody>
</table>

1.5.3.1.1. IP Search Path Precedence

If the Intel Quartus Prime software recognizes two IP cores with the same name, the following search path precedence rules determine the resolution of files:

1. Project directory.
2. Project database directory.
3. Project IP search path specified in IP Search Locations, or with the SEARCH_PATH assignment for the current project revision.
4. Global IP search path specified in IP Search Locations, or with the SEARCH_PATH assignment in the quartus2.ini file.
5. Quartus software libraries directory, such as <Quartus Installation> \libraries.

1.5.3.1.2. IP Component Description Files

The Intel Quartus Prime software identifies parameterizable IP components in the IP search path for the following files:

- Component Description File (_hw.tcl)—defines a single IP core.
- IP Index File (.ipx)—each .ipx file indexes a collection of available IP cores. This file specifies the relative path of directories to search for IP cores. In general, .ipx files facilitate faster searches.

1.5.3.2. Defining the IP Search Path with Index Files

You can create an IP Index File (.ipx) to specify a path that Platform Designer searches for IP components.

You can optionally specify the search path in a user_components.ipx file, in addition to Tools ➤ Options ➤ IP Catalog Search Locations. The user_components.ipx file allows you to add locations independent of the default search path.
A `<path>` element in a `.ipx` file specifies a directory where Platform Designer can search for IP components. A `<component>` entry specifies the path to a single component. `<path>` elements allow wildcards in definitions. An asterisk matches any file name. If you use an asterisk as a directory name, it matches any number of subdirectories.

### Example 1. Path Element in an `.ipx` File

```
<library>
  <path path="...<user directory>" />
  <path path="...<user directory>" />
  ...
  <component ...
```

A `<component>` element in an `.ipx` file contains several attributes to define a component. If you provide the required details for each component in an `.ipx` file, the startup time for Platform Designer is less than if Platform Designer must discover the files in a directory.

### Example 2. Component Element in an `.ipx` File

The example shows two `<component>` elements. Note that the paths for file names are specified relative to the `.ipx` file.

```
<library>
  <component
```
2. For **Implementation Type**, select the IP (Default), HDL, Blackbox, or HLS type. Component Implementation Type Options on page 37 defines these types.

3. Under **Compilation Info**, specify the **HDL Entity name** and **HDL compilation library** name for the implementation. These values are fixed for the **IP Implementation Type**.

4. In the **Signals & Interfaces** tab, define the port boundary of the component. Click `<add interface>` or `<add signal>` to add the interfaces and signals.

5. Optionally, click the **Block symbol** tab to visualize the signals and interfaces added in the **Signals & Interfaces** tab.

6. Optionally, in the **Export** tab you can export the signals and interfaces of an IP component as an IP-XACT file or a `_hw.tcl` file.

    **Note:** Platform Designer supports importing and exporting files in IP-XACT 2009 format and exporting IP-XACT files in 2014 format.

**Related Information**
- Component Implementation Type Options on page 37
- Adding Generic Components to a System on page 118

### 1.5.4.1. Component Implementation Type Options

**Table 5. Component Implementation Type Options**

<table>
<thead>
<tr>
<th>Implementation Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>IP</td>
<td>The default implementation type for any new component. The Implementation Type directs. Platform Designer reads the IP Implementation Type to perform the following functions:</td>
</tr>
</tbody>
</table>

*continued...*
### Implementation Type

<table>
<thead>
<tr>
<th>Implementation Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| • Runs background checks against the port widths between the IP component and the .ip file to ensure continuity.  
• Scans the .ip file for the error flag to determine if any component has parameterization errors.  
• Checks for system-info mismatches between the IP file and the IP component in the system, and prompts resolution with IP instantiation warnings in the **Instantiation Messages** tab. |
| HDL | Allows you to define a component in your system from existing RTL. You can populate the signals and interfaces parameters of the generic component from an RTL file. |
| Blackbox | Defines a component that represents only the signal and interface boundary of an entity, without providing the component’s implementation. You then provide the implementation of the component for processing with the Intel Quartus Prime software or an RTL simulator. |
| HLS | Allows you to adds an existing high level synthesis (HLS) file as a component, compile an HLS file, import a previously compiled HLS file, perform verification on an HLS project, or display the resulting compilation report. |

### 1.5.5. Creating or Opening an IP Core Variant

In addition to creating a system, Platform Designer allows you to define a stand-alone IP core variant that you can add to your Intel Quartus Prime project or to a Platform Designer system.

Follow these steps to define an IP core variant in Platform Designer:
1. In Platform Designer, click **File ➤ New IP Variant**.
2. On the **IP Variant** tab, specify the **Quartus project** to contain the IP variant.

![Figure 27. Platform Designer IP Variant Tab](image)

3. Specify any of the following options:
• **Revision**—optionally select a specific revision of a project.
• **Device family**—when defining a new project or None, allows you to specify the target Intel FPGA device family. Otherwise this field is non-editable and displays the Quartus project target device family. Click **Retrieve Values** to populate the fields.
• **Device part**—when defining a new project or None, allows you to specify the target Intel FPGA device part number. Otherwise this field is non-editable and displays the Quartus project target device part number.

4. Specify the **IP variant** name, or browse for an existing IP variant.
5. For **Component type**, click **Select** and select the IP component from the IP Catalog.
6. Click **Create**. The IP parameter editor appears. Specify the parameter values that you want for the IP variant.
7. To generate the IP variant synthesis and optional simulation files, click **Generate HDL**, specify **Generation Options**, and click **Generate**. Refer to **Generation Dialog Box Options** on page 64 for generation options.

1.6. **Connecting System Components**

You must appropriately connect the components in your Platform Designer system. The **System View** and **Connections** tabs allow you to connect and configure IP components quickly. Platform Designer supports connections between interfaces of compatible types and opposite directions.

For example, you can connect a memory-mapped master interface to a slave interface, and an interrupt sender interface to an interrupt receiver interface. You can connect any interfaces exported from a Platform Designer system within a parent system.

Platform Designer uses the high-level connectivity you specify to instantiate a suitable HDL fabric to perform the needed adaptation and arbitration between components. Platform Designer generates and includes this interconnect fabric in the RTL system output.
Figure 28. Connections Column in the System Contents Tab

Potential connections between interfaces appear as gray interconnect lines with an open circle icon at the intersection of the potential connection.

Figure 29. Potential and Implemented Connections in System View
To implement a connection, follow these steps:

1. Click inside an open connection circle to implement the connection between the interfaces. When you make a connection, Platform Designer changes the connection line to black, and fills the connection circle. Clicking a filled-in circle removes the connection.

2. To display the list of current and possible connections for interfaces in the Hierarchy or System View tabs, click View ➤ Connections.

Figure 30. Connection Display for Exported Interfaces

3. Perform any of the following to modify connections:
   - On the Connections tab, enable or disable the Connected column to enable or disable any connection. The Clock Crossing, Data Width, and Burst columns provide interconnect information about added adapters that can result in slower fMAX or increased area utilization.
   - On the System View tab, right-click in the Connection column and disable or enable Allow Connection Editing.
   - On the Connections tab view and make connections for exported interfaces. Double-click an interface in the Export column to view all possible connections in the Connections column as pins. To restore the representation of the connections, and remove the interface from the Export column, click the pin.

1.6.1. Platform Designer 64-Bit Addressing Support

Platform Designer interconnect supports up to 64-bit addressing for all Platform Designer interfaces and IP components, with a range of: 0x0000 0000 0000 0000 to 0xFFFF FFFF FFFF FFFF, inclusive.

The address parameters appear in the Base and End columns in the System View tab, on the Address Map tab, in the parameter editor, and in validation messages. Platform Designer displays as many digits as needed in order to display the top-most set bit, for example, 12 hex digits for a 48-bit address.

A Platform Designer system can have multiple 64-bit masters, with each master having its own address space. You can share slaves between masters, and masters can map slaves to different addresses. For example, one master can interact with slave 0 at base address 0000_0000_0000, and another master can see the same slave at base address c000_0000_0000.

Intel Quartus Prime debugging tools provide access to the state of an addressable system via the Avalon memory mapped interconnect. These tools are also 64-bit compatible, and process within a 64-bit address space, including a JTAG to Avalon master bridge.
Platform Designer supports auto base address assignment for Avalon memory mapped components. In the Address Map tab, click Auto Assign Base Address.

Related Information
- Address Map Tab Help
- Address Span Extender Intel FPGA IP on page 320
- auto_assign_base_addresses on page 553

1.6.1.1. Support for Avalon Memory Mapped Non-Power of Two Data Widths

Platform Designer requires that you connect all multi point Avalon memory mapped connections to interfaces with data widths that are equal to powers of two.

Platform Designer issues a validation error if an Avalon memory mapped master or slave interface on a multi point connection is parameterized with a non-power of two data width.

Note: Avalon memory mapped point-to-point connections between an Avalon memory mapped master and an Avalon memory mapped slave are an exception, you can set their data widths to a non-power of two.

1.6.2. Connecting Masters and Slaves

Specify connections between master and slave components in the Address Map tab. This tab allows you to specify the address range that each memory-mapped master uses to connect to a slave in a Platform Designer system.

The Address Map tab shows the slaves on the left, the masters across the top, and the address span of the connection in each cell. If there is no connection between a master and a slave, the table cell is empty. In this case, use the Address Map tab to view the individual memory addresses for each connected master.

Platform Designer enables you to design a system where two masters access the same slave at different addresses. If you use this feature, Platform Designer labels the Base and End address columns in the System View tab as "mixed" rather than providing the address range.

To create or edit a connection between master and slave IP components:
1. In Platform Designer, click the Address Map tab.
2. Locate the table cell that represents the connection between the master and slave component pair.
3. Either type in a base address, or update the current base address in the cell. The base address of a slave component must be a multiple of the address span of the component. This restriction is a requirement of the Platform Designer interconnect, which provides an efficient address decoding logic, which in turn allows Platform Designer to achieve the best possible $f_{MAX}$. 
1.6.3. Changing a Conduit to a Reset

1. In the IP Catalog search box, locate **IOPLL Intel FPGA IP** and double-click to add the component to your system.
2. In the **System View** tab, click the **PLL** tab.
3. Click **View ➤ Component Instantiation** and open the **Component Instantiation** tab for the selected component.
4. In the **Signals & Interfaces** tab, select the **locked** conduit interface.
5. Change the **Type** from **Conduit** to **Reset Input**, and the **Synchronous edges** from **Deassert** to **None**.
6. Select the **locked [1]** signal below the **locked** interface.
7. Change the **Signal Type** from **export** to **reset_n**. The Direction option is unavailable now.
8. Click **Apply**.

The conduit interface changes to reset for the instantiated PLL component.

1.6.4. Wire-Level Connectivity

Wire-level connectivity enables you to manipulate wire-level connections in the system level view of Platform Designer. For example, you can enter a Verilog style syntax expression to drive an input port of an IP component. You can implement wire-level connectivity with the Platform Designer GUI or with the `qsys-script` utility.
After applying the expression, the port you specify moves from the current interface into a **Wire-Level Endpoint** interface. The new interface name appends `_wirelevel` to the existing interface name. If you remove the wire-level expression, the port restores to the original interface. However, not all interfaces are restorable to legal interfaces after certain ports change. Moving a port from its original interface might result in validation errors on the original interface.

After you move a port to a **Wire-Level Endpoint** interface, wire-level expressions must drive all bits in the vector. You cannot connect ports contained within this new interface type to any other interfaces.

The following general rules apply to wire-level expressions:

- Wire-level connectivity is only available on optional input ports.
- The wire-level expression can consist of input, output, and bi-directional ports, constant values, and logic terms using standard Verilog syntax.
- Wire-level expressions can only consist of ports within the same level of hierarchy. If you require elements from a higher or lower hierarchy, you must export the appropriate elements to the same hierarchical context so that they are available for use in wire-level expressions at the same hierarchy level.
- You can apply multiple expressions to a single input port unless they collide or cause bus contention.
- You must resolve validation errors occurring on the original interface for the interface to function correctly.

Platform Designer validates the wire-level expressions and provides messages for syntax, port existence, and other systematic errors. This validation includes the following:

- Validation of Verilog syntax.
- Warning if any sub-operator elements don’t match bit size.
- Warning if resulting combined bit size does not match the driven input port.
- Validation that all module and port names exist.
- Validation that all ports in a wire-level interface are input ports.
- Validation that all wire-level expressions drive each input port within a wire-level interface.
- Validation of no bus-contention, meaning that no one wire is driven by more than one expression.
- In a composed `_hw.tcl` module, validation that all ports driven by wire-level expressions are not in any connection.
- In a composed `_hw.tcl` module, validation that all ports driven by wire-level expressions are not exported.

After you define wire-level expressions for your system and resolve any errors, you next generate the system to create the Verilog files. When you apply the wire-level connections in the Platform Designer GUI, or with the `qsys-script` utility, the wire-level expression is inserts in the Verilog wrapper file that generates for your system. When you apply the wire-level connections with composed `_hw.tcl` commands, the wire-level expression inserts in the Verilog wrapper file that generates for the specified IP component.
### 1.6.4.1. Editing Wire-Level Expressions

After you add a wire-level expression to an optional input port, you can add, edit, or remove wire-level expressions and connections in the Platform Designer GUI.

Follow these steps to edit wire-level expressions in the Platform Designer GUI:

1. To specify a new wire-level expression, right-click an input port in the Hierarchy tab and click **Add Wire-Level Expression**. The **Edit Wire-Level Expression** dialog box appears.

#### Figure 32. Edit Wire-Level Expression Dialog Box

2. To construct the expression, drag operators or ports from the list of operators or ports, and drop them into the expression field. Refer to **Wire-Level Expression Syntax** on page 46 for a list of legal operators.

3. Click the text field at the top of the **Edit Wire-Level Expression** dialog box and press the Down Arrow key to enable the expression assistant. The assistant provides a context sensitive list of available operators at the cursor position.

4. Modify the elements of the expression in the workspace:
• To add a value to an expression, right-click a node and select Insert Value.
• Double-click on a value to enter a numeric value or port name.
• Click an operator node to change the operator type.
• Reorder nodes or move nodes between operators by dragging them.

5. To manage all wire-level expressions, click View ➤ Wire-Level Expression Editor. The Wire-Level Expression Editor allows you to add new wire-level expressions, edit, or remove existing wire-level expressions.

Figure 33. Wire-Level Expression Editor

![Wire-Level Expression Editor](image)

1.6.4.2. Wire-Level Expression Syntax

The wire-level expression derives from Verilog syntax. The following is an example and list of legal operators and elements that you can use for wire-level expressions.

Example Expressions:

- `foo1.port1[5:0] = foo2.port1[5:0]`
- `foo3.port1[8:4] = foo5.port1[4:0] & 5'b10101`
- `foo6.port1[0] = 'b1`
- `foo7.port1 = foo8.port1`
- `foo9.port1[0] = ~foo10.port1[0]`
- `foo10.port1[3:0] = foo11.port2[1:0] + 4'b1100`
- `foo12.port1[3:0] = {4{0}}`
- `foo13.port1[7:0] = {foo14.port1[3:0], 4'b0011}`

Table 6. Ports

<table>
<thead>
<tr>
<th>Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;instance_name&gt;.&lt;port_name&gt;</code></td>
<td>Whole port</td>
</tr>
<tr>
<td><code>&lt;instance_name&gt;.&lt;port_name&gt;[x]</code></td>
<td>Wire x of port</td>
</tr>
<tr>
<td><code>&lt;instance_name&gt;.&lt;port_name&gt;[y:x]</code></td>
<td>Wires x to y of port. Port ranges must be in decreasing order, for example a[1:0].</td>
</tr>
<tr>
<td><code>&lt;constant base x values&gt;</code></td>
<td>For example: 1, 'b1, 4’hf, 4’o7, 32’d9</td>
</tr>
</tbody>
</table>
### Table 7. Operators (Bitwise)

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>~</td>
<td>Negation</td>
</tr>
<tr>
<td>&amp;</td>
<td>AND</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>~&amp;</td>
<td>NAND</td>
</tr>
<tr>
<td>~</td>
<td></td>
</tr>
<tr>
<td>^</td>
<td>XOR</td>
</tr>
<tr>
<td>~^</td>
<td>XNOR</td>
</tr>
</tbody>
</table>

### Table 8. Operators (Logical)

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>?</td>
<td>Conditional</td>
</tr>
<tr>
<td>!</td>
<td>Negation</td>
</tr>
<tr>
<td>&amp;&amp;</td>
<td>AND</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 9. Operators (Relational, Equality, and Shift)

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;</td>
<td>Greater Than</td>
</tr>
<tr>
<td>&lt;</td>
<td>Less Than</td>
</tr>
<tr>
<td>&gt;=</td>
<td>Greater Than or Equal To</td>
</tr>
<tr>
<td>&lt;=</td>
<td>Less Than or Equal To</td>
</tr>
<tr>
<td>==</td>
<td>Equal To</td>
</tr>
<tr>
<td>!=</td>
<td>Not Equal To</td>
</tr>
<tr>
<td>&lt;&lt;</td>
<td>Shift Left</td>
</tr>
<tr>
<td>&gt;&gt;</td>
<td>Shift Right</td>
</tr>
</tbody>
</table>

### Table 10. Operators (Mathematical)

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>Addition</td>
</tr>
<tr>
<td>-</td>
<td>Subtraction</td>
</tr>
<tr>
<td>*</td>
<td>Multiplication</td>
</tr>
<tr>
<td>/</td>
<td>Division</td>
</tr>
<tr>
<td>%</td>
<td>Modulus</td>
</tr>
</tbody>
</table>
Table 11. Operators (Other)

<table>
<thead>
<tr>
<th>Operator</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>{integer {x}}</td>
<td>Replication of x</td>
</tr>
<tr>
<td>{x, y, ...}</td>
<td>Concatenation</td>
</tr>
</tbody>
</table>

1.6.4.3. Adding or Removing Ports from Wire-Level Endpoint Interfaces

You can quickly add or remove ports from wire-level interfaces.

Follow these steps to add or remove ports from wire-level endpoint interfaces:

1. To move the port to a wire-level endpoint interface, in the Hierarchy tab, right-click a port and then click Move Port to Wire-Level Interface. After you move a port to a wire-level endpoint interface, you can view and edit it in the Component Instantiation tab.

2. To remove the port from a wire-level endpoint interface, in the Hierarchy tab, right-click a port and then click Remove Port from Wire-Level Interface.

1.6.4.4. Scripting Wire-Level Expressions

Platform Designer supports system scripting commands to apply wire-level expressions to input ports in IP components.

The following commands function with the qsys-script utility or in a _hw.tcl file to set, retrieve, or remove an expression on a port:

```
set_wirelevel_expression <instance_or_port_bit> <expression>
get_wirelevel_expressions <instance_or_port_bit>
remove_wirelevel_expressions <instance_or_port_bit>
```

These commands require a string that you compose from the left-handed and right-handed components of the expression. Platform Designer reports errors in syntax, existence, or system hierarchy.

Related Information

- Wire-Level Connection Commands on page 562
- set_wirelevel_expression on page 563
- get_wirelevel_expressions on page 563
- remove_wirelevel_expressions on page 564

1.6.5. Previewing the System Interconnect

You can review a graphical representation of the Platform Designer interconnect before you generate the system. The System with Platform Designer Interconnect window shows how Platform Designer converts connections between interfaces to interconnect logic during system generation.

To open the System with Platform Designer Interconnect window, click System ➤ Show System With Platform Designer Interconnect, or click the Show System With Interconnect button in the Domains tab.
The System with Platform Designer Interconnect window has the following tabs:

- **System Contents**—displays the original instances in your system, as well as the inserted interconnect instances. Connections between interfaces are replaced by connections to interconnect where applicable.

- **Schematic**—displays a schematic representation that shows the multiple interconnects together as a complete system.

- **Hierarchy**—displays a system hierarchical navigator, expanding the system contents to show modules, interfaces, signals, contents of subsystems, and connections.

- **Parameters**—displays the parameters for the selected element in the Hierarchy tab.

- **Memory-Mapped Interconnect**—allows you to select a memory-mapped interconnect module and view its internal command and response networks. You can also insert pipeline stages to achieve timing closure.

Figure 34. **System with Platform Designer Interconnect window**

The **System Contents**, **Hierarchy**, and **Parameters** tabs are read-only. Edits that you apply on the **Memory-Mapped Interconnect** tab are automatically reflected on the **Interconnect Requirements** tab.

The **Memory-Mapped Interconnect** tab in the System with Platform Designer Interconnect window displays a graphical representation of command and response datapaths in your system. Datapaths allow you precise control over pipelining in the interconnect. Platform Designer displays separate figures for the command and response datapaths. You can access the datapaths by clicking their respective tabs in the **Memory-Mapped Interconnect** tab.

Each node element in a figure represents either a master or slave that communicates over the interconnect, or an interconnect sub-module. Each edge is an abstraction of connectivity between elements, and its direction represents the flow of the commands or responses.

Click **Highlight Mode (Path, Successors, Predecessors)** to identify edges and datapaths between modules. Turn on **Show Pipelinable Locations** to add greyed-out registers on edges where pipelining is allowed in the interconnect.
1.7. Specifying Interconnect Parameters

Specify system-wide or domain-specific interconnect parameters on the Domains tab. Interconnect parameters allow you to customize the implementation of the system interconnection.

Figure 35. Domains Tab

The Domains tab displays the Avalon memory mapped interfaces in your system, and allows you to specify legal values for available system-level or interface parameters. While specifying parameters, you can click Show System with Interconnect to view a schematic preview of the Platform Designer complete system interconnect.
Follow these steps to specify interconnect parameters:

1. Open or create a Platform Designer system.
2. Click View ➤ Domains.
3. Under Avalon Memory Mapped Domains, select one or more domains.
4. On the Domain tab, specify values for interconnect parameter settings, as Interconnect Parameters on page 51 describes.
5. To view a preview of the Platform Designer complete system interconnect, click Show System with Interconnect. Refer to Previewing the System Interconnect on page 48 for detailed description of this preview.

Related Information

• Platform Designer Interconnect on page 143
• Reset Interfaces on page 205
• Domains and Interfaces on page 412

1.7.1. Interconnect Parameters

The following parameters are available on the Domains tab:

Table 12. Interconnect Parameters

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Limit interconnect pipeline stages to</td>
<td>Specifies the maximum number of pipeline stages that Platform Designer can insert in each command and response path to increase the fMAX at the expense of additional latency. You can specify between 0 and 4 pipeline stages, where 0 means that the interconnect has a combinational datapath. This setting is specific for each Platform Designer system or subsystem.</td>
</tr>
<tr>
<td>Clock crossing adapter type</td>
<td>Specifies the default implementation for automatically inserted clock crossing adapters:</td>
</tr>
<tr>
<td>Handshake</td>
<td>This adapter uses a simple handshaking protocol to propagate transfer control signals and responses across the clock boundary. This methodology uses fewer hardware resources because each transfer is safely propagated to the target domain before the next transfer can begin. The Handshake adapter is appropriate for systems with low throughput requirements.</td>
</tr>
<tr>
<td>FIFO</td>
<td>This adapter uses dual-clock FIFOs for synchronization. The latency of the FIFO-based adapter is a couple of clock cycles more than the handshaking clock crossing component. However, the FIFO-based adapter can sustain higher throughput because it supports multiple transactions at any given time. FIFO-based clock crossing adapters require more resources. The FIFO adapter is appropriate for memory-mapped transfers requiring high throughput across clock domains.</td>
</tr>
<tr>
<td>Auto</td>
<td>If you select Auto, Platform Designer specifies the FIFO adapter for bursting links, and the Handshake adapter for all other links.</td>
</tr>
<tr>
<td>Automate default slave insertion</td>
<td>Directs Platform Designer to automatically insert a default slave for undefined memory region accesses during system generation.</td>
</tr>
<tr>
<td>Enable instrumentation</td>
<td>When you set this option to TRUE, Platform Designer enables debug instrumentation in the Platform Designer interconnect, which then monitors interconnect performance in the system console.</td>
</tr>
</tbody>
</table>

continued...
**Option** | **Description**
--- | ---
Interconnect reset source | Select **Default** or a specific reset signal in your design.
Burst adapter implementation | Allows you to choose the converter type that Platform Designer applies to each burst.
  | **Generic converter** (slower, lower area)
  | Default. Controls all burst conversions with a single converter that is able to adapt incoming burst types. This results in an adapter that has lower $f_{MAX}$ but smaller area.
  | **Per-burst-type converter** (faster, higher area)
  | Controls incoming bursts with a particular converter, depending on the burst type. This results in an adapter that has higher $f_{MAX}$ but higher area. This setting is useful when you have AXI masters or slaves and you want a higher $f_{MAX}$.
Width adapter implementation | **Generic converter** (slower, lower area)
  | Default. Controls all burst conversions with a single converter that is able to adapt incoming burst types. This results in an adapter that has lower $f_{MAX}$ but smaller area.
  | **Optimized converter** (faster, higher area)
  | Controls incoming bursts with a particular converter, depending on the burst type. This results in an adapter that has higher $f_{MAX}$ but higher area. This setting is useful when you have AXI masters or slaves and you want a higher $f_{MAX}$.
Enable ECC protection | Specifies the default implementation for ECC protection for memory elements.
  | **FALSE**
  | Default. Disables ECC protection for memory elements in the Platform Designer interconnect.
  | **TRUE**
  | Enables ECC protection for memory elements. Platform Designer interconnect sends uncorrectable errors arising from memory as DECODEERROR (DECERR) on the Avalon response bus.
Use synchronous reset | When set to **True**, all registers in the interconnect use synchronous reset. Assert the reset for at least 16 cycles and start transactions 16 cycles after deassertion of the reset. This period allows all the IP components to reset and come out of the reset state. To avoid deadlocks in the interconnect, reset masters and slaves simultaneously. If masters and slaves have different resets, slaves must reset only after responding to all necessary transactions. The *Use synchronous reset* option is enabled by default for Intel Stratix® 10 devices, but is disabled by default for all other devices. Enabling synchronous reset for the interconnect does not enable synchronous reset for IP components in the system. You must separately enable the synchronous reset parameter for any component.

### 1.8. Specifying Signal and Interface Boundary Requirements

If you export an interface that does not match the interface requirements of the system, Platform Designer generates component instantiation errors. You must match all the exported interfaces with the interface requirements of the system.

The **Interface Requirements** tab allows you to assign a component's top-level HDL module signals to an interface, specify the expected signal and interface boundary requirements for the interface, and to resolve any interface requirement mismatches. You can also modify the signal names in an exported interface.

1. To open the **Interface Requirements** tab, click **View ➤ Interface Requirements**.
2. To load the interface requirements from a Platform Designer system, click **Import Interface Requirements** in the **Interface Requirements** table. In the dialog box that appears, select the .ipxact representation of the Platform Designer system.

3. To manually add new interface or signal requirements, click <<add interface>> or <<add signal>> in the **Interface Requirements** table.

4. To correct the mismatches, select the missing or mismatched interface or signal in the **Current System** table and click >>.  
   
   **Note:** Platform Designer highlights the mismatches between the system and interface requirements in blue, and highlights the missing interfaces and signals in green.

5. To rename an exported signal or interface, use any of the following methods:
   
   - Double-click the signal or interface in **Current System** table.
   - Select the signal or interface in the **Current System** table and press F2.
   - Select the signal or interface in the **Current System** table and rename from the **Current Parameters** pane at the bottom of the tab. The **Current Parameters** pane displays all the parameters of the selected interface or signal.

**Related Information**

Editing Exported Interface Signal Names on page 54

### 1.8.1. Interface Requirements Tab Fields

The Platform Designer **Interface Requirements** tab contains the following fields.
Table 13. Interface Requirements Tab Fields

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Current System</strong></td>
<td>Displays all the exported interfaces in the current Platform Designer system. Add or remove the interfaces in the <strong>Current System</strong> by adding or removing components from the <strong>System View</strong> tab.</td>
</tr>
<tr>
<td><strong>Interface Requirements</strong></td>
<td>This table shows all the interface requirements set for the current Platform Designer system.</td>
</tr>
<tr>
<td><strong>Parameter Differences</strong></td>
<td>This table lists the <strong>Parameter Name</strong>, <strong>Current System Value</strong>, and <strong>Interface Requirement Value</strong> for the selected mismatched interface. Note: The <strong>Interface Requirements</strong> tab highlights in blue the signals and interfaces that are the same, but have different parameter values. Selecting a blue item populates the <strong>Parameter Differences</strong> table.</td>
</tr>
<tr>
<td><strong>Import Interface Requirements</strong></td>
<td>This button allows you to populate the <strong>Interface Requirements</strong> table from an IP-XACT(2) file representing a generic component or an entire Platform Designer system.</td>
</tr>
<tr>
<td><strong>Parameters</strong></td>
<td>This table lists the signal and interface parameters for the selected interface. You can view the table as <strong>Current Parameters</strong> when you select an interface or signal from the <strong>Current System</strong> table, and as <strong>Required Parameters</strong> when you select the signal or interface from <strong>Interface Requirements</strong> table. You can modify the name of the exported signal or interface from this table. For more information about how to edit the name of an exported signal or interface, refer to <strong>Edit the Name of Exported Interfaces and Signals</strong>.</td>
</tr>
</tbody>
</table>

**Related Information**
- Specifying Signal and Interface Boundary Requirements on page 52
- Creating a System Template for a Generic Component on page 131

1.8.2. Editing Exported Interface Signal Names

To rename an exported signal or interface:
- Double-click the signal or interface in **Current System** table.
- Select the signal or interface in the **Current System** table. The **Current Parameters** pane allows you to edit the parameters of the selected interface or signal.

**Note:** All other parameters in the **Current Parameters** except **Name** are read-only for the current system.

**Figure 37. Editing the Name of Exported Interfaces and Signals**

(2) Platform Designer supports importing and exporting files in IP-XACT 2009 format and exporting IP-XACT files in 2014 format.
1.9. Configuring Platform Designer System Security

Specify system-wide or interconnect-specific Security requirements on the Domains tab.

Platform Designer interconnect supports the Arm TrustZone* security extension. The Platform Designer Arm TrustZone security extension includes secure and non-secure transaction designations, and a protocol for processing between the designations, as Table 15 on page 58 describes.

The AXI \texttt{AxPROT} protection signal specifies a secure or non-secure transaction. When an AXI master sends a command, the \texttt{AxPROT} signal specifies whether the command is secure or non-secure. When an AXI slave receives a command, the \texttt{AxPROT} signal determines whether the command is secure or non-secure. Determining the security of a transaction while sending or receiving a transaction is a run-time protocol.

AXI masters and slaves can be TrustZone-aware. All other master and slave interfaces, such as Avalon memory mapped interfaces, are non-TrustZone-aware.

The Avalon specification does not include a protection signal. Consequently, when an Avalon master sends a command, there is no embedded security and Platform Designer recognizes the command as non-secure. Similarly, when an Avalon slave receives a command, the slave always accepts the command and responds.

Follow these steps to set compile-time security support for non-TrustZone-aware components:

1. To begin creating a secure system, add masters and slaves to your system, as Adding IP Components to a System on page 29 describes.
2. Make connections between the masters and slaves in your system, as Connecting Masters and Slaves on page 42 describes.
3. Click View ➤ Domains.
4. To specify security requirements for an interconnect, click the Interface tab under Interconnect Parameters,
5. Click the Add button.
6. In the **Identifier** column, select the interconnect in the **new_target** cell.
7. In the **Setting** column, select **Security**.
8. In the **Value** column, select the appropriate **Secure**, **Non-Secure**, **Secure Ranges**, or **TrustZone-aware** security for the interface. Refer to **System Security Options** on page 57 for details of each option.
9. After setting compile-time security options for non-TrustZone-aware master and slave interfaces, you must identify those masters that require a default slave before generation, as **Specifying a Default Slave** on page 57.

**Related Information**
- **Platform Designer Interconnect** on page 143
- **Platform Designer System Design Components** on page 302
1.9.1. System Security Options

Table 14. Security Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Secure</td>
<td>Master sends only secure transactions, and the slave receives only secure transactions. Platform Designer treats transactions from a secure master as secure. Platform Designer blocks non-secure transactions to a secure slave and routes to the default slave.</td>
</tr>
<tr>
<td>Non-Secure</td>
<td>The master sends only non-secure transactions, and the slave receives any transaction, secure or non-secure. Platform Designer treats transactions from a non-secure master as non-secure. Platform Designer allows all transactions, regardless of security status, to reach a non-secure slave.</td>
</tr>
<tr>
<td>Secure Ranges</td>
<td>Applies to only the slave interface. Allows you to specify secure memory regions for a slave. Platform Designer blocks non-secure transactions to secure regions and routes to the default slave. The specified address ranges within the slave’s address span are secure, all other address ranges are not. The format is a comma-separated list of inclusive-low and inclusive-high addresses, for example, 0x0:0xfff, 0x2000:0x20ff.</td>
</tr>
</tbody>
</table>
| TrustZone-aware | TrustZone-aware masters have signals that control the security status of their transactions. TrustZone-aware slaves can accept these signals and handle security independently. The following applies to secure systems that mix secure and non-TrustZone-aware components:  
  - All AXI, AMBA 3 AXI, and AMBA 3 AXI-Lite masters are TrustZone-aware.  
  - You can set AXI, AMBA 3 AXI, and AMBA 3 AXI-Lite slaves as TrustZone-aware, secure, non-secure, or secure range ranges.  
  - You can set non-AXI master interfaces as secure or non-secure.  
  - You can set non-AXI slave interfaces as secure, non-secure, or secure address ranges. |

1.9.2. Specifying a Default Slave

If a master issues "per-access" or "not allowed" transactions, your design must contain a default slave. Per-access refers to the ability of a TrustZone-aware master to allow or disallow access or transactions.

You can achieve an optimized secure system by partitioning your design and carefully designating secure or non-secure address maps to maintain reliable data. Avoid a design that includes a non-secure master that initiates transactions to a secure slave resulting in unsuccessful transfers, within the same hierarchy.

A transaction that violates security is rerouted to the default slave and subsequently responds to the master with an error. The following rules apply to specifying a default slave:

- You can designate any slave as the default slave.
- You can share a default slave between multiple masters.
- Have one default slave for each interconnect domain.
- An interconnect domain is a group of connected memory-mapped masters and slaves that share the same interconnect. The altera_error_response_slave component includes the required TrustZone features.

To designate a slave interface as the default slave for non TrustZone-aware interfaces, follow these steps:

2. In the System View, right-click any column and turn on the Security and Default Slave columns.

3. In the System View tab, turn on the Default Slave option for the slave interface. A master can have only one default slave.

Figure 39. Security and Default Slave Columns

![Security and Default Slave Columns](image)

Table 15. Secure and Non-Secure Access Between Master, Slave, and Memory Components

<table>
<thead>
<tr>
<th>Transaction Type</th>
<th>TrustZone-aware Master</th>
<th>Non-TrustZone-aware Master Secure</th>
<th>Non-TrustZone-aware Master Non-Secure</th>
</tr>
</thead>
<tbody>
<tr>
<td>TrustZone-aware slave/memory</td>
<td>OK</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>Non-TrustZone-aware slave (secure)</td>
<td>Per-access</td>
<td>OK</td>
<td>Not allowed</td>
</tr>
<tr>
<td>Non-TrustZone-aware slave (non-secure)</td>
<td>OK</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>Non-TrustZone-aware memory (secure region)</td>
<td>Per-access</td>
<td>OK</td>
<td>Not allowed</td>
</tr>
<tr>
<td>Non-TrustZone-aware memory (non-secure region)</td>
<td>OK</td>
<td>OK</td>
<td>OK</td>
</tr>
</tbody>
</table>

Related Information

- Error Response Slave Intel FPGA IP on page 325
- Designating a Default Slave on page 330
1.9.3. Accessing Undefined Memory Regions

Access to an undefined memory region occurs when a transaction from a master targets a memory region unspecified in the slave memory map. To ensure predictable response behavior when this condition occurs, you must specify a default slave, as Specifying a Default Slave on page 57 describes.

You can designate any memory-mapped slave as a default slave. Have only one default slave for each interconnect domain in your system. Platform Designer then routes undefined memory region accesses to the default slave, which terminates the transaction with an error response.

Note: If you do not specify the default slave, Platform Designer automatically assigns the slave at the lowest address within the memory map for the master that issues the request as the default slave.

Accessing undefined memory regions can occur in the following cases:

- When there are gaps within the accessible memory map region that are within the addressable range of slaves, but are not mapped.
- Accesses by a master to a region that does not belong to any slaves that is mapped to the master.
- When a non-secured transaction is accessing a secured slave. This applies to only slaves that are secured at compilation time.
- When a read-only slave is accessed with a write command, or a write-only slave is accessed with a read command.

1.10. Upgrading Outdated IP Components in Platform Designer

When you open a Platform Designer system containing outdated IP components, you can retain and use the RTL of previously generated IP components within the Platform Designer system. If Platform Designer is unable to locate the IP core's original version, you cannot re-parametrize the IP core without upgrading the IP core to the latest version. However, Platform Designer allows you to view the parametrization of the original IP component without upgrading.

To upgrade individual IP components in your Platform Designer system:

1. Click View ➤ Parameters.
2. Select the outdated IP component in the Hierarchy or the System View tab.
3. Click the Parameters tab. This tab displays information on the current version, as well as the installed version of the selected IP component.
4. Click Upgrade. Platform Designer upgrades the IP component to the installed version, and deletes all the RTL files associated with the IP component.
To upgrade an IP component from the command-line, type the following:

```bash
qsys-generate --upgrade-ip-cores <ip_file>
```

To upgrade all the IP components in your Platform Designer system, open the associated project in the Intel Quartus Prime software, and click Project ➤ Upgrade IP Components.

### 1.11. Synchronizing System Component Information

When a component instantiation values do match the component's corresponding .ip file, Platform Designer reports these mismatches as Component Instantiation Warnings in the System Messages tab.

You must synchronize any mismatches between the component instantiation, and the component's corresponding .ip prior to system generation.

Follow these steps to synchronize one or more components in your system:

1. Select the mismatched signal or interface in the System View tab, and then and click View ➤ System Info. Alternatively, you can double-click the corresponding Component Instantiation Warning in the System Messages tab.
Figure 41. System Info Tab

2. View any component mismatches in the System Info tab. Select individual interfaces, signals, or parameters to view the specific value differences in the Component and IP file columns. Value mismatches between the Component Instantiation and the IP file appear in blue. Missing elements appear in green.

3. To synchronize the Component Instantiation and IP file .ip values in the system, perform one or more of the following:
   - Select a specific mismatched parameter, interface, or signal and click >> to synchronize the items.
   - Click Sync All to synchronize all values for the current component.
   - Click Sync All System Info to synchronize all IP components in the current system at once.

1.11.1. System Info Tab Fields

Table 16. System Info Tab Fields

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component Instantiation</td>
<td>Lists the signals and interfaces for the selected component with respect to the component instantiation. Value mismatches between the Component Instantiation and the IP file appear in blue. Missing elements appear in green.</td>
</tr>
<tr>
<td>Component Column</td>
<td>Displays the selected interface parameter value with respect to the Component Instantiation.</td>
</tr>
</tbody>
</table>

continued...
1.12. Validating System Integrity

You can use any of the following methods to validate Platform Designer system integrity.

- To perform system integrity check for the entire system, click the **Validate System Integrity** button at the bottom of main Platform Designer window. If validation finds errors, click **Reload and Update All Components** to reload signal and interface values from the corresponding IP component file.

**Figure 42. Validating System Integrity**

- View any errors and warnings on the **System Messages** tab. Double-click the warning or error messages to locate the issue in the **System View** or **Parameters** tab to correct the issue. Platform Designer generates the following types of system validation errors and warnings:

**Table 17. System Messages Types in Platform Designer**

<table>
<thead>
<tr>
<th>System Messages Types</th>
<th>Description</th>
</tr>
</thead>
</table>
| Component Instantiation Warning | Indicates the mismatches between system information parameters or IP core parameterization errors. A system information parameters mismatch refers to the mismatch between an IP component’s system parameter expectations and the component’s saved system information parameters in the corresponding .ip file. For example:  
  • Interface types do not match  
  • Interface is missing  
  • Port has been moved to another interface |

continued...
### System Messages Types

<table>
<thead>
<tr>
<th>System Messages Types</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port role has changed</td>
<td></td>
</tr>
<tr>
<td>Interface assignment is mismatched</td>
<td></td>
</tr>
<tr>
<td>Interface assignment is missing</td>
<td></td>
</tr>
<tr>
<td><strong>Component Instantiation Error</strong></td>
<td>Indicates the mismatches between HDL entity name, compilation library, or ports which results in downstream compilation errors. The component instantiation errors always indicate the fundamental mismatches between generated system and interconnect fabric RTL. For example:</td>
</tr>
<tr>
<td>Port is missing from the ip file</td>
<td></td>
</tr>
<tr>
<td>Port is missing from instantiation</td>
<td></td>
</tr>
<tr>
<td>Port direction has changed</td>
<td></td>
</tr>
<tr>
<td>Port HDL type has changed</td>
<td></td>
</tr>
<tr>
<td>Port width has changed</td>
<td></td>
</tr>
<tr>
<td>Interface Parameter is mismatched</td>
<td></td>
</tr>
<tr>
<td>Interface Parameter is missing</td>
<td></td>
</tr>
<tr>
<td><strong>System Connectivity Warning</strong></td>
<td>Platform Designer system connectivity warnings.</td>
</tr>
<tr>
<td><strong>System Connectivity Error</strong></td>
<td>Platform Designer system connectivity errors.</td>
</tr>
</tbody>
</table>

### 1.12.1. Validating the System Integrity of Individual Components

To validate the system integrity for your IP components:

1. Select the IP component in the **System View** tab.
2. Right-click and select **Validate Component Footprint** to check for any mismatches between the IP component and its .ip file representation.
3. If there are any errors, click **Reload Component Footprint** to reload the signals and interfaces for the component from the .ip file.

### 1.13. Generating a Platform Designer System

Platform Designer system generation creates the interconnect between IP components, and generates files for Intel Quartus Prime synthesis and simulation in supported third-party tools.

Follow these steps to generate a Platform Designer system:

1. Open a system in Platform Designer.
2. Consider whether to specify a unique generation ID, as **Specifying the Generation ID** on page 65 describes.
3. Click the **Generate HDL** button. The **Generation** dialog box appears.
4. Specify options for generation of **Synthesis, Simulation**, and testbench files, as **Generation Dialog Box Options** on page 64 describes.
5. Consider whether to specify options for **Parallel IP Generation**, as **Disabling or Enabling Parallel IP Generation** on page 66 describes.
Figure 43. Platform Designer Generation Dialog Box

6. To start system generation, click **Generate**.

   *Note:* Platform Designer may add unique suffixes (hashes) to ip component files during generation to ensure uniqueness of the file. The uniqueness of the files is necessary because the IP component is dynamic. The RTL generates during runtime, according to the input parameters. This methodology ensures no collisions between the multiple variants of the same IP. The hash derives from the parameter values that you specify. A given set of parameter values produces the same hash for each generation.

1.13.1. Generation Dialog Box Options

Platform Designer system generation creates files for Intel Quartus Prime synthesis and supported third-party simulators. The **Generation** dialog box appears when you click **Generate HDL**, or when you attempt to close a system prior to generation.

By default, the synthesis and simulation files generate into the Platform Designer project directory.
You can specify the following system generation options in the **Generation** dialog box:

### Table 18. Generation Dialog Box Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create HDL design files for synthesis</td>
<td>Allows you to specify Verilog or VHDL file type generation for the system's top-level definition and child instances. Select <strong>None</strong> to skip generation of synthesis files.</td>
</tr>
<tr>
<td>Create timing and resource estimates for each IP in your system to be used with third-party synthesis tools</td>
<td>Generates a non-functional Verilog Design File (.v) for use by supported third-party EDA synthesis tools. Estimates timing and resource usage for the IP component. The generated netlist file name is <code>&lt;ip_component_name&gt;_syn.v</code>.</td>
</tr>
<tr>
<td>Create Block Symbol File (.bsf)</td>
<td>Generates a Block Symbol File (.bsf) for use in a larger system schematic Block Diagram File (.bdf).</td>
</tr>
<tr>
<td>IP-XACT</td>
<td>Generates an IP-XACT file for the system, and adds the file to the IP Catalog. Note: Platform Designer supports importing and exporting files in IP-XACT 2009 format and exporting IP-XACT files in 2014 format.</td>
</tr>
<tr>
<td>Generate IP Core Documentation</td>
<td>Generates the IP user guide documentation for the components in your system (when available).</td>
</tr>
<tr>
<td>Create simulation model</td>
<td>Allows you to generate Verilog HDL or VHDL simulation model and simulation script files. Note: ModelSim* - Intel FPGA Edition supports native, mixed-language (VHDL/Verilog/SystemVerilog) simulation. Therefore, Intel simulation libraries may not be compatible with single language simulators. If you have a VHDL-only license, some versions of ModelSim simulators may not support simulation for IPs written in Verilog. As a workaround, you can use ModelSim - Intel FPGA Edition, or purchase a mixed language simulation license from Mentor.</td>
</tr>
<tr>
<td>Clear output directories for selected generation targets</td>
<td>Clears previous synthesis and simulation file generation data for the current system.</td>
</tr>
<tr>
<td>Use multiple processors for faster IP generation (when available)</td>
<td>Disables or enables parallel IP generation for faster IP generation using multiple processors when available in your system.</td>
</tr>
</tbody>
</table>

**Note:** For a list of Intel-supported simulators, refer to *Simulating Intel Designs* in the *Intel Quartus Prime Pro Edition User Guide: Third-Party Simulation*.

**Related Information**
- Editing Wire-Level Expressions on page 45
- List of Supported Simulators

### 1.13.2. Specifying the Generation ID

You can specify the **Generation ID** to uniquely identify that specific system generation. This parameter allows system tools, such as Nios II or HPS (Hard Processor System), to verify software-build compatibility with a specific Platform Designer system.

The **Generation ID** parameter is a unique integer value that derives from the timestamp during Platform Designer system generation. You can optionally modify this value to a value of your choosing to identify the system.
To specify the **Generation ID** parameter:
1. In the **Hierarchy** tab, select the top-level system.
2. Click **View ➤ Parameters**.
3. Under **System Identifier**, view or edit the value of **Generation ID**.

**Figure 44. Generation ID in Parameters Tab**

![Parameters Tab with Generation ID](image)

### 1.13.3. Disabling or Enabling Parallel IP Generation

By default, the Intel Quartus Prime software and Platform Designer use multiple processors if available in your PC or workstation for faster IP generation. IP generation for large systems can be time consuming. The use of parallel IP generation can potentially reduce the total IP generation time for designs with large numbers of IP.

The `qsys-generate` command line utility similarly uses parallel IP generation by default when multiple processors are available. You can disable or enable the use of parallel IP generation for the current IP generation, for the current project, or for all projects. You can also specify the maximum number of processors to use for parallel IP generation.

**Disabling or Enabling Parallel IP Generation for the Current IP Generation**

1. Open a system or IP component in Platform Designer, and click **Generate HDL**.
2. In the **Generation** dialog box, turn on or off **Use multiple processors for faster IP generation (when available)**. Platform Designer retains this setting for subsequent generations.
Figure 45. Disables or Enables Parallel IP Generation for the Current IP Generation

Disabling or Enabling Parallel IP Generation for a Single Project

1. In the Intel Quartus Prime software, click **Assignments ➤ Settings ➤ Compilation Process Settings**.

2. Under **Parallel IP Generation**, select **Disable parallel generation of current Quartus project IPs** to disable parallel IP generation for the current project. Select **Enable parallel generation of current Quartus project IPs** to enable parallel IP generation for the current project.

Figure 46. Enables or Disables Parallel IP Generation for a Single Project

Alternatively, you can disable or enable parallel IP generation for a project with the following line in the project .qsf file:

```
set_global_assignment -name PROJECT_IP_GEN_PARALLEL_ENABLED <off|on>
```

Figure 47. Enables or Disables Parallel IP Generation for all Projects

Disabling or Enabling Parallel IP Generation for all Projects

1. In the Intel Quartus Prime software, click **Tools ➤ Options ➤ IP Settings**.

2. Under **Parallel IP Generation**, enable or disable the **Enable parallel generation of Quartus IPs in all projects** option. When enabled, the Intel Quartus Prime software uses multiple processors (if available in your system) for faster IP generation.

Alternatively, you can disable or enable parallel IP generation for all projects by adding the following line to the quartus2.ini file:

```
ENABLE_PARALLEL_IP_GEN=<off|on>
```
Specifying the Maximum Number of Processors

Parallel IP generation derives the maximum number of processors to use from the Maximum processors allowed Compiler setting. If you specify no value for this setting, the Intel Quartus Prime software selects an appropriate number based on the available processors, and the number of tasks the processors can execute in parallel.

1. In the Intel Quartus Prime software, click Assignments ➤ Settings ➤ Compilation Process Settings.

2. Under Parallel compilation, specify the Maximum processors allowed for processing designs.

Alternatively, you can set the number of processors with the following line in the project .qsf file:

```
set_global_assignment -name NUM_PARALLEL_PROCESSORS <number>
```

For the qsys-generate command line utility, you can use the --parallel[=<number>] argument, where <number> indicates the target number of processors.

Related Information
- Compilation Process Settings Help
- qsys-generate Command-Line Options on page 378

1.13.4. Files Generated for Intel FPGA IP Cores and Platform Designer Systems

The Intel Quartus Prime Pro Edition software generates the following output file structure for IP cores and Platform Designer systems. Platform Designer automatically adds the generated .ip and .qsys files to your Intel Quartus Prime project.

For generated IP components, Platform Designer appends unique suffixes (hashes) to the IP component’s RTL file name to ensure uniqueness of the RTL file and IP component file. The uniqueness of the files is necessary because a system can have multiple instances of the same IP, each with different parameterizations, resulting in multiple variances of the IP component. The hash derives from the parameterization that you specify for the IP component. This methodology ensures no collisions between the multiple variants of the same IP.
Figure 48. Files generated for IP cores and Platform Designer Systems

Table 19. IP Core and Platform Designer Simulation Files

<table>
<thead>
<tr>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;my_system&gt;.qsys</code></td>
<td>The Platform Designer system.</td>
</tr>
<tr>
<td><code>&lt;my_subsystem&gt;.qsys</code></td>
<td>The Platform Designer subsystem.</td>
</tr>
<tr>
<td><code>ip/</code></td>
<td>Contains the parameter files for the IP components in the system and subsystems.</td>
</tr>
<tr>
<td>File Name</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .cmp</code></td>
<td>The VHDL Component Declaration (.cmp) file is a text file that contains local generic and port definitions that you can use in VHDL design files.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .-generation.rpt</code></td>
<td>IP or Platform Designer generation log file. A summary of the messages during IP generation.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .qgsimc</code></td>
<td>Simulation caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .qgsynth</code></td>
<td>Synthesis caching file that compares the .qsys and .ip files with the current parameterization of the Platform Designer system and IP core. This comparison determines if Platform Designer can skip regeneration of the HDL.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .qip</code></td>
<td>Contains all the required information about the IP component to integrate and compile the IP component in the Intel Quartus Prime software.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .csv</code></td>
<td>Contains information about the upgrade status of the IP component.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .bsf</code></td>
<td>A Block Symbol File (.bsf) representation of the IP variation for use in Block Diagram Files (.bdf).</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .spd</code></td>
<td>Required input file for ip-make-simscript to generate simulation scripts for supported simulators. The .spd file contains a list of files generated for simulation, along with information about memories that you can initialize.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .ppf</code></td>
<td>The Pin Planner File (.ppf) stores the port and node assignments for IP components created for use with the Pin Planner.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; _bb.v</code></td>
<td>Use the Verilog black box (_bb.v) file as an empty module declaration for use as a black box.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .sip</code></td>
<td>Contains information required for NativeLink simulation of IP components. Add the .sip file to your Intel Quartus Prime Standard Edition project to enable NativeLink for supported devices. The Intel Quartus Prime Pro Edition software does not support NativeLink simulation.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; _inst.v</code> or <code>&lt;my_ip&gt; _inst.vhd</code></td>
<td>HDL example instantiation template. Copy and paste the contents of this file into your HDL file to instantiate the IP variation.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .regmap</code></td>
<td>If the IP contains register information, the Intel Quartus Prime software generates the .regmap file. The .regmap file describes the register map information of master and slave interfaces. This file complements the .soicinfo file by providing more detailed register information about the system. This file enables register display views and user customizable statistics in System Console.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .svd</code></td>
<td>Allows HPS System Debug tools to view the register maps of peripherals connected to HPS within a Platform Designer system. During synthesis, the Intel Quartus Prime software stores the .svd files for slave interface visible to the System Console masters in the .sof file in the debug session. System Console reads this section, which Platform Designer can query for register map information. For system slaves, Platform Designer can access the registers by name.</td>
</tr>
<tr>
<td><code>&lt;my_ip&gt; .v &lt;my_ip&gt; .vhd</code></td>
<td>HDL files that instantiate each submodule or child IP core for synthesis or simulation.</td>
</tr>
<tr>
<td>mentor/</td>
<td>Contains a ModelSim script msim_setup.tcl to set up and run a simulation.</td>
</tr>
<tr>
<td>aldec/</td>
<td>Contains a Riviera-PRO* script rivierapro_setup.tcl to setup and run a simulation.</td>
</tr>
<tr>
<td>/synopsys/vcs</td>
<td>Contains a shell script vcs_setup.sh to set up and run a VCS* simulation.</td>
</tr>
<tr>
<td>/synopsys/vcsmx</td>
<td>Contains a shell script vcsmx_setup.sh and synopsys_sim_setup file to set up and run a VCS MX simulation.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>/cadence</td>
<td>Contains a shell script <code>ncsim_setup.sh</code> and other setup files to set up and run an NCSIM simulation.</td>
</tr>
<tr>
<td>/xcelium</td>
<td>Contains a shell script <code>xcelium_setup.sh</code> and other setup files to set up and run a Xcelium® simulation.</td>
</tr>
<tr>
<td>/common</td>
<td>Contains a set of Tcl files, <code>&lt;simulator&gt;_files.tcl</code>, which provide all design related simulation information required by a corresponding simulation script. The Tcl file contains designs from current system-level hierarchy, and references to sub-systems and IP components.</td>
</tr>
<tr>
<td>/submodules</td>
<td>Contains HDL files for the IP core submodule.</td>
</tr>
<tr>
<td>&lt;IP submodule&gt;/</td>
<td>For each generated IP submodule directory, Platform Designer generates <code>/synth</code> and <code>/sim</code> sub-directories.</td>
</tr>
</tbody>
</table>

### 1.13.5. Generating System Testbench Files

Platform Designer can generate testbench files that instantiate the current Platform Designer system and add Bus Functional Models (BFMs) to drive the top-level interfaces. BFMs interact with the system in the simulator.

You can generate a standard or simple testbench system with BFM or Mentor Verification IP (for AMBA 3 AXI or AMBA 4 AXI) components that drive the external interfaces of the system. Platform Designer generates a Verilog HDL or VHDL simulation model for the testbench system to use in the simulation tool.

First generate a testbench system, and then modify the testbench system in Platform Designer before generating the simulation model. Typically, you select only one of the simulation model options.

Follow these steps to generate system testbench files:

1. Open and configure a system in Platform Designer.
2. Click **Generate ➤ Generate Testbench System**. The **Generation** dialog box appears.
3. Specify options for the test bench system:

#### Table 20. Testbench Generation Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create testbench Platform Designer system</td>
<td>Specifies a simple or standard testbench system:</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
</table>
| • **Standard, BFMs for standard Platform Designer Interconnect**—Creates a testbench Platform Designer system with BFM IP components attached to exported Avalon and AMBA 3 AXI or AMBA 3 AXI interfaces. Includes any simulation partner modules specified by IP components in the system. The testbench generator supports AXI interfaces and can connect AMBA 3 AXI or AMBA 3 AXI interfaces to Mentor Graphics AMBA 3 AXI or AMBA 3 AXI master/slave BFMs. However, BFMs support address widths only up to 32-bits.  
| • **Simple, BFMs for clocks and resets**—Creates a testbench Platform Designer system with BFM IP components driving only clock and reset interfaces. Includes any simulation partner modules specified by IP components in the system. |

<table>
<thead>
<tr>
<th>Create testbench simulation model</th>
<th>Specifies Verilog HDL or VHDL simulation model files and simulation scripts for the testbench. Use this option if you do not need to modify the Platform Designer-generated testbench before running the simulation.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output directory</td>
<td>Specifies the path for output of generated testbench files. Turn on <strong>Clear output</strong> to remove any previously generated content from the location.</td>
</tr>
<tr>
<td>Parallel IP Generation</td>
<td>Turn on <strong>Use multiple processors for faster IP generation (when available)</strong> to generate IP using multiple CPUs when available in your system.</td>
</tr>
</tbody>
</table>

4. Click **Generate**. The testbench files generate according to your specifications.

5. Open the testbench system in Platform Designer. Make changes to the BFMs, as needed, such as changing the instance names and **VHDL ID** value. For example, you can modify the **VHDL ID** value in the **Avalon Interrupt Source Intel FPGA** IP component.

6. If you modify a BFM, regenerate the simulation model for the testbench system.

7. Compile the system and load the Platform Designer system and testbench into your simulator, and then run the simulation.

### 1.13.5.1. Platform Designer Testbench Simulation Output Directories

Platform Designer generates the following testbench files.
### 1.13.5.2. Platform Designer Testbench Files

Platform Designer generates the following testbench files.

<table>
<thead>
<tr>
<th>File Name or Directory Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;system&gt;_tb.qsys</code></td>
<td>The Platform Designer testbench system.</td>
</tr>
<tr>
<td><code>&lt;system&gt;_tb.v</code> or <code>&lt;system&gt;_tb.vhd</code></td>
<td>The top-level testbench file that connects BFM to the top-level interfaces of <code>&lt;system&gt;_tb.qsys</code>.</td>
</tr>
</tbody>
</table>

*continued...*
1.13.6. Generating Example Designs for IP Components

Some Platform Designer IP components include example designs that you can use or modify to replicate similar functionality in your own system. You must generate the examples to view or use them.

Use any of the following methods to generate example designs for IP components:

- Double-click the IP component in the Platform Designer IP Catalog or **System View** tab. The parameter editor for the component appears. If available, click the **Example Design** button in the parameter editor to generate the example design. The **Example Design** button only appears in the parameter editor if an example is available.

- For some IP components, click **Generate > Generate Example Design** to access an example design. This command only enables when a design example is available.
The following Platform Designer system example designs demonstrate various design features and flows that you can replicate in your Platform Designer system.

**Related Information**
Intel FPGA Design Example Web Page

### 1.13.7. Incremental System Generation Example

You can modify the parameters of an IP component and regenerate the RTL for just that particular IP component.

The following example demonstrates incremental generation of a Platform Designer System:

1. Create a new Platform Designer system, as Creating or Opening a Platform Designer System on page 14 describes.
2. Use the IP Catalog to locate and add the On-Chip Memory (RAM or ROM) Reset Bridge, and Clock Bridge components to the system, as Adding IP Components to a System on page 29 describes.
3. Make the necessary system connections between the IP components added to the system, as Connecting System Components on page 39 describes.
4. To save and close the system without generating, click **File ➤ Save** and close Platform Designer.
5. In the Intel Quartus Prime software, click **File ➤ Open Project**.
6. Select the Intel Quartus Prime project associated with your saved Platform Designer system. The Intel Quartus Prime software opens the project and the associated Platform Designer system.
7. To start the compilation of the Intel Quartus Prime project, click **Processing ➤ Start Compilation**.
8. After compilation completes, in Platform Designer, click **File ➤ Open**.
9. Select the .ip file for any one of the IP components in your saved system.
10. Modify some parameter in this .ip file.

   **Note:** Make sure your modifications do not affect the parent system, requiring a system update by running Validate System Integrity from within the Platform Designer system after loading the parent system, or by running qsys-validate from the command-line.

11. To save the IP file, click **File ➤ Save**.
12. To restart the compilation of the same Intel Quartus Prime project with modified Platform Designer system, click **Processing ➤ Start Compilation** in the Intel Quartus Prime software. Platform Designer generates the RTL only for the modified IP component, skipping the generation of the other components in the system.

### 1.13.8. Generating the HPS IP Component System View Description File

Platform Designer systems that contain an HPS IP component generate a System View Description (.svd) file that lists peripherals connected to the Arm processor.
The .svd (or CMSIS-SVD) file format is an XML schema specified as part of the Cortex Microcontroller Software Interface Standard (CMSIS) that Arm provides. The .svd file allows HPS system debug tools (such as the DS-5 Debugger) to view the register maps of peripherals connected to HPS in a Platform Designer system.

Related Information
- Component Interface Tcl Reference on page 594
- CMSIS - Cortex Microcontroller Software

1.13.9. Generating Header Files for Master Components

You can use the sopc-create-header-files command from the Nios II command shell to create header files for any master component in your Platform Designer system. The Nios II tool chain uses this command to create the processor's system.h file. You can also use this command to generate system level information for a hard processing system (HPS) in Intel's SoC devices or other external processors. The header file includes address map information for each slave, relative to each master that accesses the slave. Different masters may have different address maps to access a particular slave component. By default, the header files are in C format and have a .h suffix. You can select other formats with appropriate command-line options.

Table 22. sopc-create-header-files Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;sopc&gt;</td>
<td>Path to Platform Designer .sopcinfo file, or the file directory. If you omit this option, the path defaults to the current directory. If you specify a directory path, you must make sure that there is a .sopcinfo file in the directory.</td>
</tr>
<tr>
<td>--separate-masters</td>
<td>Does not combine a module's masters that are in the same address space.</td>
</tr>
<tr>
<td>--output-dir[=&lt;dirname&gt;]</td>
<td>Allows you to specify multiple header files in dirname. The default output directory is '.'.</td>
</tr>
<tr>
<td>--single[=&lt;filename&gt;]</td>
<td>Allows you to create a single header file, filename.</td>
</tr>
<tr>
<td>--single-prefix[=&lt;prefix&gt;]</td>
<td>Prefixes macros from a selected single master.</td>
</tr>
<tr>
<td>--module[=&lt;moduleName&gt;]</td>
<td>Specifies the module name when creating a single header file.</td>
</tr>
<tr>
<td>--master[=&lt;masterName&gt;]</td>
<td>Specifies the master name when creating a single header file.</td>
</tr>
<tr>
<td>--format[=&lt;type&gt;]</td>
<td>Specifies the header file format. Default file format is .h.</td>
</tr>
<tr>
<td>--silent</td>
<td>Does not display normal messages.</td>
</tr>
<tr>
<td>--help</td>
<td>Displays help for sopc-create-header-files.</td>
</tr>
</tbody>
</table>

By default, the sopc-create-header-files command creates multiple header files. There is one header file for the entire system, and one header file for each master group in each module. A master group is a set of masters in a module in the same address space. In general, a module may have multiple master groups. Addresses and available devices are a function of the master group.

Alternatively, you can use the --single option to create one header file for one master group. If there is one CPU module in the Platform Designer system with one master group, the command generates a header file for that CPU's master group. If there are no CPU modules, but there is one module with one master group, the command generates the header file for that module's master group.
You can use the --module and --master options to override these defaults. If your module has multiple master groups, use the --master option to specify the name of a master in the desired master group.

Table 23.  Supported Header File Formats

<table>
<thead>
<tr>
<th>Type</th>
<th>Suffix</th>
<th>Uses</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>h</td>
<td>.h</td>
<td>C/C++ header files</td>
<td>#define FOO 12</td>
</tr>
<tr>
<td>m4</td>
<td>.m4</td>
<td>Macro files for m4</td>
<td>m4_define(&quot;FOO&quot;, 12)</td>
</tr>
<tr>
<td>sh</td>
<td>.sh</td>
<td>Shell scripts</td>
<td>FOO=12</td>
</tr>
<tr>
<td>mk</td>
<td>.mk</td>
<td>Makefiles</td>
<td>FOO := 12</td>
</tr>
<tr>
<td>pm</td>
<td>.pm</td>
<td>Perl scripts</td>
<td>$macros{FOO} = 12;</td>
</tr>
</tbody>
</table>

Note: You can use the sopc-create-header-files command when you want to generate C macro files for DMAs that have access to memory that the Nios II does not have access to.

1.14. Simulating a Platform Designer System

You can simulate a Platform Designer system in a supported third-party simulator to verify and debug operation. Platform Designer generates the simulation models for your system, along with optional scripts to set up the simulation environment for specific, supported third-party simulators.

Platform Designer generates simulation scripts for all .ip and .qsys files of a system and places the files in the simulation script output folder (<top-level system name>/sim/<simulator name>).

Platform Designer always generates the simulation scripts from the currently loaded system down. Alternatively, you can open a subsystem to generate a simulation script just for that subsystem.

You can use scripts to compile the required device libraries and system design files in the correct order and elaborate or load the top-level system for simulation.

Table 24.  Simulation Script Variables

The simulation scripts provide variables that allow flexibility in your simulation environment.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP_LEVEL_NAME</td>
<td>If the testbench Platform Designer system is not the top-level instance in your simulation environment because you instantiate the Platform Designer testbench within your own top-level simulation file, set the TOP_LEVEL_NAME variable to the top-level hierarchy name.</td>
</tr>
<tr>
<td>QSYS_SIMDIR</td>
<td>If the simulation files generated by Platform Designer are not in the simulation working directory, use the QSYS_SIMDIR variable to specify the directory location of the Platform Designer simulation files.</td>
</tr>
<tr>
<td>QUARTUS_INSTALL_DIR</td>
<td>Points to the Quartus installation directory that contains the device family library.</td>
</tr>
</tbody>
</table>
Example 3. **Top-Level Simulation HDL File for a Testbench System**

The example below shows the `pattern_generator_tb` generated for a Platform Designer system called `pattern_generator`. The `top.sv` file defines the top-level module that instantiates the `pattern_generator_tb` simulation model, as well as a custom SystemVerilog test program with BFM transactions, called `test_program`.

```verilog
top();
module top();
pattern_generator_tb tb();
test_program pgm();
endmodule
```

1.14.1. **Adding Assertion Monitors for Simulation**

You can add monitors to Avalon Memory-Mapped, AXI, and Avalon Streaming interfaces in your system to verify protocol and test coverage with a simulator that supports SystemVerilog assertions.

**Note:** ModelSim - Intel FPGA Edition does not support SystemVerilog assertions. If you want to use assertion monitors, you must use a supported third-party simulator. For more information, refer to *Introduction to Intel FPGA IP Cores*.

**Figure 50. Inserting an Avalon Memory-Mapped Monitor Between an Avalon Memory-Mapped Master and Slave Interface**

This example demonstrates the use of a monitor with an Avalon Memory-Mapped monitor between the `pcie_compiler_bar1_0_Prefetchable Avalon Memory-Mapped master interface, and the `dma_0 control_port_slave Avalon Memory-Mapped slave interface.

Similarly, you can insert an Avalon Streaming monitor between Avalon Streaming source and sink interfaces.

1.14.2. **Simulating Software Running on a Nios II Processor**

To simulate the software in a system driven by a Nios II processor, generate the simulation model for the Platform Designer testbench system with the following steps:

1. Click **Generate ➤ Generate Testbench System**.
2. In the **Generation** dialog box, select **Simple, BFMs for clocks and resets**.
3. For **Create testbench simulation model**, select **Verilog** or **VHDL**.
4. Click **Generate**.
5. Open the Nios II Software Build Tools for Eclipse.
6. Set up an application project and board support package (BSP) for the `<system>.sopcinfo file.`
7. To simulate, right-click the application project in Eclipse, and then click Run as ➤ Nios II ModelSim. This command prepares the ModelSim simulation environment, and compiles and loads the Nios II software simulation.

8. To run the simulation in ModelSim, type run -all in the ModelSim transcript window.

9. Set the ModelSim settings and select the Platform Designer Testbench Simulation Package Descriptor (.spd) file, <system>_tb.spd. The .spd file generates with the testbench simulation model for Nios II designs, and specifies the files you require for Nios II simulation.

Related Information
Nios II Gen2 Software Developer’s Handbook

1.15. Adding a System to an Intel Quartus Prime Project

Platform Designer requires that you to specify an associated Intel Quartus Prime project at time of system creation. After you specify the associated project, Platform Designer automatically adds any system or IP component that you generate to that project. You can also manually add a Platform Designer system or component to a project.

To add a Platform Designer system or component to an Intel Quartus Prime project, perform one or more of the following steps:

1. In Platform Designer, specify the associated Quartus project when you create a system, or click File ➤ Select Quartus Project to change this setting. Platform Designer automatically adds any system or IP component that you generate to the associated Intel Quartus Prime project.

2. To manually add a Platform Designer system or component to your project, generate the system or component, and then click Project ➤ Add/Remove Files in Project in the Intel Quartus Prime software.

3. Select and add the .qsys files to your project. The Intel Quartus Prime Project Navigator Files tab lists all system and component files that you or Platform Designer add to your project.

Figure 51. Platform Designer System Files in Project
1.16. Managing Hierarchical Platform Designer Systems

Platform Designer supports hierarchical systems that include one or more Platform Designer subsystems within another Platform Designer system. Platform Designer allows you to create, explore, and edit systems and subsystems together in the same Platform Designer window. Platform Designer generates the complete system hierarchy during the top-level system’s generation.

All hierarchical Platform Designer systems appear in the IP Catalog under Project ▶ System. You select the system from the IP Catalog to reuse the system across multiple designs. In a team-based hierarchical design flow, you can divide large designs into subsystems and allow team members develop subsystems simultaneously.

Related Information
Viewing the System Hierarchy on page 19

1.16.1. Adding a Subsystem to a Platform Designer System

You can add a Platform Designer system as a subsystem (child) of another Platform Designer system (parent), at any level in the parent system hierarchy.

Follow these steps to add a subsystem to a Platform Designer system:

1. Create a Platform Designer system to use as the subsystem.
2. Open a Platform Designer system to contain the subsystem.
3. On the System View tab, use any of the following methods to add the subsystem:
   • Right-click anywhere in the System View and click Add a new subsystem to the current system.
   • Click the Add a new subsystem to the current system button on the toolbar.
   • Press Ctrl+Shift+N.
4. In the Confirm New System Name dialog box, confirm or specify the new system file name and click OK. The system appears as a new subsystem in the System View.
1.16.2. Viewing and Traversing Subsystem Contents

You can view and traverse the elements and connections within subsystems in a hierarchical Platform Designer system.

**Note:** You can only view and traverse the contents of subsystems that you define in a .qsys file, not parameterizable Platform Designer systems or _hw.tcl files.

Follow these steps to view and traverse subsystem contents:

1. Open a Platform Designer system that contains a subsystem.
2. Use any of the following methods to view the subsystem contents:
3. Use any of the following System View or Schematic tab toolbar buttons to traverse the system and subsystems:

<table>
<thead>
<tr>
<th>Table 25. System View and Schematic Tab Navigation Buttons</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Button</strong></td>
</tr>
<tr>
<td>![button]</td>
</tr>
<tr>
<td>![button]</td>
</tr>
<tr>
<td>![button]</td>
</tr>
</tbody>
</table>

Note: In the System View tab, you can press Ctrl+Shift+U to navigate up one level, and Ctrl+Shift+D to drill into a system.

1.16.3. Editing a Subsystem

You can double-click a Platform Designer subsystem in the Hierarchy tab to edit its contents in any tab. When you make a change, open tabs refresh their content to reflect your edit. You can change the level of a subsystem, or push the system into another subsystem with commands in the System View tab.
You can only edit subsystems that a writable .qsys file preserves. You cannot edit systems that you create from composed _hw.tcl files, or systems that define instance parameters.

Follow these steps to edit a Platform Designer subsystem:

1. Open a Platform Designer system that contains a subsystem.
2. In the System View or Schematic tabs, use the Move Up, Move Down, Move to Top, and Move to Bottom toolbar buttons to navigate the system level you want to edit. Platform Designer updates to reflect your selection.
3. To edit a system, double-click the system in the Hierarchy tab. The system opens and is available for edit in all Platform Designer views.
4. In the System View tab, you can rename any element, add, remove, or duplicate connections, and export interfaces, as appropriate.

Note: Changes to a subsystem affect all instances. Platform Designer identifies unsaved changes to a subsystem with an asterisk next to the subsystem in the Hierarchy tab.

### 1.16.4. Changing a Component’s Hierarchy Level

You can change the hierarchical level of components in your system.

You can lower the hierarchical level of a component, even into its own subsystem, which can simplify the top-level system view. You can also raise the level of a component or subsystem to share the component or subsystem between two unique subsystems. Management of hierarchy levels facilitates system optimization and can reduce complex connectivity in your subsystems.

Follow these steps to change a component’s hierarchy level:

1. Open a Platform Designer system that contains a subsystem.
2. In the System View tab, to group and change the hierarchy level of multiple components that share a system-level component, multi-select the components, right-click, and then click Push down into new subsystem. Platform Designer pushes the components into their own subsystem and re-establishes the exported signals and connectivity in the new location.
3. In the System View tab, to pull a component up out of a subsystem, select the component, and then click Pull up. Platform Designer pulls the component up out of the subsystem and re-establishes the exported signals and connectivity in the new location.

### 1.16.5. Saving a Subsystem

When you save a subsystem as part of a Platform Designer system, Platform Designer confirms the new subsystem name in the Confirm New System Filenames dialog box. By default, Platform Designer suggests the same name as the subsystem .qsys file and saves in the project’s /ip directory.
Follow these steps to save a subsystem:
1. Open a Platform Designer system that contains a subsystem.
2. Click **File ➤ Save** to save your Platform Designer design.
3. In the **Confirm New System Filenames** dialog box, click **OK** to accept the subsystem file names.
   
   *Note:* If you have not yet saved your top-level system, or multiple subsystems, you can type a new name, and then press **Enter**, to move to the next un-named system.
4. In the **Confirm New System Filenames** dialog box, to edit the name of a subsystem, click the subsystem, and then type the new name.

1.17. Saving, Archiving, and Restoring Platform Designer Systems

Platform Designer allows you to save or archive your system. When you archive the system, Platform Designer saves the bundled system in **.zip** format. The **.zip** file preserves all files that you need to restore the system.

**Saving a Platform Designer System**

Follow these steps to save a Platform Designer system:
1. Open a Platform Designer system, as .
2. Use any of the following methods to save Platform Designer system files:
   - To save a Platform Designer system, click **File ➤ Save**.
   - To save the system as a Platform Designer script, click **File ➤ Export System as qsys script (.tcl)**. You can restore this system by executing the **.tcl** script from the **System Scripting** tab.
   - To create a copy of the standalone **.ip** file, click **File ➤ Save As**.

**Archiving and Restoring a Platform Designer System**

Follow these steps to archive and restore a system:
1. In Platform Designer, click **File ➤ Archive System**. The **Archive System** dialog box appears.
2. Specify the **Archive file name**.
3. Enable or disable **Collect to common directory**. When enabled, Platform Designer collects all the **.qsys** files in the root directory of the archive, and all the **.ip** files to a single **ip** directory, while updating all the references to match. Disable this option to maintain the current system directory structure for the archive.
4. Click **OK**. Platform Designer generates the archive.
5. To restore the archived system, click **File ➤ Restore Archive System**. Select the **Archive file name**, and **Destination folder** to extract the restored files.

After restoration is complete, Platform Designer automatically launches the **Open System** dialog box, with the extracted project preloaded.
1.18. Running System Scripts

The **System Scripting** tab allows you to enter, save, and execute Tcl scripts on your Platform Designer system. The tab includes a selection of provided scripts, as well as support for storage and retrieval of your own scripts.

Follow these steps to enter, save, and execute Tcl scripts on your Platform Designer system:

1. To open the **System Scripting** tab, click **View ➤ System Scripting**.

2. For **User Scripts** or **Project Scripts**, click `<<add script>>` to add a new script file to this entry. You can drag items between the **Project Scripts** and **User Scripts** fields.

3. To add additional commands to run before the script, right-click the column header and enable **Additional Commands**. Selecting this option displays a third column, in addition to **File** and **Description**. Double-click the entry in this field to add commands to execute before running your script. Alternatively, you can add the additional commands to your script, directly through the display pane in the middle, in the specified section.

The **System Scripting** tab provides the following fields:
### System Scripting Tab Options

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Platform Designer Built-in Scripts</strong></td>
<td>Lists non-editable scripts that Platform Designer provides.</td>
</tr>
<tr>
<td><strong>User Scripts</strong></td>
<td>You can add your own scripts to this entry. Platform Designer saves these scripts to your user preference file, available in your home directory. The scripts that you add to this entry are available every time you open Platform Designer.</td>
</tr>
<tr>
<td><strong>Project Scripts</strong></td>
<td>You can add your own scripts to this entry. Platform Designer saves these scripts to your current system. The scripts that you add to this entry are available only when you open this specific Platform Designer system.</td>
</tr>
<tr>
<td><strong>Edit File</strong></td>
<td>Selecting the script in the <strong>File</strong> field displays the script in the pane below. Click <strong>Edit File</strong> to edit the script.</td>
</tr>
<tr>
<td><strong>Revert File</strong></td>
<td>Discards all your changes to the edited file.</td>
</tr>
<tr>
<td><strong>Save File</strong></td>
<td>Saves your changes to the edited file.</td>
</tr>
<tr>
<td><strong>Run Script</strong></td>
<td>Executes the selected script.</td>
</tr>
<tr>
<td><strong>System Scripting Messages</strong></td>
<td>Displays the warning and error messages when running the script.</td>
</tr>
</tbody>
</table>

**Related Information**

Platform Designer Command-Line Utilities on page 375
# 1.19. Creating a System with Platform Designer Revision History

The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2020.09.28        | 20.3.0                      | • Removed reference to obsolete Read/Write Waveforms option from "Modifying IP Parameters" topic.  
|                   |                             | • Removed reference to obsolete System Information tab and Implementation Templates tab from "Specifying IP Component Instantiation Options" topic.  
|                   |                             | • Removed reference to obsolete Direction option from "Changing a Conduit to a Reset" topic.  
|                   |                             | • Added details about filter controls to "Filtering the System View" topic. |
| 2020.01.31        | 19.1.0                      | • Removed obsolete "Implementing Performance Monitoring" topic. |
| 2019.10.02        | 19.1.0                      | • Updated location of interconnect parameters security setting in "Configuring Platform Designer System Security" topic. |
| 2019.09.30        | 19.1.0                      | • Removed reference to obsolete Bus Analyzer Toolkit from "Implementing Performance Monitoring" topic. |
| 2019.06.24        | 19.1.0                      | • Removed obsolete Interconnect Type parameter from "Interconnect Parameters" topic. |
| 2019.04.30        | 19.1.0                      | • Corrected typographical error in "Interconnect Parameters" topic. |
| 2019.04.01        | 19.1.0                      | • Described new Domains tab for specifying system-wide or domain-specific interconnect parameters.  
|                   |                             | • Described new default use of synchronous reset option for Intel Stratix 10 designs in "Interconnect Parameters."  
|                   |                             | • Described new Schematic tab in "Previewing the System Interconnect." |
| 2018.12.15        | 18.1.0                      | • Replaced references to System Contents tab with new System View tab.  
|                   |                             | • Described new Filter tab in Filtering the "Filtering the System View."  
|                   |                             | • Updated "Disabling or Enabling Parallel IP Generation" to indicate option is now on by default and describe optional settings.  
|                   |                             | • Moved command-line utility information into new "Platform Designer Command-Line Interface" chapter.  
|                   |                             | • Removed "Creating a Combined Simulation Script" topic that does not apply to Platform Designer.  
|                   |                             | • Revised headings and re-organized content into user task-based sections.  
|                   |                             | • Updated screenshots for latest version. |
| 2018.09.24        | 18.1.0                      | • Removed duplicated topic: Manually Control Pipelining in the Platform Design Interconnect. The topic is now in the Platform Design Interconnect chapter.  
|                   |                             | • Added statement about supported standards for IP-XACT.  
|                   |                             | • Divided topic: Specify Implementation Type for IP Components into Configure the System Representation of an IP Core and Implementation Type.  
|                   |                             | • Reorganized information about associating Intel Quartus Prime projects to Platform Designer systems.  
|                   |                             | • Grouped information regarding definition and management of IP cores in Platform Designer under topic: IP Cores in Platform Designer, and updated contents.  
|                   |                             | • Expanded description of parallel IP generation.  
|                   |                             | • In topic 64-Bit Addressing Support, added link to information about the auto base assignment feature. |

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<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2018.06.15        | 18.0.0                      | • Updated description of Enable ECC protection in table: System-Wide Interconnect Requirements.  
                      • Updated example in topic: Generate a Platform Design System with qsys-script. |
| 2018.05.07        | 18.0.0                      | • Added support for hierarchical simscripts, and the Xcelium Parallel Simulator in .  
                      • Added support for --debug command used with qsys-edit.  
                      • Added support for wire-level expressions and connectivity.  
                      • Added _hw.tcl commands to support wire-level expressions. |
| 2017.11.06        | 17.1.0                      | • Changed instances of Qsys Pro to Platform Designer |
| 2017.05.06        | 17.0.0                      | • Updated the topic - Create/Open Project in Qsys Pro  
                      • Updated the topic - Modify the Target Device  
                      • Updated the topic - Modify the IP Search Path  
                      • Added new topic - Save your System  
                      • Added new topic - Archive your System  
                      • Added new topic - Synchronize IP File References  
                      • Updated the topic - Upgrade Outdated IP Components in Qsys Pro.  
                      • Added new topic - Run System Scripts  
                      • Added new topic - View Avalon Memory Mapped Domains in Your Qsys Pro System  
                      • Updated the topic - Qsys Pro Scripting Command Reference for new Tcl scripting commands  
                      • Updated the topic - Qsys Pro Scripting Property Reference for new Tcl scripting property |
| 2016.10.31        | 16.1.0                      | • Implemented Intel rebranding.  
                      • Implemented Qsys rebranding.  
                      • Integrated Qsys Pro chapter with Qsys.  
                      • Added command-line options for qsys-archive.  
                      • Added command-line options for quartus_ipgenerate.  
                      • Updated the Qsys Pro scripting commands.  
                      • Added topic on Qsys Pro design conversion. |
| 2016.05.03        | 16.0.0                      | • Qsys Command-Line Utilities updated with latest supported command-line options.  
                      • Added: Generate Header Files |
| 2015.11.02        | 15.1.0                      | • Added: Troubleshooting IP or Qsys Pro System Upgrade.  
                      • Added: Generating Version-Agnostic IP and Qsys Pro Simulation Scripts.  
                      • Changed instances of Quartus II to Quartus Prime. |
| 2015.05.04        | 15.0.0                      | • New figure: Avalon Memory Mapped Write Master Timing Waveforms in the Parameters Tab.  
                      • Added Enable ECC protection option, Specify Qsys Interconnect Requirements.  
                      • Added External Memory Interface Debug Toolkit note, Generate a Qsys System.  
                      • Modelsim-Altera now supports native mixed-language (VHDL/Verilog/SystemVerilog) simulation, Generating Files for Synthesis and Simulation. |
| December 2014     | 14.1.0                      | • Create and Manage Hierarchical Qsys Systems.  
                      • Schematic tab.  
                      • View and Filter Clock and Reset Domains.  
                      • File ➤ Recent Projects menu item.  
                      • Updated example: Hierarchical System Using Instance Parameters |

continued...
<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| August 2014      | 14.0a10.0                  | • Added distinction between legacy and standard device generation.  
                          • Updated: Upgrading Outdated IP Components.  
                          • Updated: Generating a Qsys System.  
                          • Updated: Integrating a Qsys System with the Quartus II Software.  
                          • Added screen shot: Displaying Your Qsys System. |
| June 2014        | 14.0.0                     | • Added tab descriptions: Details, Connections.  
                          • Added Managing IP Settings in the Quartus II Software.  
                          • Added Upgrading Outdated IP Components.  
                          • Added Support for Avalon Memory Mapped Non-Power of Two Data Widths. |
| November 2013    | 13.1.0                     | • Added Integrating with the .qsys File.  
                          • Added Using the Hierarchy Tab.  
                          • Added Managing Interconnect Requirements.  
                          • Added Viewing Qsys Interconnect. |
| May 2013         | 13.0.0                     | • Added AMBA APB support.  
                          • Added qsys-generate utility.  
                          • Added VHDL BFM ID support.  
                          • Added Creating Secure Systems (TrustZones).  
                          • Added CMSIS Support for Qsys Systems With An HPS Component.  
                          • Added VHDL language support options. |
| November 2012    | 12.1.0                     | • Added AMBA AXI4 support. |
| June 2012        | 12.0.0                     | • Added AMBA AXI3I support.  
                          • Added Preset Editor updates.  
                          • Added command-line utilities, and scripts. |
| November 2011    | 11.1.0                     | • Added Synopsys VCS and VCS MX Simulation Shell Script.  
                          • Added Cadence Incisive Enterprise (NCSIM) Simulation Shell Script.  
                          • Added Using Instance Parameters and Example Hierarchical System Using Parameters. |
| May 2011         | 11.0.0                     | • Added simulation support in Verilog HDL and VHDL.  
                          • Added testbench generation support.  
                          • Updated simulation and file generation sections. |
| December 2010    | 10.1.0                     | Initial release. |
2. Creating Platform Designer Components

You can create and package IP components for use in a Platform Designer system. You can use a _hw.tcl file to describe IP components, interfaces and HDL files. Platform Designer provides the Component Editor to help you create a simple _hw.tcl file.

Related Information

- Avalon Interface Specifications
- Protocol Specifications
- Demo AXI Memory Example

2.1. Platform Designer Components

A Platform Designer component includes the following elements:

- Information about the component type, such as name, version, and author.
- HDL description of the component’s hardware, including SystemVerilog, Verilog HDL, or VHDL files, or a blackbox implementation.
- A Synopsys* Design Constraints File .sdc that defines the component for synthesis and simulation.
- For _hw.tcl components, an .ip file that defines the component’s parameters.
- A component’s interfaces, including I/O signals.

2.1.1. Platform Designer Interface Support

Platform Designer is most effective when you use standard interfaces available in the IP Catalog to design custom IP. Standard interfaces operate efficiently with Intel FPGA IP components, and you can take advantage of the bus functional models (BFMs), monitors, and other verification IP that the IP Catalog provides.

Platform Designer also supports connections between Avalon and AXI interfaces by generating the interconnect logic. This logic enables you to handle the protocol difference. Platform Designer creates the interconnect logic by converting all the protocols to a proprietary packet format. Then, the tool routes the packet through network switches to the appropriate slaves. Here, the packet converts to the slave’s protocol.

Platform Designer supports the following interface specifications:

- Intel FPGA Avalon Memory-Mapped and Streaming
- Arm AMBA 3 AXI (version 1.0)
- Arm AMBA 4 AXI (version 2.0)
- Arm AMBA 4 AXI-Lite (version 2.0)
- Arm AMBA 4 AXI-Stream (version 1.0)
- Arm AMBA 3 APB (version 1.0)

IP components (IP Cores) can have any number of interfaces in any combination. Each interface represents a set of signals that you can connect within a Platform Designer system, or export outside of a Platform Designer system.

Platform Designer IP components can include the following interface types:

<table>
<thead>
<tr>
<th>Interface Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory-Mapped</td>
<td>Connects memory-referring master devices with slave memory devices. Master devices can be processors and DMAs, while slave memory devices can be RAMs, ROMs, and control registers. Data transfers between Avalon Memory Mapped master and slave may be unidirectional (read only or write only), or bi-directional (read and write).</td>
</tr>
<tr>
<td>Streaming</td>
<td>Connects Avalon Streaming sources and sinks that stream unidirectional data, as well as high-bandwidth, low-latency IP components. Streaming creates datapaths for unidirectional traffic, including multichannel streams, packets, and DSP data. The Avalon interconnect is flexible and can implement on-chip interfaces for industry standard telecommunications and data communications cores, such as Ethernet, Interlaken, and video. You can define bus widths, packets, and error conditions.</td>
</tr>
<tr>
<td>Interrupts</td>
<td>Connects interrupt senders to interrupt receivers. Platform Designer supports individual, single-bit interrupt requests (IRQs). In the event that multiple senders assert their IRQs simultaneously, the receiver logic (typically under software control) determines which IRQ has highest priority, then responds appropriately.</td>
</tr>
<tr>
<td>Clocks</td>
<td>Connects clock output interfaces with clock input interfaces. Clock outputs can fan-out without the use of a bridge. A bridge is required only when a clock from an external (exported) source connects internally to more than one source.</td>
</tr>
<tr>
<td>Resets</td>
<td>Connects reset sources with reset input interfaces. If your system requires a particular positive-edge or negative-edge synchronized reset, Platform Designer inserts a reset controller to create the appropriate reset signal. If you design a system with multiple reset inputs, the reset controller ORs all reset inputs and generates a single reset output.</td>
</tr>
<tr>
<td>Conduits</td>
<td>Connects point-to-point conduit interfaces, or represent signals that you export from the Platform Designer system. Platform Designer uses conduits for component I/O signals that are not part of any supported standard interface. You can connect two conduits directly within a Platform Designer system as a point-to-point connection. Alternatively, you can export conduit interfaces and bring the interfaces to the top-level of the system as top-level system I/O. You can use conduits to connect to external devices, for example external DDR SDRAM memory, and to FPGA logic defined outside of the Platform Designer system.</td>
</tr>
</tbody>
</table>

Related Information
- Avalon Interface Specifications
- AMBA Protocol Specifications

2.1.2. Component Structure

Intel provides components automatically installed with the Intel Quartus Prime software. To obtain a list of all Platform Designer-compliant components available from third-party IP developers, follow these steps:
1. Navigate to the Intel FPGA Find IP web page.

2. In the Find IP search results, click the **Platform Designer (Qsys) Compliant** column filter to show all Platform Designer-compliant components.

3. Further refine the search results by selecting the **End Market**, **Technology**, **Devices**, or **Provider** search filter. The **Provider** filter allows you to select specific third-party IP partners.

Every Platform Designer-compliant component is defined with a `<component_name>_hw.tcl` file. This file is a text file written in the Tcl scripting language that describes the component to Platform Designer. When you design your own custom component, you can create the `_hw.tcl` file manually, or by using the Platform Designer Component Editor.

The Component Editor simplifies the process of creating `_hw.tcl` files by creating a file that you can edit outside of the Component Editor to add advanced procedures. When you edit a previously saved `_hw.tcl` file, Platform Designer automatically backs up the earlier version as `_hw.tcl~`.

You can move component files into a new directory, such as a network location, so that other users can use the component in their systems. The `_hw.tcl` file contains relative paths to the other files, so if you move an `_hw.tcl` file, you should also move all the HDL and other files associated with it.

There are four component types:

- **Static**—static components always generate the same output, regardless of their parameterization. Components that instantiate static components must have only static children.

- **Generated**—generated component's fileset callback allows an instance of the component to create unique HDL design files based on the instance's parameter values.

- **Composed**—composed components are subsystems constructed from instances of other components. You can use a composition callback to manage the subsystem in a composed component.

- **Generic**—generic components allow instantiation of IP components without an HDL implementation. Generic components enable hierarchical isolation between system interconnect and IP components.

**Related Information**

- [Create a Composed Component or Subsystem](#) on page 135
- [Add Component Instances to a Static or Generated Component](#) on page 137

### 2.1.3. Component File Organization

A typical component uses the following directory structure where the names of the directories are not significant:
<component_directory>/

- <hdl>/—Contains the component HDL design files, for example .v, .sv, or .vhd files that contain the top-level module, along with any required constraint files.

- <component_name>_hw.tcl—The component description file.

- <component_name>_sw.tcl—The software driver configuration file. This file specifies the paths for the .c and .h files associated with the component, when required.

- <software>/—Contains software drivers or libraries related to the component.

Note: Refer to the Nios II Software Developer's Handbook for information about writing a device driver or software package suitable for use with the Nios II processor.

Related Information
Nios II Software Developer's Handbook
Refer to the "Nios II Software Build Tools" and "Overview of the Hardware Abstraction Layer" chapters.

2.1.4. Component Versions

Platform Designer systems support multiple versions of the same component within the same system; you can create and maintain multiple versions of the same component.

If you have multiple _hw.tcl files for components with the same NAME module properties and different VERSION module properties, both versions of the component are available.

If multiple versions of the component are available in the IP Catalog, you can add a specific version of a component by right-clicking the component, and then selecting Add version <version_number>.

2.1.4.1. Upgrade IP Components to the Latest Version

When you open a Platform Designer design, if Platform Designer detects IP components that require regeneration, the Upgrade IP Cores dialog box appears and allows you to upgrade outdated components.

Components that you must upgrade in order to successfully compile your design appear in red. Status icons indicate whether a component is currently being regenerated, the component is encrypted, or that there is not enough information to determine the status of component. To upgrade a component, in the Upgrade IP Cores dialog box, select the component that you want to upgrade, and then click Upgrade. The Intel Quartus Prime software maintains a list of all IP components associated with your design on the Components tab in the Project Navigator.

Related Information
Upgrade IP Components Dialog Box
In Intel Quartus Prime Help
2.2. Design Phases of an IP Component

When you define a component with the Platform Designer Component Editor, or a custom _hw.tcl file, you specify the information that Platform Designer requires to instantiate the component in a Platform Designer system and to generate the appropriate output files for synthesis and simulation.

The following phases describe the process when working with components in Platform Designer:

- **Discovery**—During the discovery phase, Platform Designer reads the _hw.tcl file to identify information that appears in the IP Catalog, such as the component’s name, version, and documentation URLs. Each time you open Platform Designer, the tool searches for the following file types using the default search locations and entries in the IP Search Path:
  - _hw.tcl files—Each _hw.tcl file defines a single component.
  - IP Index (.ipx) files—Each .ipx file indexes a collection of available components, or a reference to other directories to search.

- **Static Component Definition**—During the static component definition phase, Platform Designer reads the _hw.tcl file to identify static parameter declarations, interface properties, interface signals, and HDL files that define the component. At this stage of the life cycle, the component interfaces may be only partially defined.

- **Parameterization**—During the parameterization phase, after an instance of the component is added to a Platform Designer system, the user of the component specifies parameters with the component’s parameter editor.

- **Validation**—During the validation phase, Platform Designer validates the values of each instance’s parameters against the allowed ranges specified for each parameter. You can use callback procedures that run during the validation phase to provide validation messages. For example, if there are dependencies between parameters where only certain combinations of values are supported, you can report errors for the unsupported values.

- **Elaboration**—During the elaboration phase, Platform Designer queries the component for its interface information. Elaboration is triggered when an instance of a component is added to a system, when its parameters are changed, or when a system property changes. You can use callback procedures that run during the elaboration phase to dynamically control interfaces, signals, and HDL files based on the values of parameters. For example, interfaces defined with static declarations can be enabled or disabled during elaboration. When elaboration is complete, the component’s interfaces and design logic must be completely defined.

- **Composition**—During the composition phase, a component can manipulate the instances in the component’s subsystem. The _hw.tcl file uses a callback procedure to provide parameterization and connectivity of sub-components.

- **Generation**—During the generation phase, Platform Designer generates synthesis or simulation files for each component in the system into the appropriate output directories, as well as any additional files that support associated tools.
2.3. Creating IP Components in the Component Editor

The Platform Designer Component Editor allows you to create and package an IP component and parameterization GUI. When you use the Component Editor to define a component, Platform Designer writes the information to an _hw.tcl file.

![Component Editor](image)

The Platform Designer Component Editor allows you to perform the following tasks:

- Specify component's identifying information, such as name, version, author, etc.
- Specify the SystemVerilog, Verilog HDL, VHDL files, and constraint files that define the component for synthesis and simulation.
- Create an HDL template to define a component's interfaces, signals, and parameters.
- Set parameters on interfaces and signals that can alter the component's structure or functionality.

If you do not have a top-level HDL component file, you can use the Platform Designer Component Editor to add interfaces, signals, and parameters. In the Component Editor, the order in which the tabs appear reflects the recommended design flow for component development. You can use the Prev and Next buttons to guide you through the tabs.
In a Platform Designer system, the interfaces of a component are connected in the system, or exported as top-level signals from the system.

If the component is not based on an existing HDL file, enter the parameters, signals, and interfaces first, and then return to the **Files** tab to create the top-level HDL file template. When you click **Finish**, Platform Designer creates the component \_hw.tcl file with the details that you enter in the Component Editor.

When you save the component, it appears in the IP Catalog.

If you require custom features that the Platform Designer Component Editor does not support, for example, an elaboration callback, use the Component Editor to create the \_hw.tcl file, and then manually edit the file to complete the component definition.

**Note:** If you add custom coding to a component, do not open the component file in the Platform Designer Component Editor. The Platform Designer Component Editor overwrites your custom edits.

**Example 4. Platform Designer Creates an \_hw.tcl File from Entries in the Component Editor**

```
# connection point clock
add_interface clock clock end
set_interface_property clock clockRate 0
set_interface_property clock ENABLED true
add_interface_port clock clk clk Input 1

# connection point reset
add_interface reset reset end
set_interface_property reset associatedClock clock
set_interface_property reset synchronousEdges DEASSERT
set_interface_property reset ENABLED true
add_interface_port reset reset_n reset_n Input 1

# connection point streaming
add_interface streaming avalon_streaming start
set_interface_property streaming associatedClock clock
set_interface_property streaming associatedReset reset
set_interface_property streaming dataBitsPerSymbol 8
set_interface_property streaming errorDescriptor ""
set_interface_property streaming firstSymbolInHighOrderBits true
set_interface_property streaming maxChannel 0
set_interface_property streaming readyLatency 0
set_interface_property streaming ENABLED true
add_interface_port streaming aso_data data Output 8
add_interface_port streaming aso_valid valid Output 1
add_interface_port streaming aso_ready ready Input 1

# connection point slave
add_interface slave axi end
set_interface_property slave associatedClock clock
set_interface_property slave associatedReset reset
set_interface_property slave readAcceptanceCapability 1
set_interface_property slave writeAcceptanceCapability 1
set_interface_property slave combinedAcceptanceCapability 1
```
set_interface_property slave readDataReorderingDepth 1
set_interface_property slave ENABLED true

add_interface_port slave axs_awid awid Input AXI_ID_W
...
add_interface_port slave axs_rresp rresp Output 2

Related Information
Component Interface Tcl Reference on page 594

2.3.1. Save an IP Component and Create the _hw.tcl File

You save a component by clicking Finish in the Platform Designer Component Editor. The Component Editor saves the component as <component_name>_hw.tcl file.

You can use IP components with other applications, such as the C compiler and a board support package (BSP) generator. Intel recommends that you move _hw.tcl files and their associated files to an ip/ directory within your Intel Quartus Prime project directory. When changing file locations, ensure that the file paths in the _hw.tcl file always point to the HDL code correctly. The Component Editor places the _hw.tcl file in the location of the .qsys file, rather than in the location of the HDL files. There can be a disconnect if you move the files without updating references. Check the ADD_FILESET_FILE property setting in the _hw.tcl.

Refer to Creating a System with Platform Designer for information on how to search for and add components to the IP Catalog for use in your designs.

Related Information
- Creating a System with Platform Designer on page 10
- Publishing Component Information to Embedded Software
  In Nios II Gen 2 Software Developer's Handbook
- Publishing Component Information to Embedded Software (Nios II Software Developer's Handbook)
- Creating a System with Platform Designer on page 10

2.3.2. Edit an IP Component with the Platform Designer Component Editor

In Platform Designer, you make changes to a component by right-clicking the component in the System View tab, and then clicking Edit. After making changes, click Finish to save the changes to the _hw.tcl file.

You can open an _hw.tcl file in a text editor to view the hardware Tcl for the component. If you edit the _hw.tcl file to customize the component with advanced features, you cannot use the Component Editor to make further changes without overwriting your customized file.

You cannot use the Component Editor to edit components installed with the Intel Quartus Prime software, such as Intel-provided components. If you edit the HDL for a component and change the interface to the top-level module, you must edit the component to reflect the changes you make to the HDL.
2.3.3. Specify IP Component Type Information

The **Component Type** tab in the Platform Designer Component Editor allows you to specify the following information about the component:

- **Name**—specifies the \_hw.tcl filename, as well as in the top-level module name when you create a synthesis wrapper file for a non HDL-based component.

- **Display name**—identifies the component in the parameter editor, which you use to configure an instance of the component, and also appears in the IP Catalog under **Project** and on the **System View** tab.

- **Version**—specifies the component version number.

- **Group**—represents the category of the component in the list of available components in the IP Catalog. You can select an existing group from the list, or define a new group by typing a name in the **Group** box. Separating entries in the **Group** box with a slash defines a subcategory. For example, if you type **Memories and Memory Controllers/On-Chip**, the component appears in the IP Catalog under the **On-Chip** group, which is a subcategory of the **Memories and Memory Controllers** group. If you save the component in the project directory, the component appears in the IP Catalog in the group you specified under **Project**. Alternatively, if you save the component in the Intel Quartus Prime installation directory, the component appears in the specified group under **IP Catalog**.

- **Description**—allows you to describe the component. This description appears when the user views the component details.

- **Created By**—specifies the component author name.

- **Icon**—specifies the relative path to an icon file (.gif, .jpg, or .png format) that represents the component and appears as the header in the parameter editor for the component. The default image is the Intel FPGA IP function icon.

- **Documentation**—specifies links to documentation for the component, and appears when you right-click the component in the IP Catalog, and then select **Details**.

  - To specify an Internet file, begin your path with **http://**, for example: http://mydomain.com/datasheets/my_memory_controller.html.

  - To specify a file in the file system, begin your path with **file:///** for Linux, and **file:///** for Windows; for example (Windows): file:///company_server/datasheets my_memory_controller.pdf.
When you use the Component Editor to create a component, it writes this basic component information in the _hw.tcl file. The package require command specifies the Intel Quartus Prime software version that Platform Designer uses to create the _hw.tcl file, and ensures compatibility with this version of the Platform Designer API in future releases.

Example 5. _hw.tcl Created from Entries in the Component Type Tab

The component defines its basic information with various module properties using the set_module_property command. For example, set_module_property NAME specifies the name of the component, while set_module_property VERSION allows you to specify the version of the component. When you apply a version to the _hw.tcl file, it allows the file to behave exactly the same way in future releases of the Intel Quartus Prime software.

```tcl
# request TCL package from ACDS 14.0
package require -exact qsys 14.0

# demo_axi_memory
set_module_property DESCRIPTION \ 
"Demo AXI-3 memory with optional Avalon streaming port"
set_module_property NAME demo_axi_memory
set_module_property VERSION 1.0
set_module_property GROUP "My Components"
set_module_property AUTHOR Altera
set_module_property DISPLAY_NAME "Demo AXI Memory"
```

Related Information

Component Interface Tcl Reference on page 594
2.3.4. Create an HDL File in the Platform Designer Component Editor

If you do not have an HDL file for your component, you can use the Platform Designer Component Editor to define the component signals, interfaces, and parameters of your component, and then create a simple top-level HDL file.

You can then edit the HDL file to add the logic that describes the component’s behavior.

1. In the Platform Designer Component Editor, specify the information about the component in the Signals & Interfaces, and Interfaces, and Parameters tabs.
2. Click the Files tab.
3. Click Create Synthesis File from Signals.
   The Component Editor creates an HDL file from the specified signals, interfaces, and parameters, and the .v file appears in the Synthesis File table.

Related Information
Specify Synthesis and Simulation Files in the Platform Designer Component Editor on page 104

2.3.5. Defining HDL Parameters in _hw.tcl

Platform Designer supports the ability to reconfigure features of parameterized modules, such as data bus width or FIFO depth. Platform Designer creates an HDL wrapper when you perform Generate HDL. By modifying your _hw.tcl files to specify parameter attributes and port properties, you can use Platform Designer to generate reusable RTL.

1. To define an alterable HDL parameter, you must declare the following two attributes for the parameter:
   • set_parameter_property <parameter_name> HDL_PARAMETER true
   • set_parameter_property <parameter_name> AFFECTS_GENERATION false

2. To have parameterized ports created in the instantiation wrapper, you can either set the width expression when adding a port to an interface, or set the width expression in the port property in _hw.tcl:
   • To set the width expression when adding a port:

     add_interface_port <interface> <port> <signal_type> <direction> <width_expression>

   • To set the width expression in the port property:

     set_port_property <port> WIDTHEXPR <width_expression>

3. To create and generate the IP component in Platform Designer editor, click the Open System ➤ IP Variant tab, specify the new IP variant name in the IP Variant field and choose the _hw.tcl file that defines user alterable HDL parameters in the Component type field.
4. Click Generate HDL to generate the IP core. Platform Designer generates a parameterized HDL module for you directly.
To instantiate the IP component in your HDL file, click Generate ➤ Show Instantiation Template in the Platform Designer editor to display an instantiation template in Verilog or VHDL. Now you can instantiate the IP core in your top-level design HDL file with the template code.

Figure 57. Instantiation Template Dialog Box

The following sample contains _hw.tcl to set exportable width values:

**Example 6. Sample _hw.tcl Component with User Alterable Expressions**

```tcl
package require -exact qsys 17.1

set_module_property NAME demo
set_module_property DISPLAY_NAME "Demo"
set_module_property ELABORATION_CALLBACK elaborate

# add exportable hdl parameter RECONFIG_DATA_WIDTH
add_parameter RECONFIG_DATA_WIDTH INTEGER 48
set_parameter_property RECONFIG_DATA_WIDTH AFFECTS_GENERATION false
set_parameter_property RECONFIG_DATA_WIDTH HDL_PARAMETER true

# add exportable hdl parameter RECONFIG_ADDR_WIDTH
add_parameter RECONFIG_ADDR_WIDTH INTEGER 32
set_parameter_property RECONFIG_ADDR_WIDTH AFFECTS_GENERATION false
set_parameter_property RECONFIG_ADDR_WIDTH HDL_PARAMETER true

# add non-exportable hdl parameter
add_parameter l_addr INTEGER 32
set_parameter l_addr HDL_PARAMETER false

# add interface
add_interface conduit end

proc elaborate {} {
    add_interface_port s0 rdata readdata output "reconfig_data_width*2 + l_addr"
    add_interface_port s0 raddr readaddress output [get_parameter_value RECONFIG_ADDR_WIDTH]
    set_port_property raddr WIDTH_EXPR "RECONFIG_ADDR_WIDTH"
}
```
2.3.6. Declaring SystemVerilog Interfaces in _hw.tcl

Platform Designer supports interfaces written in SystemVerilog.

The following example is _hw.tcl for a module with a SystemVerilog interface. The sample code is divided into parts 1 and 2.

Part 1 defines the normal array of parameters, Platform Designer interface, and ports


```tcl
# request TCL package from ACDS 17.1
# package require -exact qsys 17.1

# module ram_ip_sv_ifc_hw
#
set_module_property DESCRIPTION ""
set_module_property NAME ram_ip_sv_ifc_hw
set_module_property VERSION 1.0
set_module_property INTERNAL false
set_module_property OPAQUE_ADDRESS_MAP true
set_module_property AUTHOR ""
set_module_property DISPLAY_NAME ram_ip_hw_with_SV_d0
set_module_property INSTANTIATE_IN_SYSTEM_MODULE true
set_module_property EDITABLE true
set_module_property REPORT_TO_TALKBACK false
set_module_property ALLOW_GREYBOX_GENERATION false
set_module_property REPORT_HIERARCHY false

# Part 1 – Add parameter, platform designer interface and ports
# Adding parameter
add_parameter my_interface_parameter STRING "" "I am an interface parameter"

# Adding platform designer interface clk
add_interface clk clock end
set_interface_property clk clockRate 0
# Adding ports to clk interface
add_interface_port clk clk Input 1

# Adding platform designer interface reset
add_interface reset reset end
set_interface_property reset associatedClock clk
#Adding ports to reset interface
add_interface_port reset reset reset Input 1

# Adding platform designer interface avalon_slave
add_interface avalon_slave avalon end
set_interface_property avalon_slave addressUnits WORDS
# Adding ports to avalon_slave interface
add_interface_port avalon_slave address address Input 10
add_interface_port avalon_slave write write Input 1
add_interface_port avalon_slave readdata readdata Output 32
add_interface_port avalon_slave writedata writedata Input 32
set_interface_property avalon_slave associatedClock clk
set_interface_property avalon_slave associatedReset reset

#Adding ram_ip files
add_fileset synthesis_fileset QUARTUS_SYNTH
set_fileset_property synthesis_fileset TOP_LEVEL ram_ip
add_fileset_file ram_ip.sv SYSTEM_VERILOG PATH ram_ip.sv
```
Part 2 defines the interface name, ports, and parameters of the SystemVerilog interface.

**Example 8. Example Part 2: SystemVerilog Interface Parameters in _hw.tcl**

```tcl
# Part 2 – Adding SV interface and its properties.
# Adding SV interface
add_sv_interface bus mem_ifc

# Setting the parameter property to add SV interface parameters
set_parameter_property my_interface_parameter SV_INTERFACE_PARAMETER bus

# Setting the port properties to add them to SV interface port
set_port_property clk SV_INTERFACE_PORT bus
set_port_property reset SV_INTERFACE_PORT bus

# Setting the port properties to add them as signals inside SV interface
set_port_property address SV_INTERFACE_SIGNAL bus
set_port_property write SV_INTERFACE_SIGNAL bus
set_port_property writedata SV_INTERFACE_SIGNAL bus
set_port_property readdata SV_INTERFACE_SIGNAL bus

# Adding the SV Interface File
add_fileset_file mem_ifc.sv SYSTEM_VERILOG PATH mem_ifc.sv SYSTEMVERILOG_INTERFACE
```

**Related Information**

- SystemVerilog Interface Commands on page 681

### 2.3.7. Create an HDL File Using a Template in the Platform Designer Component Editor

You can use a template to create interfaces and signals for your Platform Designer component.

1. In Platform Designer, click **New Component** in the IP Catalog.
2. On the **Component Type** tab, define your component information in the **Name**, **Display Name**, **Version**, **Group**, **Description**, **Created by**, **Icon**, and **Documentation** boxes.
3. Click **Finish**.
   Your new component appears in the IP Catalog under the category that you define for "Group".
4. In Platform Designer, right-click your new component in the IP Catalog, and then click **Edit**.
5. In the Platform Designer Component Editor, click any interface from the Templates drop-down menu.
   The Component Editor fills the **Signals** and **Interfaces** tabs with the component interface template details.
6. On the **Files** tab, click **Create Synthesis File from Signals**.
7. Do the following in the **Create HDL Template** dialog box as shown below:
   a. Verify that the correct files appears in **File** path, or browse to the location where you want to save your file.
   b. Select the HDL language.
   c. Click **Save** to save your new interface, or **Cancel** to discard the new interface definition.
Create HDL Template Dialog Box

8. Verify the `<component_name>.v` file appears in the Synthesis Files table on the Files tab.

**Related Information**

Specify Synthesis and Simulation Files in the Platform Designer Component Editor on page 104

### 2.3.8. Specify Synthesis and Simulation Files in the Platform Designer Component Editor

The Files tab in the Platform Designer Component Editor allows you to specify synthesis and simulation files for your custom component.

If you already have an HDL file that describes the behavior and structure of your component, you can specify those files on the Files tab.

If you do not yet have an HDL file, you can specify the signals, interfaces, and parameters of the component in the Component Editor, and then use the **Create Synthesis File from Signals** option on the Files tab to create the top-level HDL file. The Component Editor generates the `_hw.tcl` commands to specify the files.

**Note:** After you analyze the component's top-level HDL file (on the Files tab), you cannot add or remove signals or change the signal names on the Signals & Interfaces tab. If you need to edit signals, edit your HDL source, and then click **Create Synthesis File from Signals** on the Files tab to integrate your changes.
A component uses filesets to specify the different sets of files that you can generate for an instance of the component. The supported fileset types are: QUARTUS_SYNTH, for synthesis and compilation in the Intel Quartus Prime software, SIM_VERILOG, for Verilog HDL simulation, and SIM_VHDL, for VHDL simulation.

In an _hw.tcl file, you can add a fileset with the add_fileset command. You can then list specific files with the add_fileset_file command. The add_fileset_property command allows you to add properties such as TOP_LEVEL.

You can populate a fileset with a fixed list of files, add different files based on a parameter value, or even generate an HDL file with a custom HDL generator function outside of the _hw.tcl file.

**Related Information**
- Create an HDL File in the Platform Designer Component Editor on page 100
- Create an HDL File Using a Template in the Platform Designer Component Editor on page 103

2.3.8.1. Specify HDL Files for Synthesis in the Platform Designer Component Editor

In the Platform Designer Component Editor, you can add HDL files and other support files with options on the Files tab.

**Figure 58. Using HDL Files to Define a Component**

A component must specify an HDL file as the top-level file. The top-level HDL file contains the top-level module. The **Synthesis Files** list may also include supporting HDL files, such as timing constraints, or other files required to successfully synthesize and compile in the Intel Quartus Prime software. The synthesis files for a component are copied to the generation output directory during Platform Designer system generation.
2.3.8.2. Analyze Synthesis Files in the Platform Designer Component Editor

After you specify the top-level HDL file in the Platform Designer Component Editor, click **Analyze Synthesis Files** to analyze the parameters and signals in the top-level, and then select the top-level module from the **Top Level Module** list. If there is a single module or entity in the HDL file, Platform Designer automatically populates the **Top-level Module** list.

Once analysis is complete and the top-level module is selected, you can view the parameters and signals on the **Parameters** and **Signals & Interfaces** tabs. The Component Editor may report errors or warnings at this stage, because the signals and interfaces are not yet fully defined.

**Note:** At this stage in the Component Editor flow, you cannot add or remove parameters or signals created from a specified HDL file without editing the HDL file itself.

The synthesis files are added to a fileset with the name QUARTUS_SYNTH and type QUARTUS_SYNTH in the _hw.tcl file created by the Component Editor. The top-level module is used to specify the TOP_LEVEL fileset property. Each synthesis file is individually added to the fileset. If the source files are saved in a different directory from the working directory where the _hw.tcl is located, you can use standard fixed or relative path notation to identify the file location for the PATH variable.

**Example 9. _hw.tcl Created from Entries in the Files tab in the Synthesis Files Section**

```tcl
# file sets
add_fileset QUARTUS_SYNTH QUARTUS_SYNTH "" ""
set_fileset_property QUARTUS_SYNTH TOP_LEVEL demo_axi_memory
add_fileset_file demo_axi_memory.sv SYSTEM_VERILOG PATH demo_axi_memory.sv
add_fileset_file single_clk_ram.v VERILOG PATH single_clk_ram.v
```

**Related Information**

- Specify HDL Files for Synthesis in the Platform Designer Component Editor on page 105
- Component Interface Tcl Reference on page 594

2.3.8.3. Name HDL Signals for Automatic Interface and Type Recognition in the Platform Designer Component Editor

If you create the component's top-level HDL file before using the Component Editor, the Component Editor recognizes the interface and signal types based on the signal names in the source HDL file. This auto-recognition feature eliminates the task of manually assigning each interface and signal type in the Component Editor.

To enable auto-recognition, you must create signal names using the following naming convention:

```tcl
<interface type prefix>_<interface name>_<signal type>
```

Specifying an interface name with `<interface name>` is optional if you have only one interface of each type in the component definition. For interfaces with only one signal, such as clock and reset inputs, the `<interface type prefix>` is also optional.
### Table 28. Interface Type Prefixes for Automatic Signal Recognition

When the Component Editor recognizes a valid prefix and signal type for a signal, it automatically assigns an interface and signal type to the signal based on the naming convention. If no interface name is specified for a signal, you can choose an interface name on the **Signals & Interfaces** tab in the Component Editor.

<table>
<thead>
<tr>
<th>Interface Prefix</th>
<th>Interface Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>asi</td>
<td>Avalon Streaming sink (input)</td>
</tr>
<tr>
<td>aso</td>
<td>Avalon Streaming source (output)</td>
</tr>
<tr>
<td>avm</td>
<td>Avalon memory-mapped master</td>
</tr>
<tr>
<td>avs</td>
<td>Avalon memory-mapped slave</td>
</tr>
<tr>
<td>axm</td>
<td>AXI master</td>
</tr>
<tr>
<td>axs</td>
<td>AXI slave</td>
</tr>
<tr>
<td>apm</td>
<td>APB master</td>
</tr>
<tr>
<td>aps</td>
<td>APB slave</td>
</tr>
<tr>
<td>coe</td>
<td>Conduit</td>
</tr>
<tr>
<td>csi</td>
<td>Clock Sink (input)</td>
</tr>
<tr>
<td>cso</td>
<td>Clock Source (output)</td>
</tr>
<tr>
<td>inr</td>
<td>Interrupt receiver</td>
</tr>
<tr>
<td>ins</td>
<td>Interrupt sender</td>
</tr>
<tr>
<td>ncm</td>
<td>Nios II custom instruction master</td>
</tr>
<tr>
<td>ncs</td>
<td>Nios II custom instruction slave</td>
</tr>
<tr>
<td>rsi</td>
<td>Reset sink (input)</td>
</tr>
<tr>
<td>rso</td>
<td>Reset source (output)</td>
</tr>
<tr>
<td>tcm</td>
<td>Avalon TC master</td>
</tr>
<tr>
<td>tcs</td>
<td>Avalon TC slave</td>
</tr>
</tbody>
</table>

Refer to the *Avalon Interface Specifications* or the *AMBA Protocol Specification* for the signal types available for each interface type.

#### Related Information
- Avalon Interface Specifications
- Protocol Specifications

### 2.3.8.4. Specify Files for Simulation in the Component Editor

To support Platform Designer system generation for your custom component, you must specify VHDL or Verilog simulation files.

You can choose to generate Verilog or VHDL simulation files. In most cases, these files are the same as the synthesis files. If there are simulation-specific HDL files or simulation models, you can use them in addition to, or in place of the synthesis files. To use your synthesis files as your simulation files, click **Copy From Synthesis Files** on the **Files** tab in the Platform Designer Component Editor.
Note: The order that you add files to the fileset determines the order of compilation. For VHDL filesets with VHDL files, you must add the files bottom-up, adding the top-level file last.

Figure 59. Specifying the Simulation Output Files on the Files Tab

You specify the simulation files in a similar way as the synthesis files with the fileset commands in a _hw.tcl file. The code example below shows SIM_VERILOG and SIM_VHDL filesets for Verilog and VHDL simulation output files. In this example, the same Verilog files are used for both Verilog and VHDL outputs, and there is one additional SystemVerilog file added. This method works for designers of Verilog IP to support users who want to generate a VHDL top-level simulation file when they have a mixed-language simulation tool and license that can read the Verilog output for the component.

Example 10. _hw.tcl Created from Entries in the Files tab in the Simulation Files Section

```
add_fileset SIM_VERILOG SIM_VERILOG "" ""
set_fileset_property SIM_VERILOG TOP_LEVEL demo_axi_memory
add_fileset_file single_clk_ram.v VERILOG PATH single_clk_ram.v

add_fileset_file verbosity_pkg.sv SYSTEM_VERILOG PATH \verification_lib/verbosity_pkg.sv

add_fileset_file demo_axi_memory.sv SYSTEM_VERILOG PATH \demo_axi_memory.sv

add_fileset SIM_VHDL SIM_VHDL "" ""
set_fileset_property SIM_VHDL TOP_LEVEL demo_axi_memory
set_fileset_property SIM_VHDL ENABLE_RELATIVE_INCLUDE_PATHS false
add_fileset_file demo_axi_memory.sv SYSTEM_VERILOG PATH \demo_axi_memory.sv

add_fileset_file single_clk_ram.v VERILOG PATH single_clk_ram.v
add_fileset_file verbosity_pkg.sv SYSTEM_VERILOG PATH \verification_lib/verbosity_pkg.sv
```

Related Information
Component Interface Tcl Reference on page 594

2.3.8.5. Include an Internal Register Map Description in the .svd for Slave Interfaces Connected to an HPS Component

Platform Designer supports the ability for IP component designers to specify register map information on their slave interfaces. This allows components with slave interfaces that are connected to an HPS component to include their internal register description in the generated .svd file.
To specify their internal register map, the IP component designer must write and generate their own .svd file and attach it to the slave interface using the following command:

```
set_interface_property <slave interface> CMSIS_SVD_FILE <file path>
```

The CMSIS_SVD_VARIABLES interface property allows for variable substitution inside the .svd file. You can dynamically modify the character data of the .svd file by using the CMSIS_SVD_VARIABLES property.

**Example 11. Setting the CMSIS_SVD_VARIABLES Interface Property**

For example, if you set the CMSIS_SVD_VARIABLES in the _hw tcl file, then in the .svd file if there is a variable `{width}` that describes the element `<size>${width}</size>`, it is replaced by `<size>23</size>` during generation of the .svd file. Note that substitution works only within character data (the data enclosed by `<element>...</element>`) and not on element attributes.

```
set_interface_property <interface name> \
CMSIS_SVD_VARIABLES "\n{width} {23}"
```

**Related Information**
- Component Interface Tcl Reference on page 594
- CMSIS - Cortex Microcontroller Software

### 2.3.9. Add Signals and Interfaces in the Platform Designer Component Editor

In the Platform Designer Component Editor, the **Signals & Interfaces** tab allows you to add signals and interfaces for your custom IP component.

As you select interfaces and associated signals, you can customize the parameters. Messages appear as you add interfaces and signals to guide you when customizing the component. In the parameter editor, a block diagram displays for each interface. Some interfaces display waveforms to show the timing of the interface. If you update timing parameters, the waveforms update automatically.

1. In Platform Designer, click **New Component** in the IP Catalog.
2. In the Platform Designer Component Editor, click the **Signals & Interfaces** tab.
3. To add an interface, click `<<add interface>>` in the left pane.
   A drop-down list appears where you select the interface type.
4. Select an interface from the drop-down list.
   The selected interface appears in the parameter editor where you can specify its parameters.
5. To add signals for the selected interface click `<<add signal>>` below the selected interface.
6. To move signals between interfaces, select the signal, and then drag it to another interface.
7. To rename a signal or interface, select the element, and then press F2.
8. To remove a signal or interface, right-click the element, and then click **Remove**.
Alternatively, to remove an signal or interface, you can select the element, and then press **Delete**. When you remove an interface, Platform Designer also removes all of its associated signals.

**Figure 60. Platform Designer Signals & Interfaces tab**

![Platform Designer Signals & Interfaces tab](image)

### 2.3.10. Specify Parameters in the Platform Designer Component Editor

Components can include parameterized HDL, which allow users of the component flexibility in meeting their system requirements. For example, a component with a configurable memory size or data width, allows using one HDL implementation in different systems, each with unique parameters values.

The **Parameters** tab allows you specify the parameters that are used to configure instances of the component in a Platform Designer system. You can specify various properties for each parameter that describe how to display and use the parameter. You can also specify a range of allowed values that are checked during the validation phase. The **Parameters** table displays the HDL parameters that are declared in the top-level HDL module. If you have not yet created the top-level HDL file, the top-level synthesis file template created from the **Files** tab include the parameters that you create on the **Parameters** tab.

When the component includes HDL files, the parameters match those defined in the top-level module, and you cannot add or remove them on the **Parameters** tab. To add or remove the parameters, edit your HDL source, and then re-analyze the file.

If you create a top-level template HDL file for synthesis with the Component Editor, you can remove the newly-created file from the **Synthesis Files** list on the **Files** tab, make your parameter changes, and then re-analyze the top-level synthesis file.
You can use the **Parameters** table to specify the following information about each parameter:

- **Name**—specifies the parameter name.
- **Default Value**—sets the default value for new instances of the component.
- **Editable**—specifies if the user can edit the parameter value.
- **Type**—defines the parameter type as string, integer, boolean, std_logic, logic vector, natural, or positive.
- **Group**—groups parameters in the parameter editor.
- **Tooltip**—adds a description of the parameter that appears when the user of the component points to the parameter in the editor.

**Figure 61. Parameters Tab in the Platform Designer Components Editor**

On the **Parameters** tab, you can click **Preview the GUI** at any time to see how the declared parameters appear in the parameter editor. Parameters with their default values appear with checks in the **Editable** column. Editable parameters cannot contain computed expressions. You can group parameters under a common heading or section in the editor with the **Group** column, and a tooltip helps users of the component understand the function of the parameter. Various parameter properties allow you to customize the component’s parameter editor, such as specifying parameter option controls, or displaying an image.

**Example 12. _hw.tcl Created from Entries in the Parameters Tab**

In this example, the first `add_parameter` command includes commonly-specified properties. The `set_parameter_property` command specifies each property individually. The **Tooltip** column on the **Parameters** tab maps to the **DESCRIPTION** property, and there is an additional unused **UNITS** property created in the code. The **HDL_PARAMETER** property specifies that the value of the parameter is specified in the HDL instance wrapper when creating instances of the component. The **Group** column in the **Parameters** tab maps to the display items section with the `add_display_item` commands. If you want to expose the HDL parameter so that you can overwrite the value when you instantiate the module, set **AFFECTS_GENERATION** to false.
Note: If a parameter \(<n>\) defines the width of a signal, the signal width must follow the format \(<n-1> : 0\).

```plaintext
# parameters
#
add_parameter AXI_ID_W INTEGER 4 "Width of ID fields"
set_parameter_property AXI_ID_W DEFAULT_VALUE 4
set_parameter_property AXI_ID_W DISPLAY_NAME AXI_ID_W
set_parameter_property AXI_ID_W TYPE INTEGER
set_parameter_property AXI_ID_W UNITS None
set_parameter_property AXI_ID_W DESCRIPTION "Width of ID fields"
set_parameter_property AXI_ID_W HDL_PARAMETER true
add_parameter AXI_ADDRESS_W INTEGER 12
set_parameter_property AXI_ADDRESS_W DEFAULT_VALUE 12
add_parameter AXI_DATA_W INTEGER 32
...
# display items
#
add_display_item "AXI Port Widths" AXI_ID_W PARAMETER ""
```

Note: If an AXI slave's ID bit width is smaller than required for your system, the AXI slave response may not reach all AXI masters. The formula of an AXI slave ID bit width is calculated as follows:

```
maximum_master_id_width_in_the_interconnect + log2
(number_of_masters_in_the_same_interconnect)
```

For example, if an AXI slave connects to three AXI masters and the maximum AXI master ID length of the three masters is 5 bits, then the AXI slave ID is 7 bits, and is calculated as follows:

```
5 bits + 2 bits \(\log_2(3\)\ masters)\) = 7
```

Platform Designer refers to AXI interface parameters to build AXI interconnect. If these parameter settings are incompatible with the component's HDL behavior, Platform Designer interconnect and transactions may not work correctly. To prevent unexpected interconnect behavior, you must set the AXI component parameters.

Table 29.  AXI Master Parameters

<table>
<thead>
<tr>
<th>AXI Master Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>readIssuingCapability</td>
<td>The maximum number of outstanding read transactions for a master.</td>
</tr>
<tr>
<td>writeIssuingCapability</td>
<td>The maximum number of outstanding write transactions for a master.</td>
</tr>
<tr>
<td>combinedIssuingCapability</td>
<td>The maximum number of outstanding transactions for a master.</td>
</tr>
</tbody>
</table>
Table 30.  AXI Slave Parameters

<table>
<thead>
<tr>
<th>AXI Slave Parameters</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>readAcceptanceCapability</td>
<td>The maximum number of outstanding read commands that a slave can accept.</td>
</tr>
<tr>
<td>writeAcceptanceCapability</td>
<td>The maximum number of outstanding write transactions that a slave can accept.</td>
</tr>
<tr>
<td>combinedAcceptanceCapability</td>
<td>The maximum number of outstanding transactions that a slave can accept.</td>
</tr>
<tr>
<td>readDataReorderingDepth</td>
<td>The number of outstanding read transactions for which a slave interface can transmit data. If readDataReorderingDepth = 1, the slave processes all transactions in order.</td>
</tr>
</tbody>
</table>

Related Information
Component Interface Tcl Reference on page 594

2.3.10.1. Valid Ranges for Parameters in the _hw.tcl File

In the _hw.tcl file, you can specify valid ranges for parameters.

Platform Designer validation checks each parameter value against the ALLOWED_RANGES property. If the values specified are outside of the allowed ranges, Platform Designer displays an error message. Specifying choices for the allowed values enables users of the component to choose the parameter value from controls in the parameter editor GUI, instead of entering a value.

The ALLOWED_RANGES property is a list of valid ranges, where each range is a single value, or a range of values defined by a start and end value.

Table 31.  ALLOWED_RANGES Property

<table>
<thead>
<tr>
<th>ALLOWED_RANGES Property</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>{a b c}</td>
<td>a, b, or c</td>
</tr>
<tr>
<td>{&quot;No Control&quot; &quot;Single Control&quot; &quot;Dual Controls&quot;}</td>
<td>Unique string values. Quotation marks are required if the strings include spaces.</td>
</tr>
<tr>
<td>{1 2 4 8 16}</td>
<td>1, 2, 4, 8, or 16</td>
</tr>
<tr>
<td>{1:3}</td>
<td>1 through 3, inclusive.</td>
</tr>
<tr>
<td>{1 2 3 7:10}</td>
<td>1, 2, 3, or 7 through 10 inclusive.</td>
</tr>
</tbody>
</table>

Related Information
Declare Parameters with Custom _hw.tcl Commands on page 115

2.3.10.2. Types of Platform Designer Parameters

Platform Designer uses the following parameter types: user parameters, system information parameters, and derived parameters.

Platform Designer User Parameters on page 114
Platform Designer System Information Parameters on page 114
Platform Designer Derived Parameters on page 115
2.3.10.2.1. Platform Designer User Parameters

User parameters are parameters that users of a component can control, and appear in the parameter editor for instances of the component. User parameters map directly to parameters in the component HDL. For user parameter code examples, such as AXI_DATA_W and ENABLE_STREAM_OUTPUT, refer to Declaring Parameters with Custom hw.tcl Commands.

2.3.10.2.2. Platform Designer System Information Parameters

A SYSTEM_INFO parameter is a parameter whose value is set automatically by the Platform Designer system. When you define a SYSTEM_INFO parameter, you provide an information type, and additional arguments.

For example, you can configure a parameter to store the clock frequency driving a clock input for your component. To do this, define the parameter as SYSTEM_INFO of type CLOCK_RATE:

```
set_parameter_property <param> SYSTEM_INFO CLOCK_RATE
```

You then set the name of the clock interface as the SYSTEM_INFO argument:

```
set_parameter_property <param> SYSTEM_INFO_ARG <clkname>
```

Obtaining Device Trait Information Using PART_TRAIT System Information Parameter

Within Platform Designer, an IP core can obtain information on the particular traits of a device using the PART_TRAIT system info parameter. This system info parameter takes an argument corresponding to the desired part trait. The requested trait must match the trait name as specified in the device database.

**Note:** Using this API declares your IP core as dependent on the requested trait.

To get the part number setting of Platform Designer system, use the value DEVICE, with the SYSTEM_INFO_ARG parameter property:

```
add_parameter part_trait_device string ""
set_parameter_property part_trait_device SYSTEM_INFO_TYPE PART_TRAIT
set_parameter_property part_trait_device SYSTEM_INFO_ARG DEVICE
```

To get the base device of the part number setting of Platform Designer system, use the value BASE_DEVICE, with the SYSTEM_INFO_ARG parameter property:

```
add_parameter part_trait_bd string ""
set_parameter_property part_trait_bd SYSTEM_INFO_TYPE PART_TRAIT
set_parameter_property part_trait_bd SYSTEM_INFO_ARG BASE_DEVICE
```

To get the device speed-grade of the part number setting of Platform Designer system, use the value DEVICE_SPEEDGRADE, with the SYSTEM_INFO_ARG parameter property:

```
add_parameter part_trait_sg string ""
set_parameter_property part_trait_sg SYSTEM_INFO_TYPE PART_TRAIT
set_parameter_property part_trait_sg SYSTEM_INFO_ARG DEVICE_SPEEDGRADE
```
2.3.10.2.3. Platform Designer Derived Parameters

Derived parameter values are calculated from other parameters during the Elaboration phase, and are specified in the **hw.tcl** file with the **DERIVED** property. Derived parameter values are calculated from other parameters during the Elaboration phase, and are specified in the **hw.tcl** file with the **DERIVED** property. For example, you can derive a clock period parameter from a data rate parameter. Derived parameters are sometimes used to perform operations that are difficult to perform in HDL, such as using logarithmic functions to determine the number of address bits that a component requires.

**Related Information**

Declare Parameters with Custom _hw.tcl Commands on page 115

Parameterized Parameter Widths

Platform Designer allows a `std_logic_vector` parameter to have a width that is defined by another parameter, similar to derived parameters. The width can be a constant or the name of another parameter.

2.3.10.3. Declare Parameters with Custom _hw.tcl Commands

The example below illustrates a custom _hw.tcl file, with more advanced parameter commands than those generated when you specify parameters in the Component Editor. Commands include the ALLOWED_RANGES property to provide a range of values for the `AXI_ADDRESS_W` (*Address Width*) parameter, and a list of parameter values for the `AXI_DATA_W` (*Data Width*) parameter. This example also shows the parameter `AXI_NUMBYTES` (*Data width in bytes*) parameter; that uses the DERIVED property. In addition, these commands illustrate the use of the GROUP property, which groups some parameters under a heading in the parameter editor GUI. You use the ENABLE_STREAM_OUTPUT_GROUP (*Include Avalon streaming source port*) parameter to enable or disable the optional Avalon Streaming interface in this design, and is displayed as a check box in the parameter editor GUI because the parameter is of type BOOLEAN. Refer to figure below to see the parameter editor GUI resulting from these **hw.tcl** commands.

**Example 13. Parameter Declaration**

In this example, the `AXI_NUMBYTES` parameter is derived during the Elaboration phase based on another parameter, instead of being assigned to a specific value. `AXI_NUMBYTES` describes the number of bytes in a word of data. Platform Designer calculates the `AXI_NUMBYTES` parameter from the `DATA_WIDTH` parameter by dividing by 8. The _hw.tcl code defines the `AXI_NUMBYTES` parameter as a derived parameter, since its value is calculated in an elaboration callback procedure. The `AXI_NUMBYTES` parameter value is not editable, because its value is based on another parameter value.

```
add_parameter AXI_ADDRESS_W INTEGER 12
set_parameter_property AXI_ADDRESS_W DISPLAY_NAME \
"AXI Slave Address Width"
set_parameter_property AXI_ADDRESS_W DESCRIPTION \
"Address width."
set_parameter_property AXI_ADDRESS_W UNITS bits
set_parameter_property AXI_ADDRESS_W ALLOWED_RANGES 4:16
```
set_parameter_property AXI_ADDRESS_W HDL_PARAMETER true
"AXI Port Widths"

add_parameter AXI_DATA_W INTEGER 32
set_parameter_property AXI_DATA_W DISPLAY_NAME "Data Width"
set_parameter_property AXI_DATA_W DESCRIPTION "Width of data buses."
set_parameter_property AXI_DATA_W UNITS bits
set_parameter_property AXI_DATA_W ALLOWED_RANGES {8 16 32 64 128 256 512 1024}
set_parameter_property AXI_DATA_W HDL_PARAMETER true
set_parameter_property AXI_DATA_W GROUP "AXI Port Widths"

add_parameter AXI_NUMBYTES INTEGER 4
set_parameter_property AXI_NUMBYTES DERIVED true
set_parameter_property AXI_NUMBYTES DISPLAY_NAME "Data Width in bytes; Data Width/8"
set_parameter_property AXI_NUMBYTES DESCRIPTION "Number of bytes in one word"
set_parameter_property AXI_NUMBYTES UNITS bytes
set_parameter_property AXI_NUMBYTES HDL_PARAMETER true
set_parameter_property AXI_NUMBYTES GROUP "AXI Port Widths"

add_parameter ENABLE_STREAM_OUTPUT BOOLEAN true
set_parameter_property ENABLE_STREAM_OUTPUT DISPLAY_NAME "Include Avalon Streaming Source Port"
set_parameter_property ENABLE_STREAM_OUTPUT DESCRIPTION "Include optional Avalon streaming source (default), or hide the interface"
set_parameter_property ENABLE_STREAM_OUTPUT GROUP "Streaming Port Control"
...

Figure 62. Resulting Parameter Editor GUI from Parameter Declarations

Related Information
- Control Interfaces Dynamically with an Elaboration Callback on page 133
- Component Interface Tcl Reference on page 594
2.3.10.4. Validate Parameter Values with a Validation Callback

You can use a validation callback procedure to validate parameter values with more complex validation operations than the ALLOWED_RANGES property allows. You define a validation callback by setting the VALIDATION_CALLBACK module property to the name of the Tcl callback procedure that runs during the validation phase. In the validation callback procedure, the current parameter values is queried, and warnings or errors are reported about the component's configuration.

Example 14. Demo AXI Memory Example

If the optional Avalon streaming interface is enabled, then the control registers must be wide enough to hold an AXI RAM address, so the designer can add an error message to ensure that the user enters allowable parameter values.

```tcl
set_module_property VALIDATION_CALLBACK validate
proc validate {} {
    if {
        [get_parameter_value ENABLE_STREAM_OUTPUT] &&
        ([get_parameter_value AXI_ADDRESS_W] >
         [get_parameter_value AV_DATA_W])
    } send_message error "If the optional Avalon streaming port is enabled, the AXI Data Width must be equal to or greater than the Avalon control port Address Width"
}
```

Related Information

- Component Interface Tcl Reference on page 594
- Demo AXI Memory Example
2.4. Adding Generic Components to a System

Platform Designer allows you to add generic components with the implementation defined in \_hw.tcl (IP type), in an HDL file (HDL type), in high level synthesis files (HLS type), or with only a partially defined implementation (Blackbox type). The generic component enables hierarchical isolation of the IP components by separating the component instantiation from the component implementation. This generic component is available as Generic Component in the Platform Designer IP Catalog.

When you generate a system containing a generic component, the system's RTL instantiates the component, but does not provide the implementation for the component. Rather, you must provide the implementation for the component in a downstream compiler such as Intel Quartus Prime software or in RTL code.

The following generic component Implementation Types are available in the Component Instantiation editor, depending on your use case:

<table>
<thead>
<tr>
<th>Implementation Type</th>
<th>Description</th>
</tr>
</thead>
</table>
| IP                  | The default implementation type that defines the component in \_hw.tcl and preserves the component as a .ip file. Platform Designer automatically manages components with the Implementation Type of IP in the following ways:  
  - Runs background checks against the port widths between the IP component and the .ip file to ensure continuity.  
  - Scans the .ip file for the error flag to determine if any component has parameterization errors.  
  - Checks for system-info mismatches between the IP file and the IP component in the system, and prompts resolution with IP instantiation warnings in the Instantiation Messages tab. |
| HDL                 | Defines a generic component from existing RTL. You can load the signals, interfaces, and parameters of the generic component from the HDL file containing the RTL. The HDL parameters are represented as constants local to a module, which you can redefine when instantiating the module. Generic HDL components have no .ip file. |
| Blackbox            | Defines a generic component that represents only the signal and interface boundary of an entity, without providing the component's implementation. You then provide the implementation of the component for processing with the Intel Quartus Prime software or an RTL simulator. Generic blackbox components have no .ip file. |
| HLS                 | Defines a generic component from existing high level synthesis (HLS) files. You compile the HLS file, import a previously compiled HLS file, perform verification on an HLS project, or display the resulting compilation report. Available only on Windows* edition. |

1. From the Platform Designer IP Catalog, double-click Generic Component. The Component Instantiation editor appears.
2. For Implementation Type, click IP, HDL, Blackbox, or HLS for your generic component. Refer to Table 32 on page 118.
3. Add parameters to the generic component, as applicable:
   - To add parameters to a generic HDL component, click the Add File button under Implementation Files to specify the RTL that defines your generic component, as Adding Generic HDL Component Parameters on page 120 describes.
   - To add parameters to a generic Blackbox component, click the Parameters tab, and then Add Parameter button to define the parameters for your generic component, as Adding Generic Blackbox Component Parameters on page 121 describes.
4. Add interfaces and signals to the generic component, as Adding Generic Component Interfaces and Signals on page 122.

5. Click Finish, the generic component appears in the System View.

6. In the System View, select the generic component that you create in step 5.

Figure 64. New Generic Component in System View
7. In the **System View** tab, double-click the **Export** column to export the signal(s) when you generate the system HDL.

8. In the **Parameters** tab for the component, modify the default parameter values as needed.

9. In Platform Designer, click the **Generate HDL** button. Platform Designer generates the HDL for the system and generic component according to your specifications.

### 2.4.1. Adding Generic HDL Component Parameters

You can specify and modify HDL parameters for generic components that have an HDL implementation. This technique allows you to reuse the HDL component in another context with different parameter values. Platform Designer analyzes the HDL implementation, identifies the HDL parameters present, and loads the HDL parameters into the **Component Instantiation** editor where you can modify them. To add parameters in HDL mode, follow these steps:

**Figure 65. HDL Implementation Type in Component Instantiation Editor**

![HDL Implementation Type in Component Instantiation Editor](image)
1. Add a generic HDL component, as Adding Generic Components to a System on page 118 describes.

2. In the Component Instantiation editor Files tab, click the Add File button to select the HDL file that contains the component definition.

3. Under Implementation Files, select the HDL file, and then click Analyze HDL files. The signals and interfaces found in the HDL component appear in the Signals & Interfaces tab. The parameters found in the HDL component appear in the Parameters tab.

4. On the Parameters tab, modify the parameter Name, Value, Type, Bit Width, and whether Editable.

![Parameters Tab for HDL Instantiation](image)

5. View the interfaces and signals, as Adding Generic Component Interfaces and Signals on page 122 describes.

6. When you are done adding parameters and interfaces, click Finish in the Component Instantiation editor. The component appears in the System View tab.

Note: You must treat a generic component with an Implementation Type of HDL as custom RTL, specific to your current system. When you set a generic component's Implementation Type to HDL, the output of any RTL that you add to the component is within the system's output directory.

2.4.2. Adding Generic Blackbox Component Parameters

You can specify and modify parameters for generic components that have a Blackbox implementation. This technique allows you to instantiate a component that defines only the signal and interface boundary of an entity, without providing the component's implementation at this stage. You can then add parameters and define their default properties in the Component Instantiation editor.

1. Define a generic blackbox component, as Adding Generic Components to a System on page 118 describes.

2. In the Component Instantiation editor, click the Parameters tab.
3. Click the **Add Parameter** button to add and specify default values for the parameter **Name**, **Value**, **Type**, **Bit Width**, and whether **Editable**.

4. Add signals and interfaces on the **Signals and Interfaces** tab, as **Adding Generic Component Interfaces and Signals** on page 122 describes.

5. When you are done adding parameters and interfaces, click **Finish** in the **Component Instantiation** editor. The component appears in the **System View** tab.

### 2.4.3. Adding Generic Component Interfaces and Signals

The **Signals & Interfaces** tab of the **Component Instantiation** editor allows you to customize signals and interfaces for your generic component:

1. Double-click **Generic Component** in the IP Catalog.

2. In the **Component Instantiation** editor, click the **Signals & Interfaces** tab, as **Adding Generic Component Interfaces and Signals** on page 122 describes.

3. To add an interface, click `<add interface>` in the left pane and select the interface. The selected interface appears in the parameter editor to the right, where you specify its parameters.

4. To add signals to the selected interface, click `<add signal>` below the selected interface.

5. To move signals between interfaces, select the signal and drag it to another interface.

6. To rename a signal or interface, select the element, and then press F2.

7. To remove a signal or interface, right-click the element, and then click **Remove**.

**Note:** Alternatively, to remove a signal or interface, select the element and press **Delete**. When you remove an interface, Platform Designer also removes all of its associated signals.
Figure 68. Creating Custom Interfaces

Note: To add existing template interfaces to your generic component, select the interface from the Templates menu in the Component Instantiation editor.

2.4.3.1. Mirroring Interfaces in a Generic Component

To mirror existing signals and interfaces from an IP component to your generic component:

1. Double-click Generic Component in the IP Catalog.
2. In the Component Instantiation editor, click the Signals & Interfaces tab.
3. Click the Mirror button. A list appears which lists all the available components in the system and their associated interfaces.
4. Select the desired interface. Platform Designer mirrors the interface and its associated signals and adds the mirrored interfaces and signals to the Signals & Interfaces tab of the generic component.

Example 15. Mirroring Interfaces in a Generic Component Example

<table>
<thead>
<tr>
<th>Selected Interface</th>
<th>Mirrored Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Avalon Memory-Mapped Master (avalon_master)</td>
<td>Avalon Memory-Mapped Slave (avalon_slave)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Signals of the Selected Interface</th>
<th>Signals of the Mirrored Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>waitrequest(Input 1)</td>
<td>waitrequest(Output 1)</td>
</tr>
<tr>
<td>readdata(Input 32)</td>
<td>readdata(Output 32)</td>
</tr>
<tr>
<td>readdatavalid(Input 1)</td>
<td>readdatavalid(Output 1)</td>
</tr>
<tr>
<td>burstcount(Output 32)</td>
<td>burstcount(Input 32)</td>
</tr>
</tbody>
</table>
2.4.3.2. Cloning Interfaces in a Generic Component

To clone existing signals and interfaces from an IP component to your generic component:

1. Double-click **Generic Component** in the IP Catalog.
2. In the **Component Instantiation** editor, click the **Signals & Interfaces** tab.
3. Click the **Clone** button. A list appears which lists all the available components in the system and their associated interfaces.
4. Select the desired interface. Platform Designer clones the interface and adds an exact replica of the interface and its associated signals to the **Signals & Interfaces** tab of the generic component.
Figure 70. Cloning Interfaces

2.4.3.3 Importing Interfaces to a Generic Component

To import interfaces from an existing IP or IP-XACT(3) file to a generic component:

1. Double-click **Generic Component** in the IP Catalog.
2. In the **Component Instantiation** editor, click the **Signals & Interfaces** tab.
3. Click the **Import** button. A dialog box appears from where you choose the IP/IP-XACT file to import to the generic component.
4. Select the interface. Platform Designer populates the **Signals & Interfaces** tab with the signals and interfaces defined in the selected file.

(3) Platform Designer supports importing and exporting files in IP-XACT 2009 format and exporting IP-XACT files in 2014 format.
2.4.4. Adding Generic HLS Components

High Level Synthesis (HLS) files can be compiled to create Platform Designer components and are written according to the \texttt{i++} specification. HLS files can be in \texttt{*.c,*.cc,*.cpp,*.c++,*.cp, or *.cxx} format.

An HLS file defines one or more components in an \texttt{i++} format that Platform Designer compiles into HDL. In order to add components from an HLS file there are two basic steps:

1. Identify and add the HLS file.
2. \textbf{Import} an already compiled file from a previous Platform Designer session or project, or \textbf{Compile} the HLS file in Platform Designer.

Once the component has been imported or compiled, Platform Designer performs the following actions:

- Imports an \texttt{.ip} resulting from the HLS compilation to the component name defined in the HLS file.
- Sets the \textbf{HDL entity name} and \textbf{HDL compilation library} to the component defined in the HLS file.
- Adds the \texttt{.ip} file to the empty generic component.
- Adds paths to the \texttt{.ip} and \texttt{.hw.tcl} output files to the Platform Designer search path to enable instantiation.
- Populates the signals and interfaces of the component from the \texttt{.ip} file.
After compilation, the HLS compiler creates a `<component_name>.prj` folder with the following directories:

<table>
<thead>
<tr>
<th>Folder</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>/component</td>
<td>Contains IP and _hw.tcl files.</td>
</tr>
<tr>
<td>/quartus</td>
<td>Contains Intel Quartus Prime Pro Edition project files that instantiate the HLS component. You can use this to verify timing and logic usage.</td>
</tr>
<tr>
<td>/reports</td>
<td>Contains a compilation report in HTML.</td>
</tr>
<tr>
<td>/verification</td>
<td>Contains verification files, if you decided to create a verification executable.</td>
</tr>
</tbody>
</table>

**Related Information**

Intel High Level Synthesis Compiler Getting Started Guide

**2.4.4.1. Add High Level Synthesis Files to a Generic Component**

You can quickly add High Level Synthesis (HLS) components to a Platform Designer project by dragging and dropping files into the Platform Designer **System View** tab. The drag-and-drop process selects the HLS implementation type, and adds the HLS file to the **HLS files** box.

To add a component with an HLS implementation, perform the following steps in Platform Designer:

1. Drag an HLS file to the **System View** tab of Platform Designer.
   or
2. Type generic component in the IP Catalog.
3. To launch the **Component Instantiation** editor, double-click **Generic Component**.
4. To add a component from an HLS file to the empty generic component, select the **HLS Implementation Type**.
5. Click + and select an HLS file to add.

You can click + to add more than one HLS file. Click - to remove HLS files. The primary case for adding multiple HLS files is when you are using a library of components defined by one or more high level synthesis files.

**Figure 72. Add an HLS Implementation Type File**
2.4.4.2. Compile High Level Synthesis Files

The **Compile** option for High Level Synthesis (HLS) component instantiation in Platform Designer invokes the Intel HLS Compiler to compile HLS files and modify a generic component.

Performing a compile on an HLS file has the following results:

- Imports an `.ip` resulting from the HLS compilation to the component name defined in the HLS file.
- Sets the **HDL entity name** and **HDL compilation library** to the component defined in the HLS file.
- Adds the `.ip` file to the empty generic component.
- Adds paths to the `.ip` and `_hw.tcl` output files to the Platform Designer search path to enable instantiation.
- Populates the signals and interfaces of the component from the `.ip` file.

After you have added an HLS file:

1. Click **Compile**.

**Figure 73.** HLS Component Instantiation

2. In the **HLS Options** dialog box, you can select from the following options:

---

**Related Information**

- **Compile High Level Synthesis Files** on page 128
- **Import High Level Synthesis Files** on page 130

---

Figure 74. HLS Options Dialog Box

![HLS Options Dialog Box](image)

- The project name defaults to the entity name defined in the HLS file. To set a new project name, select **new project name** and enter a new HLS project name in the dialog box.

**Figure 75. Change the Project Name**

![Change the Project Name](image)

- Provide additional arguments to the HLS compiler. Refer to **Command Compiler Options** in the *Intel High Level Synthesis Reference Manual* for information on compiler arguments.

- Disable or enable simulation file creation. A simulation file is required to use the **Run Verification** option after compilation is complete.

- Enable verbose logging to create a compilation log file.

- Enable or disable display of the HLS report in a browser window directly after compilation is complete.

- Perform verification with or without additional verification arguments if you chose to create a verification executable. Refer to the *Intel High Level Synthesis Compiler User Guide* for information on verification arguments.

3. Click **OK** to compile the HLS file and create the component.

4. If your HLS file defines more than one component, the **Choose File to Import** dialog box prompts you to select a specific component from a list.

5. After compiling, click **Show Report** to display a compilation report in a browser window.

6. If you created simulation files for your component, you can click **Run Verification** to perform verification.

**Related Information**

- Compiler Command Options
- Intel High Level Synthesis Compiler User Guide
2.4.4.3. Import High Level Synthesis Files

If you have a compiled High Level Synthesis (HLS) file, you can import it instead to save compilation time.

1. Click **Import**.

**Figure 76. HLS Component Instantiation**

You should only use **Import** when your HLS file defines previously compiled components.

2. In the **HLS Options** dialog box, you can select from the following options:
   a. The project name defaults to the entity name defined in the HLS file. To set a new project name, select **new project name** and enter a new HLS project name in the dialog box.

**Figure 77. HLS Options Dialog Box**

b. Enable or disable display of the HLS report in a browser window directly after compilation is complete.
Perform verification with or without additional verification arguments if you chose to create a verification executable. Refer to the *Intel High Level Synthesis Compiler User Guide* for information on verification arguments.

3. Click **OK**.
4. If your HLS file defines more than one component, the **Choose File to Import** dialog box prompts you to select a specific component .ip from a list.
5. After importing, click **Show Report** to display a compilation report in a browser window if the compilation report is enabled.
6. Click **Run Verification** to perform verification if it is enabled.

**Related Information**

*Intel High Level Synthesis Compiler User Guide*

### 2.4.5. Creating a System Template for a Generic Component

To create a Platform Designer system template:

1. Double-click **Generic Component** in the IP Catalog.
2. In the **Component Instantiation** editor, add the interfaces and signals for the new component in the **Signals & Interfaces** tab, as .
3. Select the **Implementation Templates** tab.
4. Click **Create Platform Designer System Template** button. This option creates an empty Platform Designer system and saves the template as a .qsys file to implement this generic component.

**Figure 79. Creating System templates**

To implement this component:

1. To open the template Platform Designer system, click **File ➤ Open** and choose the specific .qsys file.
2. Add either or both IP components and generic components then export their interfaces to satisfy the specified interface requirements.
3. To view the exported interfaces in the **Interface Requirements** tab, select **View ➤ Interface Requirements**.
2.4.6. Exporting a Generic Component

You can export a generic component as a .ipxact file as well as _hw.tcl file:

1. Double-click **Generic Component** in the IP Catalog.
2. Select the **Export** tab.
3. To export generic component as an IP-XACT file, click **Export IP-XACT File** and select the location to save your IP-XACT file.
4. To export generic component as a _hw.tcl file, click **Export _hw.tcl File** and select the location to save your _hw.tcl file.

2.5. Scripting Wire-Level Expressions

Platform Designer supports system scripting commands to apply wire-level expressions to input ports in IP components.

The following commands function with the qsys-script utility or in a _hw.tcl file to set, retrieve, or remove an expression on a port:

```plaintext
set_wirelevel_expression <instance_or_port_bit> <expression>
get_wirelevel_expressions <instance_or_port_bit>
remove_wirelevel_expressions <instance_or_port_bit>
```

These commands require a string that you compose from the left-handed and right-handed components of the expression. Platform Designer reports errors in syntax, existence, or system hierarchy.

**Related Information**

- Wired-Level Connection Commands on page 562
- set_wirelevel_expression on page 563
- get_wirelevel_expressions on page 563
- remove_wirelevel_expressions on page 564
2.6. Control Interfaces Dynamically with an Elaboration Callback

You can allow user parameters to dynamically control your component's behavior with an elaboration callback procedure during the elaboration phase. Using an elaboration callback allows you to change interface properties, remove interfaces, or add new interfaces as a function of a parameter value. You define an elaboration callback by setting the module property `ELABORATION_CALLBACK` to the name of the Tcl callback procedure that runs during the elaboration phase. In the callback procedure, you can query the parameter values of the component instance, and then change the interfaces accordingly.

**Example 16. Avalon Streaming Source Interface Optionally Included in a Component Specified with an Elaboration Callback**

```tcl
set_module_property ELABORATION_CALLBACK elaborate
proc elaborate {} {
    # Optionally disable the Avalon streaming data output
    if {[get_parameter_value ENABLE_STREAM_OUTPUT] == "false" }{
        set_port_property aso_data    termination true
        set_port_property aso_valid   termination true
        set_port_property aso_ready   termination true
        set_port_property aso_ready   termination_value 0
    }
    # Calculate the Data Bus Width in bytes
    set bytewidth_var [expr {[get_parameter_value AXI_DATA_W]/8}]
    set_parameter_value AXI_NUMBYTES $bytewidth_var
}
```

**Related Information**
- Declare Parameters with Custom `_hw.tcl` Commands on page 115
- Validate Parameter Values with a Validation Callback on page 117
- Component Interface Tcl Reference on page 594

2.7. Control File Generation Dynamically with Parameters and a Fileset Callback

You can use a fileset callback to control which files are created in the output directories during the generation phase based on parameter values, instead of providing a fixed list of files. In a callback procedure, you can query the values of the parameters and use them to generate the appropriate files. To define a fileset callback, you specify a callback procedure name as an argument in the `add_fileset` command. You can use the same fileset callback procedure for all of the filesets, or create separate procedures for synthesis and simulation, or Verilog and VHDL.

**Example 17. Fileset Callback Using Parameters to Control Filesets in Two Different Ways**

The `RAM_VERSION` parameter chooses between two different source files to control the implementation of a RAM block. For the top-level source file, a custom Tcl routine generates HDL that optionally includes control and status registers, depending on the value of the `CSR_ENABLED` parameter.
During the generation phase, Platform Designer creates a top-level Platform Designer system HDL wrapper module to instantiate the component top-level module, and applies the component's parameters, for any parameter whose parameter property HDL_PARAMETER is set to true.

```tcl
# Create synthesis fileset with fileset_callback and set top level
add_fileset my_synthesis_fileset QUARTUS_SYNTH fileset_callback
set_fileset_property my_synthesis_fileset TOP_LEVEL demo_axi_memory

# Create Verilog simulation fileset with same fileset_callback
# and set top level
add_fileset my_verilog_sim_fileset SIM_VERILOG fileset_callback
set_fileset_property my_verilog_sim_fileset TOP_LEVEL demo_axi_memory

# Add extra file needed for simulation only
add_fileset_file verbosity_pkg.sv SYSTEM_VERILOG PATH verification_lib/verbosity_pkg.sv

# Create VHDL simulation fileset (with Verilog files for mixed-language VHDL simulation)
add_fileset my_vhdl_sim_fileset SIM_VHDL fileset_callback
set_fileset_property my_vhdl_sim_fileset TOP_LEVEL demo_axi_memory

add_fileset_file verbosity_pkg.sv SYSTEM_VERILOG PATH verification_lib/verbosity_pkg.sv

# Define parameters required for fileset_callback
add_parameter RAM_VERSION INTEGER 1
set_parameter_property RAM_VERSION ALLOWED_RANGES {1 2}
set_parameter_property RAM_VERSION HDL_PARAMETER false
add_parameter CSR_ENABLED BOOLEAN enable
set_parameter_property CSR_ENABLED HDL_PARAMETER false

# Create Tcl callback procedure to add appropriate files to filesets based on parameters
proc fileset_callback { entityName } {
    send_message INFO "Generating top-level entity $entityName"
    set ram [get_parameter_value RAM_VERSION]
    set csr_enabled [get_parameter_value CSR_ENABLED]

    send_message INFO "Generating memory implementation based on RAM_VERSION $ram"
    if {$ram == 1} {
        add_fileset_file single_clk_ram1.v VERILOG PATH single_clk_ram1.v
    } else {
        add_fileset_file single_clk_ram2.v VERILOG PATH single_clk_ram2.v
    }

    send_message INFO "Generating top-level file for CSR_ENABLED $csr_enabled"
    generate_my_custom_hdl $csr_enabled demo_axi_memory_gen.sv

    add_fileset_file demo_axi_memory_gen.sv VERILOG PATH demo_axi_memory_gen.sv
}
```
2.8. Create a Composed Component or Subsystem

A composed component is a subsystem containing instances of other components. Unlike an HDL-based component, a composed component's HDL is created by generating HDL for the components in the subsystem, in addition to the Platform Designer interconnect to connect the subsystem instances.

You can add child instances in a composition callback of the _hw.tcl file.

With a composition callback, you can also instantiate and parameterize subcomponents as a function of the composed component's parameter values. You define a composition callback by setting the COMPOSITION_CALLBACK module property to the name of the composition callback procedures.

A composition callback replaces the validation and elaboration phases. HDL for the subsystem is generated by generating all of the sub-components and the top-level that combines them.

To connect instances of your component, you must define the component's interfaces. Unlike an HDL-based component, a composed component does not directly specify the signals that are exported. Instead, interfaces of submodules are chosen as the external interface, and each internal interface's ports are connected through the exported interface.

Exporting an interface means that you are making the interface visible from the outside of your component, instead of connecting it internally. You can set the EXPORT_OF property of the externally visible interface from the main program or the composition callback, to indicate that it is an exported view of the submodule's interface.

Exporting an interface is different than defining an interface. An exported interface is an exact copy of the subcomponent’s interface, and you are not allowed to change properties on the exported interface. For example, if the internal interface is a 32-bit or 64-bit master without bursting, then the exported interface is the same. An interface on a subcomponent cannot be exported and also connected within the subsystem.

When you create an exported interface, the properties of the exported interface are copied from the subcomponent's interface without modification. Ports are copied from the subcomponent's interface with only one modification; the names of the exported ports on the composed component are chosen to ensure that they are unique.
Example 18. Composed _hw.tcl File that Instantiates Two Sub-Components

Platform Designer connects the components, and also connects the clocks and resets. Note that clock and reset bridge components are required to allow both sub-components to see common clock and reset inputs.

```tcl
package require -exact qsys 14.0
set_module_property name my_component
set_module_property COMPOSITION_CALLBACK composed_component

proc composed_component {} {
    add_instance clk altera_clock_bridge
    add_instance reset altera_reset_bridge
    add_instance regs my_regs_microcore
    add_instance phy my_phy_microcore

    add_interface clk clock end
    add_interface reset reset end
    add_interface slave avalon slave
    add_interface pins conduit end

    set_interface_property clk EXPORT_OF clk.in_clk
    set_instance_property_value reset synchronous_edges deassert
    set_interface_property reset EXPORT_OF reset.in_reset
    set_interface_property slave EXPORT_OF regs.slave
    set_interface_property pins EXPORT_OF phy.pins

    add_connection clk.out_clk reset.clk
    add_connection clk.out_clk regs.clk
    add_connection clk.out_clk phy.clk
    add_connection reset.out_reset regs.reset
    add_connection reset.out_reset phy.clk_reset
    add_connection regs.output phy.input
    add_connection phy.output regs.input
}
```

Related Information

Component Interface Tcl Reference on page 594
2.9. Add Component Instances to a Static or Generated Component

You can create nested components by adding component instances to an existing component. Both static and generated components can create instances of other components. You can add child instances of a component in a _hw.tcl using elaboration callback.

With an elaboration callback, you can also instantiate and parameterize sub-components with the `add_hdl_instance` command as a function of the parent component's parameter values.

When you instantiate multiple nested components, you must create a unique variation name for each component with the `add_hdl_instance` command. Prefixing a variation name with the parent component name prevents conflicts in a system. The variation name can be the same across multiple parent components if the generated parameterization of the nested component is exactly the same.

*Note:* If you do not adhere to the above naming variation guidelines, Platform Designer validation-time errors occur, which are often difficult to debug.

**Related Information**
- Static IP Components on page 137
- Generated Components on page 138

2.9.1. Static IP Components

Static IP components always generate the same output, regardless of their parameterization. Components that instantiate static components must have only static children.

A design file that is static between all parameterizations of a component can only instantiate other static design files. Since static IPs always render the same HDL regardless of parameterization, Platform Designer generates static IPs only once across multiple instantiations, meaning they have the same top-level name set.

**Example 19. Typical Usage of the add_hdl_instance Command for Static Components**

```tcl
package require -exact qsys 14.0

set_module_property name add_hdl_instance_example
add_fileset synth_fileset QUARTUS_SYNTH synth_callback
set_fileset_property synth_fileset TOP_LEVEL basic_static
set_module_property elaboration_callback elab

proc elab {} {
    # Actual API to instantiate an IP Core
    add_hdl_instance emif_instance_name altera_mem_if_ddr3_emif

    # Make sure the parameters are set appropriately
    set_instance_parameter_value emif_instance_name SPEED_GRADE {7}
    ...
}
proc synth_callback { output_name } {
    add_fileset_file "basic_static.v" VERILOG PATH basic_static.v
}
```
Example 20. Top-Level HDL Instance and Wrapper File Created by Platform Designer

In this example, Platform Designer generates a wrapper file for the instance name specified in the _hw.tcl file.

```vhdl
// Top Level Component HDL
module basic_static (input_wire, output_wire, inout_wire);
input [31:0] input_wire;
output [31:0] output_wire;
inout [31:0] inout_wire;

// Instantiation of the instance added via add_hdl_instance
// command. This is an example of how the instance added via
// the add_hdl_instance command can be used
// in the top-level file of the component.
emif_instance_name fixed_name_instantiation_in_top_level(
  .pll_ref_clk (input_wire), // pll_ref_clk.clk
  .global_reset_n (input_wire), // global_reset.reset_n
  .soft_reset_n (input_wire), // soft_reset.reset_n
  ...
);  
endmodule

// Wrapper for added HDL instance
// emif_instance_name.v
// Generated using ACDS version 14.0
`timescale 1 ps / 1 ps
module emif_instance_name (
  input wire pll_ref_clk, // pll_ref_clk.clk
  input wire global_reset_n, // global_reset.reset_n
  input wire soft_reset_n, // soft_reset.reset_n
  output wire afi_clk, // afi_clk.clk
  ...
);
example_addhdlinstance_system
  _add_hdl_instance_example_0_emif_instance
  _name_emif_instance_name emif_instance_name (
    .pll_ref_clk (pll_ref_clk), // pll_ref_clk.clk
    .global_reset_n (global_reset_n), // global_reset.reset_n
    .soft_reset_n (soft_reset_n), // soft_reset.reset_n
    ...
);  
endmodule
```

2.9.2. Generated Components

A generated component's fileset callback allows an instance of the component to create unique HDL design files based on the instance's parameter values. For example, you can write a fileset callback to include a control and status interface based on the value of a parameter. The callback overcomes a limitation of HDL languages, which do not allow run-time parameters.

Generated components change their generation output (HDL) based on their parameterization. If a component is generated, then any component that may instantiate it with multiple parameter sets must also be considered generated, since its HDL changes with its parameterization. This case has an effect that propagates up to the top-level of a design.

Since generated components are generated for each unique parameterized instantiation, when implementing the add_hdl_instance command, you cannot use the same fixed name (specified using instance_name) for the different variants of
the child HDL instances. To facilitate unique naming for the wrapper of each unique parameterized instantiation of child HDL instances, you must use the following command so that Platform Designer generates a unique name for each wrapper. You can then access this unique wrapper name with a fileset callback so that the instances are instantiated inside the component's top-level HDL.

- To declare auto-generated fixed names for wrappers, use the command:

  ```
  set_instance_property instance_name HDLINSTANCE_USE_GENERATED_NAME true
  ```

  **Note:** You can only use this command with a generated component in the global context, or in an elaboration callback.

- To obtain auto-generated fixed name with a fileset callback, use the command:

  ```
  get_instance_property instance_name HDLINSTANCE_GET_GENERATED_NAME
  ```

  **Note:** You can only use this command with a fileset callback. This command returns the value of the auto-generated fixed name, which you can then use to instantiate inside the top-level HDL.

**Example 21. Typical Usage of the add_hdl_instance Command for Generated Components**

Platform Designer generates a wrapper file for the instance name specified in the _hw.tcl file.

```tcl
package require -exact qsys 14.0
set_module_property name generated_toplevel_component
set_module_property ELABORATION_CALLBACK elaborate
add_fileset QUARTUS_SYNTH QUARTUS_SYNTH generate
add_fileset SIM_VERILOG SIM_VERILOG generate
add_fileset SIM_VHDL SIM_VHDL generate
proc elaborate {} {
    # Actual API to instantiate an IP Core
    add_hdl_instance emif_instance_name altera_mem_if_ddr3_emif

    # Make sure the parameters are set appropriately
    set_instance_parameter_value emif_instance_name SPEED_GRADE 7

    # instruct Platform Designer to use auto generated fixed name
    set_instance_property emif_instance_name HDLINSTANCE_USE_GENERATED_NAME 1
}
proc generate { entity_name } {
    # get the autogenerated name for emif_instance_name added
    # via add_hdl_instance
    set autogeneratedfixedname [get_instance_property
        emif_instance_name HDLINSTANCE_GET_GENERATED_NAME]
    set fileID [open "generated_toplevel_component.v" r]
    set temp ""

    # read the contents of the file
    while {[eof $fileID] != 1} {
        gets $fileID lineInfo
        # replace the top level entity name with the name provided
        set lineInfo [regsub -all "substitute_entity_name_here" "$lineInfo \
```
Example 22. Top-Level HDL Instance and Wrapper File Created By Platform Designer

```verilog
module substitute_entity_name_here (input_wire, output_wire, inout_wire);
  input [31:0] input_wire;
  output [31:0] output_wire;
  inout [31:0] inout_wire;

  // Instantiation of the instance added via add_hdl_instance
  // command. This is an example of how the instance added
  // via add_hdl_instance command can be used
  // in the top-level file of the component.

  substitute_autogenerated_emifinstancename_here
    fixed_name_instantiation_in_top_level (
      .pll_ref_clk (input_wire), // pll_ref_clk.clk
      .global_reset_n (input_wire), // global_reset.reset_n
      .soft_reset_n (input_wire), // soft_reset.reset_n
      ...
    );
endmodule

// Wrapper for added HDL instance
// generated_toplevel_component_0_emif_instance_name.v is the
// auto generated //emif_instance_name
// Generated using ACDS version 13.

`timescale 1 ps / 1 ps
module generated_toplevel_component_0_emif_instance_name (
  input wire pll_ref_clk, // pll_ref_clk.clk
  input wire global_reset_n, // global_reset.reset_n
  input wire soft_reset_n, // soft_reset.reset_n
  output wire afi_clk, // afi_clk.clk
  ...
);

example_addhdlinstance_system_add_hdl_instance_example_0_emif
  _instance_name_emif_instance_name emif_instance_name (
    .pll_ref_clk (pll_ref_clk), // pll_ref_clk.clk
    .global_reset_n (global_reset_n), // global_reset.reset_n
    .soft_reset_n (soft_reset_n), // soft_reset.reset_n
    ...
); endmodule
```

Related Information

- Control File Generation Dynamically with Parameters and a Fileset Callback on page 133
- Intellectual Property & Reference Designs
2.9.3. Design Guidelines for Adding Component Instances

In order to promote standard and predictable results when generating static and generated components, follow these best-practices:

- For two different parameterizations of a component, a component must never generate a file of the same name with different instantiations. The contents of a file of the same name must be identical for every parameterization of the component.

- If a component generates a nested component, it must never instantiate two different parameterizations of the nested component using the same instance name. If the parent component's parameterization affects the parameters of the nested component, the parent component must use a unique instance name for each unique parameterization of the nested component.

- Static components that generate differently based on parameterization have the potential to cause problems in the following cases:
  - Different file names with the same entity names, results in same entity conflicts at compilation-time
  - Different contents with the same file name results in overwriting other instances of the component, and in either file, compile-time conflicts or unexpected behavior.

- Generated components that generate files not based on the output name and that have different content results in either compile-time conflicts, or unexpected behavior.

- If preserving a custom component as part of an Intel Quartus Prime Archive (.qar), you must first explicitly add the component _hw.tcl file to the project to ensure that the .qar includes the component. Click Project ➤ Add/Remove Files in Project to add files to your project.

---

2.10. Creating Platform Designer Components Revision History

The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2020.09.28        | 20.3                       | • Revised "Adding Generic Components to a System" to describes all implementations and refer to substeps for HDL and Blackbox parameters.  
  • Revised "Adding Generic HDL Component Parameters" for latest steps and screenshot.  
  • Added new "Adding Generic Blackbox Component Parameters" topic.  
  • Added statement about AFFECTS_GENERATION to "Specify Parameters in the Platform Designer Component Editor" topic.  
  • Reorganized the order of some topic to group similar items. |
| 2020.05.01        | 20.1                       | • Added note about .qar file requirements to "Design Guidelines for Component Instances" topic. |
| 2020.04.06        | 18.1.0                     | • Updated links and web page names in "Component Structure" and "Creating Platform Designer Components" topics. |
| 2019.06.19        | 18.1.0                     | • Added descriptions of AXI parameters in "Specify Parameters in the Platform Designer Component Editor." |

continued...
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<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.12.15</td>
<td>18.1.0</td>
<td>• Replaced references to System Contents tab with new System View tab.</td>
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<tr>
<td>2018.05.07</td>
<td>18.0</td>
<td>• Added scripting support for wire-level expressions.</td>
</tr>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>• Changed instances of Qsys Pro to Platform Designer</td>
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<td></td>
<td></td>
<td>• Replaced mentions of altera_axi_default_slave to altera_error_response_slave</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added support for SystemVerilog interfaces with _hw.tcl.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added support for user alterable HDL parameters with _hw.tcl.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added support for High Level Synthesis file compilation.</td>
</tr>
<tr>
<td>2017.05.08</td>
<td>17.0.0</td>
<td>• Updated Figure: Address Span Extender</td>
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<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Implemented Intel rebranding.</td>
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<td></td>
<td></td>
<td>• Implemented Qsys rebranding.</td>
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<tr>
<td></td>
<td></td>
<td>• Added topics for Generic Component.</td>
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<tr>
<td>2015.11.02</td>
<td>15.1.0</td>
<td>Changed instances of Quartus II to Quartus Prime.</td>
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<tr>
<td>2015.05.04</td>
<td>15.0.0</td>
<td>• Updated screen shots Files tab, Qsys Component Editor.</td>
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<tr>
<td></td>
<td></td>
<td>• Added topic: Specify Interfaces and Signals in the Qsys Component Editor.</td>
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<td></td>
<td>• Added topic: Create an HDL File in the Qsys Component Editor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added topic: Create an HDL File Using a Template in the Qsys Component Editor.</td>
</tr>
<tr>
<td>November 2013</td>
<td>13.1.0</td>
<td>• add_hdl_instance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added Creating a Component With Differing Structural Qsys View and Generated Output Files.</td>
</tr>
<tr>
<td>May 2013</td>
<td>13.0.0</td>
<td>• Consolidated content from other Qsys chapters.</td>
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<tr>
<td></td>
<td></td>
<td>• Added Upgrading IP Components to the Latest Version.</td>
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<tr>
<td></td>
<td></td>
<td>• Updated for AMBA APB support.</td>
</tr>
<tr>
<td>November 2012</td>
<td>12.1.0</td>
<td>• Added AMBA AXI4 support.</td>
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<tr>
<td></td>
<td></td>
<td>• Added the demo_axi_memory example with screen shots and example _hw.tcl code.</td>
</tr>
<tr>
<td>June 2012</td>
<td>12.0.0</td>
<td>• Added new tab structure for the Component Editor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added AXI 3 support.</td>
</tr>
<tr>
<td>November 2011</td>
<td>11.1.0</td>
<td>Template update.</td>
</tr>
<tr>
<td>May 2011</td>
<td>11.0.0</td>
<td>• Removed beta status.</td>
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<tr>
<td></td>
<td></td>
<td>• Added Avalon Tri-state Conduit (Avalon-TC) interface type.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added many interface templates for Nios custom instructions and Avalon-TC interfaces.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.1.0</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
3. Platform Designer Interconnect

Platform Designer interconnect is a high-bandwidth structure that allows you to connect IP components to other IP components with various interfaces.

Platform Designer allows you to establish connections between Avalon and AXI interfaces by generating an interconnect logic. This logic enables you to handle the protocol differences. Platform Designer creates the interconnect logic by converting all the protocols to a proprietary packet format. Then, the tool routes the packet through network switches to the appropriate slaves. Here, the packet converts to the slave’s protocol.

Platform Designer supports Avalon, AMBA 3 AXI (version 1.0), AMBA 4 AXI (version 2.0), AMBA 4 AXI-Lite (version 2.0), AMBA 4 AXI-Stream (version 1.0), and AMBA 3 APB (version 1.0) interface specifications.

The video AMBA AXI and Intel Avalon Interoperation Using Platform Designer describes seamless integration of IP components using the AMBA AXI and the Intel Avalon interfaces.

Synchronous Reset Support

Platform Designer interconnect now supports synchronous reset of registers in the interconnect. Use of synchronous reset can result in higher performance for Intel Stratix 10 designs because Intel Stratix 10 Hyper-Registers lack a reset signal. If a register in your Intel Stratix 10 design uses asynchronous reset, the Compiler cannot implement the register as a Hyper-Register, potentially reducing performance.

When Use synchronous reset is set to True in the Domains tab, all registers in the interconnect use synchronous reset. The Use synchronous reset option is enabled by default for Intel Stratix 10 devices, but is disabled by default for all other devices.

Note: In Platform Designer systems with no clock domain crossing, the initial reset requires asserting for at least 16 cycles. This action prevents the propagation of incorrect values that the reset tree skew may generate during the initial reset release, ensuring the resetting of all the Platform Designer components and interconnect. If system has multiple clocks, reset must be held high for at least 16 slowest clock cycles.

Related Information

- Avalon Interface Specifications
- Creating a System with Platform Designer on page 10
- Creating Platform Designer Components on page 90
- Platform Designer System Design Components on page 302
- AMBA AXI and Intel Avalon Interoperation Using Platform Designer
- Specifying Interconnect Parameters on page 50
3.1. Memory-Mapped Interfaces

Platform Designer supports the implementation of memory-mapped interfaces for Avalon, AXI, and APB protocols.

Platform Designer interconnect transmits memory-mapped transactions between masters and slaves in packets. The command network transports read and write packets from master interfaces to slave interfaces. The response network transports response packets from slave interfaces to master interfaces.

For each component interface, Platform Designer interconnect manages memory-mapped transfers and interacts with signals on the connected interface. Master and slave interfaces can implement different signals based on interface parameterizations, and Platform Designer interconnect provides any necessary adaptation between them.

In the path between master and slaves, Platform Designer interconnect may introduce registers for timing synchronization, finite state machines for event sequencing, or nothing at all, depending on the services required by the interfaces.

Platform Designer interconnect supports the following implementation scenarios:

- Any number of components with master and slave interfaces. The master-to-slave relationship can be one-to-one, one-to-many, many-to-one, or many-to-many.
- Masters and slaves of different data widths.
- Masters and slaves operating in different clock domains.
- IP Components with different interface properties and signals. Platform Designer adapts the component interfaces so that interfaces with the following differences can be connected:
  - Avalon and AXI interfaces that use active-high and active-low signaling. AXI signals are active high, except for the reset signal.
  - Interfaces with different burst characteristics.
  - Interfaces with different latencies.
  - Interfaces with different data widths.
  - Interfaces with different optional interface signals.

  Note: Since interface connections between AMBA 3 AXI and AMBA 4 AXI declare a fixed set of signals with variable latency, there is no need for adapting between active-low and active-high signaling, burst characteristics, different latencies, or port signatures. Adaptation might be necessary between Avalon interfaces.

In this example, there are two components mastering the system, a processor and a DMA controller, each with two master interfaces. The masters connect through the Platform Designer interconnect to slaves in the Platform Designer system.

The dark blue blocks represent interconnect components. The dark gray boxes indicate items outside of the Platform Designer system and the Intel Quartus Prime software design, and show how to export component interfaces and how to connect these interfaces to external devices.
3.1.1. Platform Designer Packet Format

The Platform Designer packet format supports Avalon, AXI, and APB transactions. Memory-mapped transactions between masters and slaves are encapsulated in Platform Designer packets. For Avalon systems without AXI or APB interfaces, some fields are ignored or removed.
### 3.1.1.1. Fields in the Platform Designer Packet Format

The fields of the Platform Designer packet format are of variable length to minimize resource usage. However, if most components in a design have a single data width, for example 32-bits, and a single component has a data width of 64-bits, Platform Designer inserts a width adapter to accommodate 64-bit transfers.

**Table 34. Platform Designer Packet Format for Memory-Mapped Master and Slave Interfaces**

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
<td>Specifies the byte address for the lowest byte in the current cycle. There are no restrictions on address alignment.</td>
</tr>
<tr>
<td>Size</td>
<td>Encodes the run-time size of the transaction. In conjunction with address, this field describes the segment of the payload that contains valid data for a beat within the packet.</td>
</tr>
<tr>
<td>Address Sideband</td>
<td>Carries &quot;address&quot; sideband signals. The interconnect passes this field from master to slave. This field is valid for each beat in a packet, even though it is only produced and consumed by an address cycle. Up to 8-bit sideband signals are supported for both read and write address channels.</td>
</tr>
<tr>
<td>Cache</td>
<td>Carries the AXI cache signals.</td>
</tr>
<tr>
<td>Transaction (Exclusive)</td>
<td>Indicates whether the transaction has exclusive access.</td>
</tr>
<tr>
<td>Transaction (Posted)</td>
<td>Used to indicate non-posted writes (writes that require responses).</td>
</tr>
<tr>
<td>Data</td>
<td>For command packets, carries the data to be written. For read response packets, carries the data that has been read.</td>
</tr>
<tr>
<td>Byteenable</td>
<td>Specifies which symbols are valid. AXI can issue or accept any byteenable pattern. For compatibility with Avalon, Intel recommends that you use the following legal values for 32-bit data transactions between Avalon masters and slaves:</td>
</tr>
<tr>
<td></td>
<td>• 1111—Writes full 32 bits</td>
</tr>
<tr>
<td></td>
<td>• 0011—Writes lower 2 bytes</td>
</tr>
<tr>
<td></td>
<td>• 1100—Writes upper 2 bytes</td>
</tr>
<tr>
<td></td>
<td>• 0001—Writes byte 0 only</td>
</tr>
<tr>
<td></td>
<td>• 0010—Writes byte 1 only</td>
</tr>
<tr>
<td></td>
<td>• 0100—Writes byte 2 only</td>
</tr>
<tr>
<td></td>
<td>• 1000—Writes byte 3 only</td>
</tr>
<tr>
<td>Source_ID</td>
<td>The ID of the master or slave that initiated the command or response.</td>
</tr>
<tr>
<td>Destination_ID</td>
<td>The ID of the master or slave to which the command or response is directed.</td>
</tr>
<tr>
<td>Response</td>
<td>Carries the AXI response signals.</td>
</tr>
<tr>
<td>Thread ID</td>
<td>Carries the AXI transaction ID values.</td>
</tr>
<tr>
<td>Byte count</td>
<td>The number of bytes remaining in the transaction, including this beat. Number of bytes requested by the packet.</td>
</tr>
</tbody>
</table>

*continued...*
### Command: Burstwrap

The burstwrap value specifies the wrapping behavior of the current burst. The burstwrap value is of the form $2^n - 1$. The following types are defined:

- **Variable wrap**: Variable wrap bursts can wrap at any integer power of 2 value. When the burst reaches the wrap boundary, it wraps back to the previous burst boundary so that only the low order bits are used for addressing. For example, a burst starting at address 0x1C, with a burst wrap boundary of 32 bytes and a burst size of 20 bytes, would write to addresses 0x1C, 0x0, 0x4, 0x8, and 0xC.

- For a burst wrap boundary of size $<m>$, Burstwrap = $<m> - 1$, or for this case Burstwrap = $(32 - 1) = 31$ which is $2^5 - 1$.

- For AXI masters, the burstwrap boundary value ($m$) is based on the different AXBURST:
  - Burstwrap set to all 1's. For example, for a 6-bit burstwrap, burstwrap is $6'b111111$.
  - For WRAP bursts, burstwrap = AXLEN * size – 1.
  - For FIXED bursts, burstwrap = size – 1.
  - Sequential bursts increment the address for each transfer in the burst. For sequential bursts, the Burstwrap field is set to all 1's. For example, with a 6-bit Burstwrap field, the value for a sequential burst is $6'b111111$ or 63, which is $2^6 - 1$.

For Avalon masters, Platform Designer adaptation logic sets a hardwired value for the burstwrap field, according to the declared master burst properties. For example, for a master that declares sequential bursting, the burstwrap field is set to ones. Similarly, masters that declare burst have their burstwrap field set to the appropriate constant value.

For AXI masters, the burstwrap boundary value ($m$) is based on the different AXBURST:

- Burstwrap set to all 1's. For example, for a 6-bit burstwrap, burstwrap is $6'b111111$.
- For WRAP bursts, burstwrap = AXLEN * size – 1.
- For FIXED bursts, burstwrap = size – 1.
- Sequential bursts increment the address for each transfer in the burst. For sequential bursts, the Burstwrap field is set to all 1's. For example, with a 6-bit Burstwrap field, the value for a sequential burst is $6'b111111$ or 63, which is $2^6 - 1$.

### Command: Protection

Access level protection. When the lowest bit is 0, the packet has normal access. When the lowest bit is 1, the packet has privileged access. For Avalon memory mapped interfaces, this field maps directly to the privileged access signal, which allows a memory-mapped master to write to an on-chip memory ROM instance. The other bits in this field support AXI secure accesses and use the same encoding, as described in the AXI specification.

### Command: QoS

QoS (Quality of Service Signaling) is a 4-bit field that is part of the AMBA 4 AXI interface that carries QoS information for the packet from the AXI master to the AXI slave. Transactions from AMBA 3 AXI and Avalon masters have the default value $4'b0000$, that indicates that they are not participating in the QoS scheme. QoS values are dropped for slaves that do not support QoS.

### Command: Data sideband

Carries data sideband signals for the packet. On a write command, the data sideband directly maps to WUSER. On a read response, the data sideband directly maps to RUSER. On a write response, the data sideband directly maps to BUSER.

### Table 35. Transaction Types for Memory-Mapped Interfaces

The table below describes the information that each bit transports in the packet format’s transaction field.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>PKT_TRANS_READ</td>
<td>When asserted, indicates a read transaction.</td>
</tr>
<tr>
<td>1</td>
<td>PKT_TRANS_COMPRESSED_READ</td>
<td>For read transactions, specifies whether the read command can be expressed in a single cycle (all byte enables asserted on every cycle).</td>
</tr>
<tr>
<td>2</td>
<td>PKT_TRANS_WRITE</td>
<td>When asserted, indicates a write transaction.</td>
</tr>
<tr>
<td>3</td>
<td>PKT_TRANS_POSTED</td>
<td>When asserted, no response is required.</td>
</tr>
<tr>
<td>4</td>
<td>PKT_TRANS_LOCK</td>
<td>When asserted, indicates arbitration is locked. Applies to write packets.</td>
</tr>
</tbody>
</table>
3.1.1.3. Platform Designer Transformations

The memory-mapped master and slave components connect to network interface modules that encapsulate the transaction in Avalon streaming packets. The memory-mapped interfaces have no information about the encapsulation or the function of the layer transporting the packets. The interfaces operate in accordance with memory-mapped protocol and use the read and write signals and transfers.

**Figure 83. Transformation when Generating a System with Memory-Mapped and Slave Components**

Platform Designer components that implement the blocks appear shaded.

![Diagram](image)

**Related Information**
- Master Network Interfaces on page 150
- Slave Network Interfaces on page 153

### 3.1.2. Interconnect Domains

An interconnect domain is a group of connected memory-mapped masters and slaves that share the same interconnect. The components in a single interconnect domain share the same packet format.

#### 3.1.2.1. Using One Domain with Width Adaptation

When one of the masters in a system connects to all the slaves, Platform Designer creates a single domain with two packet formats: one with 64-bit data, and one with 16-bit data. A width adapter manages accesses between the 16-bit master and 64-bit slaves.
Figure 84. **One Domain with 1:4 and 4:1 Width Adapters**

In this system example, there are two 64-bit masters that access two 64-bit slaves. It also includes one 16-bit master, that accesses two 16-bit slaves and two 64-bit slaves. The 16-bit Avalon master connects through a 1:4 adapter, then a 4:1 adapter to reach its 16-bit slaves.
3.1.2.2. Using Two Separate Domains

Figure 85. Two Separate Domains
In this system example, Platform Designer uses two separate domains. The first domain includes two 64-bit masters connected to two 64-bit slaves. A second domain includes one 16-bit master connected to two 16-bit slaves. Because the interfaces in Domain 1 and Domain 2 do not share any connections, Platform Designer can optimize the packet format for the two separate domains. In this example, the first domain uses a 64-bit data width and the second domain uses 16-bit data.

3.1.3. Master Network Interfaces

Figure 86. Avalon Memory Mapped Master Network Interface
Avalon network interfaces drive default values for the QoS and BUSER, WUSER, and RUSER packet fields in the master agent, and drop the packet fields in the slave agent.

Note: The response signal from the Limiter to the Agent is optional.
Figure 87. **AXI Master Network Interface**

An AMBA 4 AXI master supports INCR bursts up to 256 beats, QoS signals, and data sideband signals.

---

**Note:** For a complete definition of the optional read response signal, refer to *Avalon Memory-Mapped Interface Signal Types* in the *Avalon Interface Specifications*.

**Related Information**
- Avalon Interface Specifications
- Creating a System with Platform Designer on page 10

3.1.3.1. **Avalon Memory Mapped Master Agent**

The Avalon Memory Mapped Master Agent translates Avalon memory mapped master transactions into Platform Designer command packets and translates the Platform Designer Avalon memory mapped slave response packets into Avalon memory mapped responses.

3.1.3.2. **Avalon Memory Mapped Master Translator**

The Avalon Memory Mapped Master Translator interfaces with an Avalon memory mapped master component and converts the Avalon memory mapped master interface to a simpler representation for use in Platform Designer.

The Avalon Memory Mapped Master translator performs the following functions:
- Translates active-low signaling to active-high signaling
- Inserts wait states to prevent an Avalon memory mapped master from reading invalid data
- Translates word and symbol addresses
- Translates word and symbol burst counts
- Manages re-timing and re-sequencing bursts
- Removes unnecessary address bits

3.1.3.3. **AXI Master Agent**

An AXI Master Agent accepts AXI commands and produces Platform Designer command packets. It also accepts Platform Designer response packets and converts those into AXI responses. This component has separate packet channels for read
commands, write commands, read responses, and write responses. Avalon master agent drives the QoS and BUSER, WUSER, and RUSER packet fields with default values AXQ0 and b0000, respectively.

Note: For signal descriptions, refer to Platform Designer Packet Format.

Related Information
Fields in the Platform Designer Packet Format on page 146

3.1.3.4. AXI Translator

AMBA 4 AXI allows omitting signals from interfaces. The translator bridges between these “incomplete” AMBA 4 AXI interfaces and the “complete” AMBA 4 AXI interface on the network interfaces.

Attention: If an Avalon or AMBA 4 AXI slave is connected to a master without response ports, the interconnect could ignore transaction responses such as SLAVEERROR or DECODEERROR. This situation could lead to returning invalid data to the master.

The AXI translator is inserted for both AMBA 4 AXI masters and slaves and performs the following functions:

• Matches ID widths between the master and slave in 1x1 systems.
• Drives default values as defined in the AMBA Protocol Specifications for missing signals.
• Performs lock transaction bit conversion when an AMBA 3 AXI master connects to an AMBA 4 AXI slave in 1x1 systems.

Related Information
Arm AMBA Protocol Specifications

3.1.3.5. APB Master Agent

An APB master agent accepts APB commands and produces or generates Platform Designer command packets. It also converts Platform Designer response packets to APB responses.

3.1.3.6. APB Slave Agent

An APB slave agent issues resulting transaction to the APB interface. It also accepts creates Platform Designer response packets.

3.1.3.7. APB Translator

An APB peripheral does not require pslverr signals to support additional signals for the APB debug interface.

The APB translator is inserted for both the master and slave and performs the following functions:

• Sets the response value default to OKAY if the APB slave does not have a pslverr signal.
• Turns on or off additional signals between the APB debug interface, which is used with HPS (Intel SoC’s Hard Processor System).
3.1.3.8. AHB Slave Agent

The Platform Designer interconnect supports non-bursting Advanced High-performance Bus (AHB) slave interfaces.

3.1.3.9. Memory-Mapped Router

The Memory-Mapped Router routes command packets from the master to the slave, and response packets from the slave to the master. For master command packets, the router uses the address to set the Destination_ID and Avalon streaming channel. For the slave response packet, the router uses the Destination_ID to set the Avalon streaming channel. The demultiplexers use the Avalon streaming channel to route the packet to the correct destination.

3.1.3.10. Memory-Mapped Traffic Limiter

The Memory-Mapped Traffic Limiter ensures the responses arrive in order. It prevents any command from being sent if the response could conflict with the response for a command that has already been issued. By guaranteeing in-order responses, the Traffic Limiter simplifies the response network.

3.1.4. Slave Network Interfaces

3.1.4.1. Avalon Memory Mapped Slave Translator

The Avalon Memory Mapped Slave Translator converts the Avalon memory mapped slave interface to a simplified representation that the Platform Designer network can use.

Figure 88. Avalon Memory Mapped Slave Network Interface
An Avalon Memory Mapped Slave Translator performs the following functions:

- Drives the `beginbursttransfer` and `byteenable` signals.
- Supports Avalon memory mapped slaves that operate using fixed timing and or slaves that use the `readdatavalid` signal to identify valid data.
- Translates the `read`, `write`, and `chipselect` signals into the representation that the Avalon streaming slave response network uses.
- Converts active low signals to active high signals.
- Translates word and symbol addresses and burstcounts.
- Handles burstcount timing and sequencing.
- Removes unnecessary address bits.

**Related Information**

Slave Network Interfaces on page 153

### 3.1.4.2. AXI Translator

AMBA 4 AXI allows omitting signals from interfaces. The translator bridges between these "incomplete" AMBA 4 AXI interfaces and the "complete" AMBA 4 AXI interface on the network interfaces.

**Figure 89. AXI Slave Network Interface**

An AMBA 4 AXI slave supports up to 256 beat INCr bursts, QoS signals, and data sideband signals.

The AXI translator is inserted for both AMBA 4 AXI master and slave, and performs the following functions:

- Matches ID widths between master and slave in 1x1 systems.
- Drives default values as defined in the *AMBA Protocol Specifications* for missing signals.
- Performs lock transaction bit conversion when an AMBA 3 AXI master connects to an AMBA 4 AXI slave in 1x1 systems.
3.1.4.3. Wait State Insertion

Wait states extend the duration of a transfer by one or more cycles. Wait state insertion logic accommodates the timing needs of each slave, and causes the master to wait until the slave can proceed. Platform Designer interconnect inserts wait states into a transfer when the target slave cannot respond in a single clock cycle, as well as in cases when slave read and write signals have setup or hold time requirements.

Figure 90. Wait State Insertion Logic for One Master and One Slave

Wait state insertion logic is a small finite-state machine that translates control signal sequencing between the slave side and the master side. Platform Designer interconnect can force a master to wait for the wait state needs of a slave; for example, arbitration logic in a multi-master system. Platform Designer generates wait state insertion logic based on the properties of all slaves in the system.

3.1.4.4. Avalon Memory Mapped Slave Agent

The Avalon Memory Mapped Slave Agent accepts command packets and issues the resulting transactions to the Avalon interface. For pipelined slaves, an Avalon streaming FIFO stores information about pending transactions. The size of this FIFO is the maximum number of pending responses that you specify when creating the slave component. The Avalon Memory Mapped Slave Agent also backpressures the Avalon memory mapped master command interface when the FIFO is full if the slave component includes the waitrequest signal.

3.1.4.5. AXI Slave Agent

An AXI Slave Agent works like a reverse master agent. The AXI Slave Agent accepts Platform Designer command packets to create AXI commands, and accepts AXI responses to create Platform Designer response packets. This component has separate packet channels for read commands, write commands, read responses, and write responses.

3.1.5. Arbitration

When multiple masters contend for access to a slave, Platform Designer automatically inserts arbitration logic, which grants access in fairness-based, round-robin order. You can alternatively choose to designate a slave as a fixed priority arbitration slave, and then manually assign priorities in the Platform Designer GUI.

3.1.5.1. Round-Robin Arbitration

When multiple masters contend for access to a slave, Platform Designer automatically inserts arbitration logic which grants access in fairness-based, round-robin order.
In a fairness-based arbitration protocol, each master has an integer value of transfer shares with respect to a slave. One share represents permission to perform one transfer. The default arbitration scheme is equal share round-robin that grants equal, sequential access to all requesting masters. You can change the arbitration scheme to weighted round-robin by specifying a relative number of arbitration shares to the masters that access a given slave. AXI slaves have separate arbitration for their independent read and write channels, and the Arbitration Shares setting affects both the read and write arbitration. To display arbitration settings, right-click an instance on the System View tab, and then click Show Arbitration Shares.

Figure 91. Arbitration Shares in the Connections Column

<table>
<thead>
<tr>
<th>Connections</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mm_master_bfm_0_avalon</td>
<td>Altera UVM Avalon-MM Master BFM</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>n0</td>
<td>Avalon Memory Mapped Master</td>
<td></td>
</tr>
<tr>
<td>mm_master_bfm_1_axi</td>
<td>Altera AXI3 Master Module</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>alera_axi_master</td>
<td>AXI Master</td>
<td></td>
</tr>
<tr>
<td>mm_master_bfm_2_axi</td>
<td>Altera AXI3 Master Module</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>alera_axi_master</td>
<td>AXI Master</td>
<td></td>
</tr>
<tr>
<td>mm_slave_bfm_0_avalon</td>
<td>Altera UVM Avalon-MM Slave BFM</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>s0</td>
<td>Avalon Memory Mapped Slave</td>
<td></td>
</tr>
<tr>
<td>mm_slave_bfm_1_avalon</td>
<td>Altera UVM Avalon-MM Slave BFM</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>s0</td>
<td>Avalon Memory Mapped Slave</td>
<td></td>
</tr>
<tr>
<td>mm_slave_bfm_2_axi</td>
<td>Altera AXI Slave Module</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Input</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Input</td>
<td></td>
</tr>
<tr>
<td>alera_axi_slave</td>
<td>AXI Slave</td>
<td></td>
</tr>
<tr>
<td>CLOCK_0</td>
<td>Altera Avalon Clock and Reset Source</td>
<td></td>
</tr>
<tr>
<td>clk</td>
<td>Clock Output</td>
<td></td>
</tr>
<tr>
<td>clk_reset</td>
<td>Reset Output</td>
<td></td>
</tr>
<tr>
<td>dummy_src</td>
<td>Avalon Streaming Source</td>
<td></td>
</tr>
<tr>
<td>dummy_sink</td>
<td>Avalon Streaming Sink</td>
<td></td>
</tr>
</tbody>
</table>

3.1.5.1.1. Fairness-Based Shares

In a fairness-based arbitration scheme, each master-to-slave connection provides a transfer share count. This count is a request for the arbiter to grant a specific number of transfers to this master before giving control to a different master. One share represents permission to perform one transfer.
**Figure 92. Arbitration of Continuous Transfer Requests from Two Masters**

Consider a system with two masters connected to a single slave. Master 1 has its arbitration shares set to three, and Master 2 has its arbitration shares set to four. Master 1 and Master 2 continuously attempt to perform back-to-back transfers to the slave. The arbiter grants Master 1 access to the slave for three transfers, and then grants Master 2 access to the slave for four transfers. This cycle repeats indefinitely. The figure below describes the waveform for this scenario.

**Figure 93. Arbitration of Two Masters with a Gap in Transfer Requests**

If a master stops requesting transfers before it exhausts its shares, it forfeits all its remaining shares, and the arbiter grants access to another requesting master. After completing one transfer, Master 2 stops requesting for one clock cycle. As a result, the arbiter grants access back to Master 1, which gets a replenished supply of shares.

### 3.1.5.1.2. Round-Robin Scheduling

When multiple masters contend for access to a slave, the arbiter grants shares in round-robin order. Platform Designer includes only requesting masters in the arbitration for each slave transaction.

### 3.1.5.2. Fixed Priority Arbitration

Fixed priority arbitration is an alternative arbitration scheme to the default round-robin scheme.

You can selectively apply fixed priority arbitration to any slave in a Platform Designer system. You can design Platform Designer systems where a subset of slaves use the default round-robin arbitration, and other slaves use fixed priority arbitration. Fixed priority arbitration uses a fixed priority algorithm to grant access to a slave amongst its connected masters.

To set up fixed priority arbitration, you must first designate a fixed priority slave in your Platform Designer system in the **Interconnect Requirements** tab. You can then assign an arbitration priority number for each master connected to a fixed priority slave in the **System View** tab, where the highest numeric value receives the highest priority. When multiple masters request access to a fixed priority arbitrated slave, the arbiter gives the master with the highest priority first access to the slave.

For example, when a fixed priority slave receives requests from three masters on the same cycle, the arbiter grants the master with highest assigned priority first access to the slave, and backpressures the other two masters.
Note: When you connect an AXI master to an Avalon memory mapped slave designated to use a fixed priority arbitrator, the interconnect instantiates a command-path intermediary round-robin multiplexer in front of the designated slave.

3.1.5.2.1. Designate a Platform Designer Slave to Use Fixed Priority Arbitration

You can designate any slave in your Platform Designer system to use fixed priority arbitration. You must assign each master connected to a fixed priority slave a numeric priority. The master with the highest higher priority receives first access to the slave. No two masters can have the same priority.

1. In Platform Designer, navigate to the Interconnect Requirements tab.
2. Click Add to add a new requirement.
3. In the Identifier column, select the slave for fixed priority arbitration.
4. In the Setting column, select qsys mm.arbitrationScheme.
5. In the Value column, select fixed-priority.
7. In the System View tab, right-click the designated fixed priority slave, and then select Show Arbitration Shares.
8. For each master connected to the fixed priority arbitration slave, type a numerical arbitration priority in the box that appears in place of the connection circle.
9. Right click the designated fixed priority slave and uncheck Show Arbitration Shares to return to the connection circles.

3.1.5.2.2. Fixed Priority Arbitration with AXI Masters and Avalon Memory Mapped Slaves

When an AXI master is connected to a designated fixed priority arbitration Avalon memory mapped slave, Platform Designer interconnect automatically instantiates an intermediary multiplexer in front of the Avalon memory mapped slave.

Since AXI masters have separate read and write channels, each channel appears as two separate masters to the Avalon memory mapped slave. To support fairness between the AXI master's read and write channels, the instantiated round-robin intermediary multiplexer arbitrates between simultaneous read and write commands from the AXI master to the fixed-priority Avalon memory mapped slave.

When an AXI master is connected to a fixed priority AXI slave, the master's read and write channels are directly connected to the AXI slave's fixed-priority multiplexers. In this case, there is one multiplexer for the read command, and one multiplexer for the write command and therefore an intermediary multiplexer is not required.

The red circles indicate placement of the intermediary multiplexer between the AXI master and Avalon Memory Mapped slave due to the separate read and write channels of the AXI master.
3.1.6. Memory-Mapped Arbiter

The input to the Memory-Mapped Arbiter is the command packet for all masters requesting access to a specific slave. The arbiter outputs the channel number for the selected master. This channel number controls the output of a multiplexer that selects the slave device.
Arbitration Logic

In this example, four Avalon memory-mapped masters connect to four Avalon memory-mapped slaves. In each cycle, an arbiter positioned in front of each Avalon memory-mapped slave selects among the requesting Avalon memory-mapped masters.

Note: If you specify a Limit interconnect pipeline stages to parameter greater than zero, the output of the Arbiter is registered. Registering this output reduces the amount of combinational logic between the master and the interconnect, increasing the f\text{MAX} of the system.

Note: You can use the Memory-Mapped Arbiter for both round-robin and fixed priority arbitration.
3.1.7. Datapath Multiplexing Logic

Datapath multiplexing logic drives the `writedata` signal from the granted master to the selected slave, and the `readdata` signal from the selected slave back to the requesting master. Platform Designer generates separate datapath multiplexing logic for every master in the system (`readdata`), and for every slave in the system (`writedata`). Platform Designer does not generate multiplexing logic if it is not needed.

**Figure 96. Datapath Multiplexing Logic for One Master and Two Slaves**

![Datapath Multiplexing Logic Diagram]

3.1.8. Width Adaptation

Platform Designer width adaptation converts between Avalon memory-mapped master and slaves with different data and byte enable widths, and manages the run-time size requirements of AXI. Width adaptation for AXI to Avalon interfaces is also supported.

3.1.8.1. Memory-Mapped Width Adapter

The Memory-Mapped Width Adapter is used in the Avalon streaming domain and operates with information contained in the packet format.

The memory-mapped width adapter accepts packets on its sink interface with one data width and produces output packets on its source interface with a different data width. The ratio of the narrow data width must be a power of two, such as 1:4, 1:8, and 1:16. The ratio of the wider data width to the narrower width must also be a power of two, such as 4:1, 8:1, and 16:1. These output packets may have a different size if the input size exceeds the output data bus width, or if data packing is enabled.

When the width adapter converts from narrow data to wide data, each input beat's data and byte enables are copied to the appropriate segment of the wider output data and byte enables signals.
This adapter assumes that the field ordering of the input and output packets is the same, with the only
difference being the width of the data and accompanying byte enable fields. When the width adapter converts
from wide data to narrow data, the narrower data is transmitted over several beats. The first output beat
contains the lowest addressed segment of the input data and byte enables.

For all cases of AXI wide-to-narrow adaptation, read data is re-packed to match the
original size. Responses are merged, with the following error precedence: DECERR, SLVERR, OKAY, and EXOKAY.

<table>
<thead>
<tr>
<th>Burst Type</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Incrementing</td>
<td>If the transaction size is less than or equal to the output width, the burst is unmodified. Otherwise, it is converted to an incrementing burst with a larger length and size equal to the output width. If the resulting burst is unsuitable for the slave, the burst is converted to multiple sequential bursts of the largest allowable lengths. For example, for a 2:1 downsizing ratio, an INCR9 burst is converted into INCR16 + INCR2 bursts. This is true if the maximum burstcount a slave can accept is 16, which is the case for AMBA 3 AXI slaves. Avalon slaves have a maximum burstcount of 64.</td>
</tr>
<tr>
<td>Wrapping</td>
<td>If the transaction size is less than or equal to the output width, the burst is unmodified. Otherwise, it is converted to a wrapping burst with a larger length, with a size equal to the output width. If the resulting burst is unsuitable for the slave, the burst is converted to multiple sequential bursts of the largest allowable lengths; respecting wrap boundaries. For example, for a 2:1 downsizing ratio, a WRAP16 burst is converted into two or three INCR bursts, depending on the address.</td>
</tr>
<tr>
<td>Fixed</td>
<td>If the transaction size is less than or equal to the output width, the burst is unmodified. Otherwise, it is converted into repeated sequential bursts over the same addresses. For example, for a 2:1 downsizing ratio, a FIXED single burst is converted into an INCR2 burst.</td>
</tr>
</tbody>
</table>
3.1.8.1.2. AXI Narrow-to-Wide Adaptation

Table 37. AXI Narrow-to-Wide Adaptation (Upsizing)

<table>
<thead>
<tr>
<th>Burst Type</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Incrementing</td>
<td>The burst (and its response) passes through unmodified. Data and write strobes are placed in the correct output segment.</td>
</tr>
<tr>
<td>Wrapping</td>
<td>The burst (and its response) passes through unmodified.</td>
</tr>
<tr>
<td>Fixed</td>
<td>The burst (and its response) passes through unmodified.</td>
</tr>
</tbody>
</table>

3.1.9. Burst Adapter

Platform Designer interconnect uses the memory-mapped burst adapter to accommodate the burst capabilities of each interface in the system, including interfaces that do not support burst transfers.

The maximum burst length for each interface is a property of the interface and is independent of other interfaces in the system. Therefore, a specific master may be capable of initiating a burst longer than a slave’s maximum supported burst length. In this case, the burst adapter translates the large master burst into smaller bursts, or into individual slave transfers if the slave does not support bursting. Until the master completes the burst, arbiter logic prevents other masters from accessing the target slave. For example, if a master initiates a burst of 16 transfers to a slave with maximum burst length of 8, the burst adapter initiates 2 bursts of length 8 to the slave.

Avalon memory mapped and AXI burst transactions allow a master uninterrupted access to a slave for a specified number of transfers. The master specifies the number of transfers when it initiates the burst. Once a burst begins between a master and slave, arbiter logic is locked until the burst completes. For burst masters, the length of the burst is the number of cycles that the master has access to the slave, and the selected arbitration shares have no effect.

Note: AXI masters can issue burst types that Avalon cannot accept, for example, fixed bursts. In this case, the burst adapter converts the fixed burst into a sequence of transactions to the same address.

Note: For AMBA 4 AXI slaves, Platform Designer allows 256-beat INCR bursts. You must ensure that 256-beat narrow-sized INCR bursts are shortened to 16-beat narrow-sized INCR bursts for AMBA 3 AXI slaves.

Avalon memory mapped masters always issue addresses that are aligned to the size of the transfer. However, when Platform Designer uses a narrow-to-wide width adaptation, the resulting address may be unaligned. For unaligned addresses, the burst adapter issues the maximum sized bursts with appropriate byte enables. This brings the burst-in-progress up to an aligned slave address. Then, it completes the burst on aligned addresses.

The burst adapter supports variable wrap or sequential burst types to accommodate different properties of memory-mapped masters. Some bursting masters can issue more than one burst type.

Burst adaptation is available for Avalon to Avalon, Avalon to AXI, and AXI to Avalon, and AXI to AXI connections. For information about AXI-to-AXI adaptation, refer to AXI Wide-to-Narrow Adaptation.
Note: For AMBA 4 AXI to AMBA 3 AXI connections, Platform Designer follows an AMBA 4 AXI 256 burst length to AMBA 3 AXI 16 burst length.

3.1.9.1. Burst Adapter Implementation Options

Platform Designer automatically inserts burst adapters into your system depending on your master and slave connections, and properties. You can select burst adapter implementation options on the Interconnect Requirements tab.

To access the implementation options, you must select the Burst adapter implementation setting for the $system identifier.

- **Generic converter (slower, lower area)**—Default. Controls all burst conversions with a single converter that can adapt incoming burst types. This results in an adapter that has lower $f_{\text{MAX}}$, but smaller area.
- **Per-burst-type converter (faster, higher area)**—Controls incoming bursts with a specific converter, depending on the burst type. This results in an adapter that has higher $f_{\text{MAX}}$, but higher area. This setting is useful when you have AXI masters or slaves and you want a higher $f_{\text{MAX}}$.

Note: For more information about the Interconnect Requirements tab, refer to Creating a System with Platform Designer.

Related Information
Creating a System with Platform Designer on page 10

3.1.9.2. Burst Adaptation: AXI to Avalon

The following entries specify the behavior when converting between AXI and Avalon burst types.

### Table 38. Burst Adaptation: AXI to Avalon

<table>
<thead>
<tr>
<th>Burst Type</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Incrementing</td>
<td><strong>Sequential Slave</strong>&lt;br&gt;Bursts that exceed slave_max_burst_length are converted to multiple sequential bursts of a length less than or equal to the slave_max_burst_length. Otherwise, the burst is unconverted. For example, for an Avalon slave with a maximum burst length of 4, an INCR7 burst is converted to INCR4 + INCR3. <strong>Wrapping Slave</strong>&lt;br&gt;Bursts that exceed the slave_max_burst_length are converted to multiple sequential bursts of length less than or equal to the slave_max_burst_length. Bursts that exceed the wrapping boundary are converted to multiple sequential bursts that respect the slave's wrapping boundary.</td>
</tr>
<tr>
<td>Wrapping</td>
<td><strong>Sequential Slave</strong>&lt;br&gt;A WRAP burst is converted to multiple sequential bursts. The sequential bursts are less than or equal to the max_burst_length and respect the transaction's wrapping boundary <strong>Wrapping Slave</strong>&lt;br&gt;If the WRAP transaction's boundary matches the slave's boundary, then the burst passes through. Otherwise, the burst is converted to sequential bursts that respect both the transaction and slave wrap boundaries.</td>
</tr>
<tr>
<td>Fixed</td>
<td>Fixed bursts are converted to sequential bursts of length 1 that repeatedly access the same address.</td>
</tr>
<tr>
<td>Narrow</td>
<td>All narrow-sized bursts are broken into multiple bursts of length 1.</td>
</tr>
</tbody>
</table>
3.1.9.3. Burst Adaptation: Avalon to AXI

The following entries specify the behavior when converting between Avalon and AXI burst types.

Note: The Platform Designer-generated interconnect that adapts between an Avalon memory-mapped interface master and a connected AXI slave does not account for the AXI3 or AXI4 4KB boundary restriction for burst transactions. When connecting an Avalon memory-mapped interface FPGA master to an AXI slave in Platform Designer, you must ensure that the bursts do not exceed the AXI3 or AXI4 4KB boundary restriction for burst transactions.

Table 39. Burst Adaptation: Avalon to AXI

<table>
<thead>
<tr>
<th>Burst Type</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sequential</td>
<td>Bursts of length greater than 16 are converted to multiple INCR bursts of a length less than or equal to 16. Bursts of length less than or equal to 16 are not converted.</td>
</tr>
<tr>
<td>Wrapping</td>
<td>Only Avalon masters with alwaysBurstMaxBurst = true are supported. The WRAP burst is passed through if the length is less than or equal to 16. Otherwise, it is converted to two or more INCR bursts that respect the transaction’s wrap boundary.</td>
</tr>
<tr>
<td>GENERIC_CONVERTER</td>
<td>Controls all burst conversions with a single converter that adapts all incoming burst types, resulting in an adapter that has smaller area, but lower fMAX.</td>
</tr>
</tbody>
</table>

3.1.10. Waitrequest Allowance Adapter

The Waitrequest Allowance Adapter allows a connection between a master and a slave interface with different waitrequestAllowance properties.

The Waitrequest Allowance adapter provides the following features:

- The adapter is used in the memory-mapped domain and operates with signals on the memory-mapped interface.
- Signal widths and all properties other than waitrequestAllowance are identical on master and slave interfaces.
- The adapter does not modify any command properties such as data width, burst type, or burst count.
- The adapter is inserted by the Platform Designer interconnect software when a master and slave with different waitrequestAllowance property are connected.

When the slave has a waitrequestAllowance = n the master must deassert read or write signals after <n> transfers when waitrequest is asserted.

Table 40. Interconnect Scenarios Requiring waitrequestAllowance

<table>
<thead>
<tr>
<th>Master (m) / Slave (n) waitrequestAllowance</th>
<th>Adaptation Required</th>
<th>Description</th>
<th>Adapter Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>m = n</td>
<td>No</td>
<td>The master waitrequestAllowance is equal to the slave’s waitrequestAllowance.</td>
<td>All signals are passed through.</td>
</tr>
<tr>
<td>m = 0; n &gt; 0</td>
<td>Yes</td>
<td>The master cannot send when waitrequest=1, but holds the value on the bus. This would result in the slave receiving multiple copies.</td>
<td>The adapter deasserts valid when input waitrequest is asserted.</td>
</tr>
</tbody>
</table>

continued...
3.1.11. Read and Write Responses

Platform Designer merges write responses if a write is converted (burst adapted) into multiple bursts. Platform Designer requires read response merging for a downsized (wide-to-narrow width adapted) read.

Platform Designer merges responses based on the following precedence rule:

<table>
<thead>
<tr>
<th>DECERR</th>
<th>SLVERR</th>
<th>OKAY</th>
<th>EXOKAY</th>
</tr>
</thead>
</table>

Adaptation between a master with write responses and a slave without write responses can be costly, especially if there are multiple slaves, or if the slave supports bursts. To minimize the cost of logic between slaves, consider placing the slaves that do not have write responses behind a bridge so that the write response adaptation logic cost is only incurred once, at the bridge’s slave interface.

The following table describes what happens when there is a mismatch in response support between the master and slave.

**Table 41. Response Support for Mismatched Master and Slave**

<table>
<thead>
<tr>
<th>Master with Response</th>
<th>Slave with Response</th>
<th>Slave Without Response</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Interconnect delivers response from the slave to the master. Response merging or duplication may be necessary for bus sizing.</td>
<td>Interconnect delivers an OKAY response to the master</td>
</tr>
<tr>
<td>Master without Response</td>
<td>Master ignores responses from the slave</td>
<td>No need for responses. Master, slave and interconnect operate without response support.</td>
</tr>
</tbody>
</table>
Note: If there is a bridge between the master and the endpoint slave, and the responses must come from the endpoint slave, ensure that the bridge passes the appropriate response signals through from the endpoint slave to the master.

If the bridge does not support responses, then the responses are generated by the interconnect at the slave interface of the bridge, and responses from the endpoint slave are ignored.

For the response case where the transaction violates security settings or uses an illegal address, the interconnect routes the transactions to the default slave. For information about Platform Designer system security, refer to Manage System Security. For information about specifying a default slave, refer to Error Response Slave in Platform Designer System Design Components.

Note: Avalon memory mapped slaves without a response signal are not able to notify a connected master that a transaction has not completed successfully. As a result, Platform Designer interconnect generates an OKAY response on behalf of the Avalon memory mapped slave.

Related Information
- Master Network Interfaces on page 150
- Error Response Slave Intel FPGA IP on page 325
- Error Correction Coding (ECC) in Platform Designer Interconnect on page 222

3.1.12. Platform Designer Address Decoding

Address decoding logic forwards appropriate addresses to each slave.

Address decoding logic simplifies component design in the following ways:
- The interconnect selects a slave whenever it is being addressed by a master. Slave components do not need to decode the address to determine when they are selected.
- Slave addresses are properly aligned to the slave interface.
- Changing the system memory map does not involve manually editing HDL.

Figure 98. Address Decoding for One Master and Two Slaves

In this example, Platform Designer generates separate address decoding logic for each master in a system. The address decoding logic processes the difference between the master address width (<M>) and the individual slave address widths (<S> and <T>). The address decoding logic also maps only the necessary master address bits to access words in each slave's address space.
Platform Designer controls the base addresses with the **Base** setting of active components on the **System View** tab. The base address of a slave component must be a multiple of the address span of the component. This restriction is part of the Platform Designer interconnect to allow the address decoding logic to be efficient, and to achieve the best possible $f_{\text{MAX}}$.

**Figure 99. Address Decoding Base Settings**

3.2. Avalon Streaming Interfaces

High bandwidth components with streaming data typically use Avalon streaming interfaces for the high throughput datapath. Streaming interfaces can also use memory-mapped connection interfaces to provide an access point for control. In contrast to the memory-mapped interconnect, the Avalon streaming interconnect always creates a point-to-point connection between a single data source and data sink.
**Figure 100. Avalon Memory-Mapped and Avalon Streaming Interfaces**

In this example, there are the following connection pairs:

- Data source in the Rx Interface transfers data to the data sink in the FIFO.
- Data source in the FIFO transfers data to the Tx Interface data sink.

The memory-mapped interface allows a processor to access the data source, FIFO, or data sink to provide system control. If your source and sink interfaces have different formats, for example, a 32-bit source and an 8-bit sink, Platform Designer automatically inserts the necessary adapters. You can view the adapters on the System View tab by clicking System ▶ Show System with Platform Designer Interconnect.

**Figure 101. Avalon Streaming Connection Between the Source and Sink**

This source-sink pair includes only the data signal. The sink must be able to receive data as soon as the source interface comes out of reset.
Figure 102. Signals Indicating the Start and End of Packets, Channel Numbers, Error Conditions, and Backpressure

All data transfers using Avalon streaming interconnect occur synchronously on the rising edge of the associated clock interface. Throughput and frequency of a system depends on the components and how they are connected.

The IP Catalog includes Avalon streaming components that you can use to create datapaths, including datapaths whose input and output streams have different properties. Generated systems that include memory-mapped master and slave components may also use these Avalon streaming components because Platform Designer generation creates interconnect with a structure similar to a network topology, as described in Platform Designer Transformations. The following sections introduce the Avalon streaming components.

Related Information
Platform Designer Transformations on page 148

3.2.1. Avalon Streaming Adapters

Platform Designer automatically adds Avalon streaming adapters between two components during system generation when it detects mismatched interfaces. If you connect mismatched Avalon streaming sources and sinks, for example, a 32-bit source and an 8-bit sink, Platform Designer inserts the appropriate adapter type to connect the mismatched interfaces.

After generation, you can view the inserted adapters selecting System ➤ Show System With Platform Designer Interconnect. For each mismatched source-sink pair, Platform Designer inserts an Avalon streaming adapter. The adapter instantiates the necessary adaptation logic as sub-components. You can review the logic for each adapter instantiation in the Hierarchy view by expanding each adapter’s source and sink interface and comparing the relevant ports. For example, to determine why a channel adapter is inserted, expand the channel adapter’s sink and source interfaces and review the channel port properties for each interface.

You can turn off the auto-inserted adapters feature by adding the qsys_enable_avalon_streaming_transform=off command to the quartus.ini file. When you turn off the auto-inserted adapters feature, if mismatched interfaces are detected during system generation, Platform Designer does not insert adapters and reports the mismatched interface with validation error message.
3. Platform Designer Interconnect

Note: The auto-inserted adapters feature does not work for video IP connections.

3.2.1.1. Avalon Streaming Adapter

The Avalon streaming adapter combines the logic of the channel, error, data format, and timing adapters. The Avalon streaming adapter provides adaptations between interfaces that have mismatched Avalon streaming endpoints. Based on the source and sink interface parameterizations for the Avalon streaming adapter, Platform Designer instantiates the necessary adapter logic (channel, error, data format, or timing) as hierarchal sub-components.

3.2.1.1.1. Avalon Streaming Adapter Parameters Common to Source and Sink Interfaces

Table 42. Avalon Streaming Adapter Parameters Common to Source and Sink Interfaces

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Width</td>
<td>Width of a single symbol in bits.</td>
</tr>
<tr>
<td>Use Packet</td>
<td>Indicates whether the source and sink interfaces connected to the adapter's source and sink interfaces include the startofpacket and endofpacket signals, and the optional empty signal.</td>
</tr>
</tbody>
</table>

3.2.1.1.2. Avalon Streaming Adapter Upstream Source Interface Parameters

Table 43. Avalon Streaming Adapter Upstream Source Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Data Width</td>
<td>Controls the data width of the source interface data port.</td>
</tr>
<tr>
<td>Source Top Channel</td>
<td>Maximum number of output channels allowed.</td>
</tr>
<tr>
<td>Source Channel Port Width</td>
<td>Sets the bit width of the source interface channel port. If set to 0, there is no channel port on the sink interface.</td>
</tr>
<tr>
<td>Source Error Port Width</td>
<td>Sets the bit width of the source interface error port. If set to 0, there is no error port on the sink interface.</td>
</tr>
<tr>
<td>Source Error Descriptors</td>
<td>A list of strings that describe the error conditions for each bit of the source interface error signal.</td>
</tr>
<tr>
<td>Source Uses Empty Port</td>
<td>Indicates whether the source interface includes the empty port, and whether the sink interface should also include the empty port.</td>
</tr>
<tr>
<td>Source Empty Port Width</td>
<td>Indicates the bit width of the source interface empty port, and sets the bit width of the sink interface empty port.</td>
</tr>
<tr>
<td>Source Uses Valid Port</td>
<td>Indicates whether the source interface connected to the sink interface uses the valid port, and if set, configures the sink interface to use the valid port.</td>
</tr>
<tr>
<td>Source Uses Ready Port</td>
<td>Indicates whether the sink interface uses the ready port, and if set, configures the source interface to use the ready port.</td>
</tr>
<tr>
<td>Source Ready Latency</td>
<td>Specifies what ready latency to expect from the source interface connected to the adapter's sink interface.</td>
</tr>
</tbody>
</table>
3.2.1.1.3. Avalon Streaming Adapter Downstream Sink Interface Parameters

Table 44. Avalon Streaming Adapter Downstream Sink Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sink Data Width</td>
<td>Indicates the bit width of the data port on the sink interface connected to the source interface.</td>
</tr>
<tr>
<td>Sink Top Channel</td>
<td>Maximum number of output channels allowed.</td>
</tr>
<tr>
<td>Sink Channel Port Width</td>
<td>Indicates the bit width of the channel port on the sink interface connected to the source interface.</td>
</tr>
<tr>
<td>Sink Error Port Width</td>
<td>Indicates the bit width of the error port on the sink interface connected to the adapter's source interface. If set to zero, there is no error port on the source interface.</td>
</tr>
<tr>
<td>Sink Error Descriptors</td>
<td>A list of strings that describe the error conditions for each bit of the error port on the sink interface connected to the source interface.</td>
</tr>
<tr>
<td>Sink Uses Empty Port</td>
<td>Indicates whether the sink interface connected to the source interface uses the empty port, and whether the source interface should also use the empty port.</td>
</tr>
<tr>
<td>Sink Empty Port Width</td>
<td>Indicates the bit width of the empty port on the sink interface connected to the source interface, and configures a corresponding empty port on the source interface.</td>
</tr>
<tr>
<td>Sink Uses Valid Port</td>
<td>Indicates whether the valid port on the sink interface is connected to the source interface, and if set, configures the source interface to use the valid port.</td>
</tr>
<tr>
<td>Sink Uses Ready Port</td>
<td>Indicates whether the ready port on the sink interface is connected to the source interface, and if set, configures the sink interface to use the ready port.</td>
</tr>
<tr>
<td>Sink Ready Latency</td>
<td>Specifies what ready latency to expect from the source interface connected to the sink interface.</td>
</tr>
</tbody>
</table>

3.2.1.2. Channel Adapter

The channel adapter provides adaptations between interfaces that have different channel signal widths.

Table 45. Channel Adapter Adaptations

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description of Adapter Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>The source uses channels, but the sink does not.</td>
<td>Platform Designer gives a warning at generation time. The adapter provides a simulation error and signals an error for data for any channel from the source other than 0.</td>
</tr>
<tr>
<td>The sink has channel, but the source does not.</td>
<td>Platform Designer gives a warning at generation time, and the channel inputs to the sink are all tied to a logical 0.</td>
</tr>
<tr>
<td>The source and sink both support channels, and the source’s maximum channel number is less than the sink’s maximum channel number.</td>
<td>The source’s channel is connected to the sink’s channel unchanged. If the sink’s channel signal has more bits, the higher bits are tied to a logical 0.</td>
</tr>
</tbody>
</table>
| The source and sink both support channels, but the source’s maximum channel number is greater than the sink’s maximum channel number. | The source’s channel is connected to the sink’s channel unchanged. If the source’s channel signal has more bits, the higher bits are left unconnected. Platform Designer gives a warning that channel information may be lost.  
An adapter provides a simulation error message and an error indication if the value of channel from the source is greater than the sink’s maximum number of channels.  
In addition, the valid signal to the sink is deasserted so that the sink never sees data for channels that are out of range. |
3.2.1.2.1. Avalon Streaming Channel Adapter Input Interface Parameters

Table 46. Avalon Streaming Channel Adapter Input Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Signal Width (bits)</td>
<td>Width of the input channel signal in bits</td>
</tr>
<tr>
<td>Max Channel</td>
<td>Maximum number of input channels allowed.</td>
</tr>
</tbody>
</table>

3.2.1.2.2. Avalon Streaming Channel Adapter Output Interface Parameters

Table 47. Avalon Streaming Channel Adapter Output Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Signal Width (bits)</td>
<td>Width of the output channel signal in bits</td>
</tr>
<tr>
<td>Max Channel</td>
<td>Maximum number of output channels allowed.</td>
</tr>
</tbody>
</table>

3.2.1.2.3. Avalon Streaming Channel Adapter Common to Input and Output Interface Parameters

Table 48. Avalon Streaming Channel Adapter Common to Input and Output Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Bits Per Symbol</td>
<td>Number of bits for each symbol in a transfer.</td>
</tr>
<tr>
<td>Include Packet Support</td>
<td>When the Avalon Streaming Channel adapter supports packets, the startofpacket, endofpacket, and optional empty signals are included on its sink and source interfaces.</td>
</tr>
<tr>
<td>Include Empty Signal</td>
<td>Indicates whether an empty signal is required.</td>
</tr>
<tr>
<td>Data Symbols Per Beat</td>
<td>Number of symbols per transfer.</td>
</tr>
<tr>
<td>Support Backpressure with the ready signal</td>
<td>Indicates whether a ready signal is required.</td>
</tr>
<tr>
<td>Ready Latency</td>
<td>Specifies the ready latency to expect from the sink connected to the module's source interface.</td>
</tr>
<tr>
<td>Error Signal Width (bits)</td>
<td>Bit width of the error signal.</td>
</tr>
<tr>
<td>Error Signal Description</td>
<td>A list of strings that describes what each bit of the error signal represents.</td>
</tr>
</tbody>
</table>

3.2.1.3. Data Format Adapter

The data format adapter allows you to connect interfaces that have different values for the parameters defining the data signal, or interfaces where the source does not use the empty signal, but the sink does use the empty signal. One of the most common uses of this adapter is to convert data streams of different widths.

Table 49. Data Format Adapter Adaptations

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description of Adapter Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>The source and sink’s bits per symbol parameters are different.</td>
<td>The connection cannot be made.</td>
</tr>
<tr>
<td>The source and sink have a different number of symbols per beat.</td>
<td>The adapter converts the source’s width to the sink’s width.</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Condition</th>
<th>Description of Adapter Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>If the adaptation is from a wider to a narrower interface, a beat of data at the input corresponds to multiple beats of data at the output. If the input error signal is asserted for a single beat, it is asserted on output for multiple beats. If the adaptation is from a narrow to a wider interface, multiple input beats are required to fill a single output beat, and the output error is the logical OR of the input error signal.</td>
<td></td>
</tr>
<tr>
<td>The source uses the empty signal, but the sink does not use the empty signal.</td>
<td>Platform Designer cannot make the connection.</td>
</tr>
</tbody>
</table>

**Figure 103. Avalon Streaming Interconnect with Data Format Adapter**

In this example, the data format adapter allows a connection between a 128-bit output data stream and three 32-bit input data streams.

### 3.2.1.3.1. Avalon Streaming Data Format Adapter Input Interface Parameters

**Table 50. Avalon Streaming Data Format Adapter Input Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Symbols Per Beat</td>
<td>Number of symbols per transfer.</td>
</tr>
<tr>
<td>Include Empty Signal</td>
<td>Indicates whether an empty signal is required.</td>
</tr>
</tbody>
</table>

### 3.2.1.3.2. Avalon Streaming Data Format Adapter Output Interface Parameters

**Table 51. Avalon Streaming Data Format Adapter Output Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Symbols Per Beat</td>
<td>Number of symbols per transfer.</td>
</tr>
<tr>
<td>Include Empty Signals</td>
<td>Indicates whether an empty signal is required.</td>
</tr>
</tbody>
</table>
3.2.1.3.3. Avalon Streaming Data Format Adapter Common to Input and Output Interface Parameters

Table 52. Avalon Streaming Data Format Adapter Common to Input and Output Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Bits Per Symbol</td>
<td>Number of bits for each symbol in a transfer.</td>
</tr>
<tr>
<td>Include Packet Support</td>
<td>When the Avalon Streaming Data Format adapter supports packets, Platform</td>
</tr>
<tr>
<td></td>
<td>Designer uses startofpacket, endofpacket, and empty signals.</td>
</tr>
<tr>
<td>Channel Signal Width (bits)</td>
<td>Width of the output channel signal in bits.</td>
</tr>
<tr>
<td>Max Channel</td>
<td>Maximum number of channels allowed.</td>
</tr>
<tr>
<td>Read Latency</td>
<td>Specifies the ready latency to expect from the sink connected to the module's</td>
</tr>
<tr>
<td></td>
<td>source interface.</td>
</tr>
<tr>
<td>Error Signal Width (bits)</td>
<td>Width of the error signal output in bits.</td>
</tr>
<tr>
<td>Error Signal Description</td>
<td>A list of strings that describes what each bit of the error signal represents.</td>
</tr>
</tbody>
</table>

3.2.1.4. Error Adapter

The error adapter ensures that per-bit-error information provided by the source interface is correctly connected to the sink interface’s input error signal. Error conditions that both source and sink can process are connected. If the source has an error signal representing an error condition that is not supported by the sink, the signal is left unconnected; the adapter provides a simulation error message and an error indication if the error is asserted. If the sink has an error condition that is not supported by the source, the sink’s input error bit corresponding to that condition is set to 0.

Note: The output interface error signal descriptor accepts an error set with an other descriptor. Platform Designer assigns the bit-wise ORing of all input error bits that are unmatched, to the output interface error bits set with the other descriptor.

3.2.1.4.1. Avalon Streaming Error Adapter Input Interface Parameters

Table 53. Avalon Streaming Error Adapter Input Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error Signal Width (bits)</td>
<td>The width of the error signal. Valid values are 0–256 bits. Type 0 if the error signal is not used.</td>
</tr>
<tr>
<td>Error Signal Description</td>
<td>The description for each of the error bits. If scripting, separate the description fields by commas. For a successful connection, the description strings of the error bits in the source and sink must match and are case sensitive.</td>
</tr>
</tbody>
</table>
3.2.1.4.2. Avalon Streaming Error Adapter Output Interface Parameters

Table 54. Avalon Streaming Error Adapter Output Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error Signal Width (bits)</td>
<td>The width of the error signal. Valid values are 0–256 bits. Type 0 if you do not need to send error values.</td>
</tr>
<tr>
<td>Error Signal Description</td>
<td>The description for each of the error bits. Separate the description fields by commas. For successful connection, the description of the error bits in the source and sink must match, and are case sensitive.</td>
</tr>
</tbody>
</table>

3.2.1.4.3. Avalon Streaming Error Adapter Common to Input and Output Interface Parameters

Table 55. Avalon Streaming Error Adapter Common to Input and Output Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Support Backpressure with the ready signal</td>
<td>Turn on this option to add the backpressure functionality to the interface.</td>
</tr>
<tr>
<td>Ready Latency</td>
<td>When the ready signal is used, the value for ready_latency indicates the number of cycles between when the ready signal is asserted and when valid data is driven.</td>
</tr>
<tr>
<td>Channel Signal Width (bits)</td>
<td>The width of the channel signal. A channel width of 4 allows up to 16 channels. The maximum width of the channel signal is eight bits. Set to 0 if channels are not used.</td>
</tr>
<tr>
<td>Max Channel</td>
<td>The maximum number of channels that the interface supports. Valid values are 0–255.</td>
</tr>
<tr>
<td>Data Bits Per Symbol</td>
<td>Number of bits per symbol.</td>
</tr>
<tr>
<td>Data Symbols Per Beat</td>
<td>Number of symbols per active transfer.</td>
</tr>
<tr>
<td>Include Packet Support</td>
<td>Turn on this option if the connected interfaces support a packet protocol, including the startofpacket, endofpacket and empty signals.</td>
</tr>
<tr>
<td>Include Empty Signal</td>
<td>Turn this option on if the cycle that includes the endofpacket signal can include empty symbols. This signal is not necessary if the number of symbols per beat is 1.</td>
</tr>
</tbody>
</table>

3.2.1.5. Timing Adapter

The timing adapter allows you to connect component interfaces that require a different number of cycles before driving or receiving data. This adapter inserts a FIFO buffer between the source and sink to buffer data or pipeline stages to delay the back-pressure signals. You can also use the timing adapter to connect interfaces that support the ready signal, and those that do not. The timing adapter treats all signals other than the ready and valid signals as payload, and simply drives them from the source to the sink.
### Table 56. Timing Adapter Adaptations

<table>
<thead>
<tr>
<th>Condition</th>
<th>Adaptation</th>
</tr>
</thead>
<tbody>
<tr>
<td>The source has \texttt{ready}, but the sink does not.</td>
<td>In this case, the source can respond to \texttt{backpressure}, but the sink never needs to apply it. The \texttt{ready} input to the source interface is connected directly to logical 1.</td>
</tr>
<tr>
<td>The source does not have \texttt{ready}, but the sink does.</td>
<td>The sink may apply \texttt{backpressure}, but the source is unable to respond to it. There is no logic that the adapter can insert that prevents data loss when the source asserts \texttt{valid} but the sink is not ready. The adapter provides simulation time error messages if data is lost. The user is presented with a warning, and the connection is allowed.</td>
</tr>
<tr>
<td>The source and sink both support \texttt{backpressure}, but the sink’s \texttt{ready} latency is greater than the source’s.</td>
<td>The source responds to \texttt{ready} assertion or deassertion faster than the sink requires it. The number of pipeline stages equal to the difference in \texttt{ready} latency are inserted in the \texttt{ready} path from the sink back to the source, causing the source and the sink to see the same cycles as \texttt{ready} cycles.</td>
</tr>
<tr>
<td>The source and sink both support \texttt{backpressure}, but the sink’s \texttt{ready} latency is less than the source’s.</td>
<td>The source cannot respond to \texttt{ready} assertion or deassertion in time to satisfy the sink. A FIFO whose depth is equal to the difference in \texttt{ready} latency is inserted to compensate for the source’s inability to respond in time.</td>
</tr>
</tbody>
</table>

### 3.2.1.5.1. Avalon Streaming Timing Adapter Input Interface Parameters

**Table 57. Avalon Streaming Timing Adapter Input Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Support Backpressure with the \texttt{ready} signal</td>
<td>Indicates whether a \texttt{ready} signal is required.</td>
</tr>
<tr>
<td>Read Latency</td>
<td>Specifies the \texttt{ready} latency to expect from the sink connected to the module’s source interface.</td>
</tr>
<tr>
<td>Include Valid Signal</td>
<td>Indicates whether the sink interface requires a valid signal.</td>
</tr>
</tbody>
</table>

### 3.2.1.5.2. Avalon Streaming Timing Adapter Output Interface Parameters

**Table 58. Avalon Streaming Timing Adapter Output Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Support Backpressure with the \texttt{ready} signal</td>
<td>Indicates whether a \texttt{ready} signal is required.</td>
</tr>
<tr>
<td>Read Latency</td>
<td>Specifies the \texttt{ready} latency to expect from the sink connected to the module’s source interface.</td>
</tr>
<tr>
<td>Include Valid Signal</td>
<td>Indicates whether the sink interface requires a valid signal.</td>
</tr>
</tbody>
</table>

### 3.2.1.5.3. Avalon Streaming Timing Adapter Common to Input and Output Interface Parameters

**Table 59. Avalon Streaming Timing Adapter Common to Input and Output Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Bits Per Symbol</td>
<td>Number of bits for each symbol in a transfer.</td>
</tr>
<tr>
<td>Include Packet Support</td>
<td>Turn this option on if the connected interfaces support a packet protocol, including the startofpacket, endofpacket and empty signals.</td>
</tr>
<tr>
<td>Include Empty Signal</td>
<td>Turn this option on if the cycle that includes the endofpacket signal can include empty symbols. This signal is not necessary if the number of symbols per beat is 1.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Symbols Per Beat</td>
<td>Number of symbols per active transfer.</td>
</tr>
<tr>
<td>Channel Signal Width (bits)</td>
<td>Width of the output channel signal in bits.</td>
</tr>
<tr>
<td>Max Channel</td>
<td>Maximum number of output channels allowed.</td>
</tr>
<tr>
<td>Error Signal Width (bits)</td>
<td>Width of the output error signal in bits.</td>
</tr>
<tr>
<td>Error Signal Description</td>
<td>A list of strings that describes errors.</td>
</tr>
</tbody>
</table>
3.3. Avalon Streaming Credit Interfaces

Avalon Streaming Credit interfaces are for use with components that drive high-bandwidth, low-latency, unidirectional data. Typical applications include multiplexed streams, packets, and DSP data. The Avalon Streaming Credit interface signals can describe traditional streaming interfaces supporting a single stream of data, without knowledge of channels or packet boundaries. The interface can also support more complex protocols capable of burst and packet transfers with packets interleaved across multiple channels.

All Avalon Streaming Credit source and sink interfaces are not necessarily interoperable. However, if two interfaces provide compatible functions for the same application space, adapters are available to allow them to interoperate.

You can also connect the Avalon Streaming Credit source to an Avalon Streaming sink via an adapter. Similarly, you can connect an Avalon Streaming source to an Avalon Streaming Credit sink via an adapter.

Avalon Streaming Credit interfaces support datapaths requiring the following features:

- Low-latency, high-throughput point-to-point data transfer
- Multiple channels support with flexible packet interleaving
- Sideband signaling of channel, error, and start and end of packet delineation
- Support for data bursting
- User signals as sideband signals for functionality users define

Related Information

- Avalon Streaming Credit Adapters on page 180
- Avalon Streaming Credit Multiplexer on page 190
- Avalon Streaming Credit Demultiplexer on page 192
- Avalon Streaming Credit Pipeline Bridge on page 195

3.3.1. Terms and Concepts

The Avalon Streaming Credit interface protocol defines the following terms and concepts:

- **Avalon Streaming Credit System**— An Avalon Streaming Credit system contains one or more Avalon Streaming Credit connections that transfer data from a source interface to a sink interface.

- **Avalon Streaming Credit Components**— A typical system using Avalon Streaming interfaces combines multiple functional modules, called components. The system designer configures the components and connects them together to implement a system.

- **Source and Sink Interfaces and Connections**—When two components are connected, credits flow from the sink to the source; and the data flows from the source interface to the sink interface. The combination of a source interface connected to a sink interface is referred to as a connection.

- **Transfers**— A transfer results in data and control propagation from a source interface to a sink interface. For data interfaces, source can start data transfer only if it has credits available. Similarly, sink can accept data only if it has outstanding credits.
• **Symbol**—A symbol is the smallest unit of data. One or more symbols make up the single unit of data transferred in a cycle.

• **Beat**—A beat is a single cycle transfer between a source and sink interface made up of one or more symbols.

• **Packet**—A packet is an aggregation of data and control signals that is transmitted together. A packet may contain a header to help routers and other network devices direct the packet to the correct destination. The packet format is defined by the application, not this specification. Avalon Streaming packets can be variable in length and can be interleaved across a connection. With an Avalon Streaming Credit interfaces, the use of packets is optional.

### 3.3.2. Avalon Streaming Credit Adapters

Avalon Streaming Credit adapters perform data width conversion when the Avalon Streaming Credit source and Avalon Streaming Credit sink have different data widths. For example, if an Avalon Streaming Credit source and Avalon Streaming Credit sink have different data widths, you can insert the Avalon Streaming Credit Wide to Narrow Adapter, or the Avalon Streaming Credit Narrow to Wide Adapter, for data width conversion.

Platform Designer interconnect supports the following data format adapters for Avalon Streaming Credit interfaces:

**Related Information**

- Avalon Interface Specifications
- Avalon Streaming Credit Wide to Narrow Adapter on page 180
- Avalon Streaming Credit Narrow to Wide Adapter on page 182
- Avalon Streaming Credit Max Credit Adapter on page 185
- Avalon Streaming Ready to Credit Adapter on page 186
- Avalon Streaming Credit to Ready Adapter on page 188

### 3.3.2.1. Avalon Streaming Credit Wide to Narrow Adapter

The Avalon Streaming Credit Wide to Narrow Adapter has the following blocks for performing primary functions.

**Table 60. Avalon Streaming Credit Wide to Narrow Adapter Blocks**

<table>
<thead>
<tr>
<th>Adapter Block</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Management</td>
<td>Accepts incoming wide data and converts the wide data to narrow data for the sink.</td>
</tr>
<tr>
<td>Credit Management</td>
<td>Accepts incoming credits from sink and sends credits to the source. However, credits received from sink do not directly transfer to the source. Internally, this adapter implements credit management logic. The adapter sends data out if continued...</td>
</tr>
</tbody>
</table>
### Adapter Block

<table>
<thead>
<tr>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>there are credits and data available. If all the credits from sink are serviced, then the adapter holds the incoming data from the source side until the adapter receives more credits from the sink.</td>
</tr>
</tbody>
</table>

### Packet Management

Accepts the `startofpacket`, `endofpacket`, and `empty` package signals and drives them appropriately, while maintaining packet and data integrity, on the output.

### User Signal Management

Accepts user defined signals (such as `channel`, `error`, `user_signal_per_packet`, `user_signal_per_symbol`) and sends the signal to the source side, in accordance with the wide to narrow conversion.

The adapter is available for parameterization as **Avalon Streaming Credit Wide to Narrow Adapter Intel FPGA IP** in the Platform Designer IP Catalog.

#### 3.3.2.1.1. Avalon Streaming Credit Wide to Narrow Adapter Interface Parameters

You can specify the following parameters for the Avalon Streaming Credit Wide to Narrow Adapter by double-clicking **Avalon Streaming Credit Wide to Narrow Adapter Intel FPGA IP** in the Platform Designer IP Catalog:

**Note:** The source data width must be an integer multiple of the sink data width.

#### Table 61. Avalon Streaming Credit Wide to Narrow Adapter Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum Credit Allowed</strong> (Sink Interface)</td>
<td>Specifies the maximum number of credits allowed by the sink interface. The legal value is 8.</td>
<td>8</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when <strong>Use Channel</strong> is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when <strong>Use Error</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when <strong>Use Empty</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td><strong>Maximum Credit Allowed</strong> (Source Interface)</td>
<td>Specifies the maximum number of credits allowed by the source interface. Legal values are from 1 to 256.</td>
<td>1,2,4,8,16,32,64,128,256</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the <code>startofpacket</code>, <code>endofpacket</code>, and <code>empty</code> signals.</td>
<td>On</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the <code>empty</code> signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enables or disables the <code>channel</code> signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the <code>error</code> signal.</td>
<td>On</td>
</tr>
<tr>
<td>Enable User Signals</td>
<td>Allows you to specify the name, width, and type of user signals.</td>
<td>On</td>
</tr>
</tbody>
</table>

### 3.3.2.1.2. Avalon Streaming Credit Wide to Narrow Adapter Interface Signals

**Figure 105. Avalon Streaming Credit Wide to Narrow Adapter Interface Signals**

![Diagram of avst_credit_w2n_0](image)

**Related Information**

Avalon Streaming Credit Interface Signal Roles on page 243

### 3.3.2.2. Avalon Streaming Credit Narrow to Wide Adapter

The Avalon Streaming Credit Narrow to Wide Adapter has the following blocks for performing primary functions:
Table 62.  **Avalon Streaming Credit Narrow to Wide Adapter Blocks**

<table>
<thead>
<tr>
<th>Adapter Block</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Management</strong></td>
<td>Accepts incoming narrow data and converts the narrow data to wide data for the sink.</td>
</tr>
<tr>
<td><strong>Credit Management</strong></td>
<td>Accepts incoming credits from sink and sends credits to the source. However, credits received from sink do not directly transfer to the source. Internally, this adapter implements credit management logic. The adapter sends data out if there are credits and data available. If all the credits from sink are serviced, then the adapter holds the incoming data from the source side until the adapter receives more credits from the sink.</td>
</tr>
<tr>
<td><strong>Packet Management</strong></td>
<td>Accepts the startofpacket, endofpacket, and empty package signals and drives them appropriately, while maintaining packet and data integrity, on the output.</td>
</tr>
<tr>
<td><strong>User Signal Management</strong></td>
<td>Accepts user defined signals (such as channel, error, user_signal_per_packet, user_signal_per_symbol) and sends the signal to the source side, in accordance with the narrow to wide conversion.</td>
</tr>
</tbody>
</table>

The adaptor is available for parameterization as **Avalon Streaming Credit Narrow to Wide Adapter Intel FPGA IP** in the Platform Designer IP Catalog.

**Figure 106.  Avalon Streaming Credit Narrow to Wide Adapter**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Credit Allowed (Sink Interface)</td>
<td>Specifies the maximum number of credits allowed by the sink interface. The legal value is 32.</td>
<td>32</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when <strong>Use Channel</strong> is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when <strong>Use Error</strong> is disabled.</td>
<td>1-1024</td>
</tr>
</tbody>
</table>
### Parameter Name | Description | Legal Values
--- | --- | ---
**Width of Empty Port** | The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when **Use Empty** is disabled. | 1-1024

**Maximum Credit Allowed** *(Source Interface)* | Specifies the maximum number of credits allowed by the source interface. Legal values are from 1 to 256. | 1,2,4,8,16,32,64,128, 256

**Use Packets** | Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals. | On|Off

**Use Empty** | Enables or disables the empty signal. | On|Off

**Use Channel** | Enables or disables the channel signal. | On|Off

**Use Error** | Enables or disables the error signal. | On|Off

**Enable User Signals** | Allows you to specify the name, width, and type of user signals. | On|Off

---

#### 3.3.2.2.2. Avalon Streaming Credit Narrow to Wide Adapter Interface Signals

**Figure 107. Avalon Streaming Credit Narrow to Wide Adapter Interface Signals**

![Avalon Streaming Credit Narrow to Wide Adapter Interface Signals Diagram](avst_credit_n2w_0)

**Related Information**

Avalon Streaming Credit Interface Signal Roles on page 243
3.3.2.3. Avalon Streaming Credit Max Credit Adapter

The Avalon Streaming Max Credit Adapter facilitates credit flow integrity when the source's **Maximum Credit Allowed** \((\text{maxCredit})\) parameter value is less than the sink's **Maximum Credit Allowed** \((\text{maxCredit})\) value. The adaptor is available for parameterization as **Avalon Streaming Credit Max Credit Adapter Intel FPGA IP** from the Platform Designer IP Catalog.

**Figure 108. Avalon Streaming Credit Max Credit Adapter**

This adapter can accept up to the \(\text{maxCredit}\) of sink credits from the sink, and then supply credits to source according to the source's \(\text{maxCredit}\) property.

For example, if the source's \(\text{maxCredit}\) is 4 and the sink's \(\text{maxCredit}\) is 8, and the sink provides a value of 8 on the credit bus, the adapter sends 4 credits to the source. When the adapter receives 4 valid beats from the source, the adapter releases the remaining 4 credits to the source. This adapter does not modify data from the source.

3.3.2.3.1. Avalon Streaming Credit Max Credit Adapter Interface Parameters

You can specify the following parameters for the Avalon Streaming Credit Max Credit Adapter by double-clicking **Avalon Streaming Credit Max Credit Adapter Intel FPGA IP** in the Platform Designer IP Catalog:

**Table 64. Avalon Streaming Credit Max Credit Adapter Interface Parameters**

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum Credit Allowed</strong> (Sink Interface)</td>
<td>Specifies the maximum number of credits allowed by the sink interface. Legal values are from 1 to 256.</td>
<td>(1,2,4,8,16,32,64,128,256)</td>
</tr>
<tr>
<td><strong>Number of symbols</strong></td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>(1-1024)</td>
</tr>
<tr>
<td><strong>Symbol width</strong></td>
<td>Specifies the number of data bits per symbol.</td>
<td>(1-1024)</td>
</tr>
<tr>
<td><strong>Width of Channel Port</strong></td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is disabled.</td>
<td>(1-128)</td>
</tr>
<tr>
<td><strong>Width of Error Port</strong></td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when Use Error is disabled.</td>
<td>(1-1024)</td>
</tr>
<tr>
<td><strong>Width of Empty Port</strong></td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when Use Empty is disabled.</td>
<td>(1-1024)</td>
</tr>
<tr>
<td><strong>Maximum Credit Allowed</strong> (Source Interface)</td>
<td>Specifies the maximum number of credits allowed by the source interface. Legal values are from 1 to 256.</td>
<td>(1,2,4,8,16,32,64,128,256)</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the empty signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enables or disables the channel signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the error signal.</td>
<td>On</td>
</tr>
<tr>
<td>Enable User Signals</td>
<td>Allows you to specify the name, width, and type of user signals.</td>
<td>On</td>
</tr>
</tbody>
</table>

3.3.2.3.2. Avalon Streaming Credit Max Credit Adapter Interface Signals

**Figure 109. Avalon Streaming Credit Max Credit Adapter Interface Signals**

![Avalon Streaming Credit Max Credit Adapter Interface Signals](avst_credit_max_ca_0)

**Related Information**

Avalon Streaming Credit Interface Signal Roles on page 243

3.3.2.4. Avalon Streaming Ready to Credit Adapter

The Avalon Streaming Ready to Credit Adapter facilitates connectivity between an Avalon Streaming sink and an Avalon Streaming Credit source.
The Avalon Streaming Ready to Credit adapter:
- Outputs credits on the Avalon Streaming Credit sink interface.
- Outputs data on the Avalon Streaming source interface.
- Asserts ready on the Avalon Streaming sink interface.
- Supports the readyLatency property on the Avalon Streaming sink interface.
- Is available as **Avalon Streaming Ready to Credit Intel FPGA IP** from the Platform Designer IP Catalog.

**Figure 110. Avalon Streaming Ready to Credit Adapter**

![Avalon Streaming Ready to Credit Adapter](image)

### 3.3.2.4.1. Avalon Streaming Ready to Credit Adapter Interface Parameters

You can specify the following parameters for the Avalon Streaming Ready to Credit Adapter by double-clicking **Avalon Streaming Ready to Credit Intel FPGA IP** in the Platform Designer IP Catalog:

#### Table 65. Avalon Streaming Ready to Credit Adapter Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Credit Allowed (Sink Interface)</td>
<td>Specifies the maximum number of credits allowed by the sink interface. Legal values are from 1 to 256.</td>
<td>1,2,4,8,16,32,64,128,256</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when <strong>Use Channel</strong> is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when <strong>Use Error</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when <strong>Use Empty</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Ready Latency</td>
<td>Specifies the ready latency to expect from the sink connected to the module's source interface.</td>
<td>0-32</td>
</tr>
<tr>
<td>synchronous reset</td>
<td>Specifies that the adaptor should have a synchronous reset.</td>
<td>On</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
</tbody>
</table>
### 3.3.2.4.2. Avalon Streaming Ready to Credit Adapter Interface Signals

**Figure 111. Avalon Streaming Ready to Credit Adapter Interface Signals**

![Avalon Streaming Ready to Credit Adapter Interface Signals Diagram](image)

#### Related Information

- Avalon Streaming Credit Interface Signal Roles on page 243

### 3.3.2.5. Avalon Streaming Credit to Ready Adapter

The Avalon Streaming Credit to Ready Adapter facilitates connectivity between an Avalon Streaming Credit sink and an Avalon Streaming source.

The Avalon Streaming Credit to Ready adapter:
- Receives credits on the Avalon Streaming Credit source interface.
- Asserts `ready` on the Avalon Streaming sink interface.
- Supports the **Ready Latency** (`readyLatency`) parameter on the Avalon Streaming sink interface.
- Is available as **Avalon Streaming Credit to Ready Intel FPGA IP** from the Platform Designer IP Catalog.
3. Platform Designer Interconnect

You can specify the following parameters for the Avalon Streaming Credit to Ready adapter by double-clicking **Avalon Streaming Credit to Ready Intel FPGA IP** in the Platform Designer IP Catalog:

### Table 66. Avalon Streaming Credit to Ready Adapter Interface Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Credit Allowed (Source Interface)</td>
<td>Specifies the maximum number of credits allowed by the source interface. The legal value is 16.</td>
<td>16</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when Use Error is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when Use Empty is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Ready Latency</td>
<td>Specifies the readyLatency of the source connected to the adapter sink interface.</td>
<td>0-32</td>
</tr>
<tr>
<td>synchronous reset</td>
<td>Specifies that the adaptor should have a synchronous reset.</td>
<td>On</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the empty signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enables or disables the channel signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the error signal.</td>
<td>On</td>
</tr>
</tbody>
</table>
3.3.2.5.2. Avalon Streaming Credit to Ready Adapter Interface Signals

Figure 113. Avalon Streaming Credit to Ready Adapter Interface Signals

The Avalon Streaming Credit Multiplexer allows multiple sources to access a single sink.

- Supports round-robin arbitration.
- Receives credits from the sink, and ensures credits supplied to sources are independent.
- Implements separate credit management logic on both source and sink interfaces.
- Maintains packet integrity from a source.
- Is available as **Avalon Streaming Credit Multiplexer Intel FPGA IP** from the Platform Designer IP Catalog.

Related Information

Avalon Streaming Credit Interface Signal Roles on page 243
3.3.3.1. Avalon Streaming Credit Multiplexer Parameters

You can specify the following parameters for the Avalon Streaming Credit Multiplexer by double-clicking Avalon Streaming Credit Multiplexer Intel FPGA IP in the Platform Designer IP Catalog:

Table 67. Avalon Streaming Credit Multiplexer Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of mux input</td>
<td>Specifies the number of inputs to the multiplexer.</td>
<td>N/A</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the empty signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enables or disables the channel signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the error signal.</td>
<td>On</td>
</tr>
<tr>
<td>Maximum Credit Allowed (Source Interface)</td>
<td>Specifies the maximum number of credits allowed by the source interface. Legal values are from 1 to 256.</td>
<td>1,2,4,8,16,32,64,128, 256</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when Use Error is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when Use Empty is disabled.</td>
<td>1-1024</td>
</tr>
</tbody>
</table>
3.3.3.2. Avalon Streaming Credit Multiplexer Interface Signals

Figure 115. Avalon Streaming Credit Multiplexer Interface Signals

Related Information
Avalon Streaming Credit Interface Signal Roles on page 243

3.3.4. Avalon Streaming Credit Demultiplexer

The Avalon Streaming Credit Demultiplexer allows one source to access multiple sinks.
The Avalon Streaming Credit Demultiplexer:
- Must have a channel signal from the source as an input.
- The channel input from the source must be at least \( \text{ceil}(\log_2(\text{NUM_SINK})) \) wide, where \( \text{NUM_SINK} \) is the number of sinks.

For example, if the source connects to 6 sinks, the channel signal from source must be at least 3 bits. The least significant \( \text{ceil}(\log_2(\text{NUM_SINK})) \) bits route data from the source to the appropriate sink. For example, if the demultiplexer connects to 5 sinks (sink0, sink1, sink2, sink3, sink4), and the channel signal is 8-bit wide, with a value on the channel bus of 00010010, data routes to sink2.

- The source is responsible for maintaining packet integrity to any sink.
- During a packet transmission, the source must not change the lower order channel bits, otherwise the sinks may receive incomplete or invalid packets.
- Is available as Avalon Streaming Credit Demultiplexer Intel FPGA IP from the Platform Designer IP Catalog.

Figure 116. Avalon Streaming Credit Demultiplexer

3.3.4.1. Avalon Streaming Credit Demultiplexer Parameters

You can specify the following parameters for the Avalon Streaming Credit Demultiplexer by double-clicking Avalon Streaming Credit Demultiplexer Intel FPGA IP in the Platform Designer IP Catalog:

Table 68. Avalon Streaming Credit Demultiplexer Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of demux input</td>
<td>Specifies the number of inputs to the demultiplexer.</td>
<td>N/A</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
<tr>
<td>Maximum Credit Allowed (Sink Interface)</td>
<td>Specifies the maximum number of credits allowed by the sink interface. Legal values are from 1 to 256.</td>
<td>1,2,4,8,16,32,64,128, 256</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is disabled.</td>
<td>1-128</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when Use Error is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when Use Empty is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the empty signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enables or disables the channel signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the error signal.</td>
<td>On</td>
</tr>
</tbody>
</table>

### 3.3.4.2. Avalon Streaming Credit Demultiplexer Interface Signals

**Figure 117. Avalon Streaming Credit Demultiplexer Interface Signals**

![Avalon Streaming Credit Demultiplexer Interface Signals](image)

**Related Information**

Avalon Streaming Credit Interface Signal Roles on page 243
3.3.5. Avalon Streaming Credit Pipeline Bridge

The Avalon Streaming Credit Pipeline Bridge allows you to insert an arbitrary number of pipeline stages on both the credit and data paths. The number of pipeline stages on the credit path, from sink to source, need not be equal to the number of pipeline stages on the data path, from source to sink.

This bridge is available as **Avalon Streaming Credit Pipeline Bridge Intel FPGA IP** from the Platform Designer IP Catalog.

Figure 118. Avalon Streaming Credit Pipeline Bridge

![Avalon Streaming Credit Pipeline Bridge](image)

3.3.5.1. Avalon Streaming Credit Pipeline Bridge Parameters

You can specify the following parameters for the Avalon Streaming Credit Pipeline Bridge by double-clicking **Avalon Streaming Credit Pipeline Bridge Intel FPGA IP** in the Platform Designer IP Catalog:

Table 69. Avalon Streaming Credit Pipeline Bridge Parameters

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Pipeline Depth</td>
<td>Specifies the depth (size) of the data pipeline.</td>
<td>1-16</td>
</tr>
<tr>
<td>Credit Pipeline Depth</td>
<td>Specifies the depth (size) of the data pipeline.</td>
<td>1-16</td>
</tr>
<tr>
<td>Maximum Credit Allowed (Source Interface)</td>
<td>Specifies the maximum number of credits allowed by the source interface. Legal values are from 1 to 256.</td>
<td>1,2,4,8,16,32,64,128,256</td>
</tr>
<tr>
<td>Number of symbols</td>
<td>Specifies the maximum number of symbols that can transfer.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Symbol width</td>
<td>Specifies the number of data bits per symbol.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Channel Port</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when <strong>Use Channel</strong> is disabled.</td>
<td>1-128</td>
</tr>
<tr>
<td>Width of Error Port</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when <strong>Use Error</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Width of Empty Port</td>
<td>The width of the empty signal on the output interfaces. A value of 0 indicates that the empty signal is not in use. This parameter is disabled when <strong>Use Empty</strong> is disabled.</td>
<td>1-1024</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
<td>On</td>
</tr>
<tr>
<td>Use Empty</td>
<td>Enables or disables the empty signal.</td>
<td>On</td>
</tr>
</tbody>
</table>

continued...
### 3.3.5.2. Avalon Streaming Credit Pipeline Bridge Interface Signals

**Figure 119. Avalon Streaming Credit Pipeline Bridge Interface Signals**

![Avalon Streaming Credit Pipeline Bridge Interface Signals](image)

<table>
<thead>
<tr>
<th>Parameter Name</th>
<th>Description</th>
<th>Legal Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Use Channel</td>
<td>Enables or disables the channel signal.</td>
<td>On</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enables or disables the error signal.</td>
<td>On</td>
</tr>
<tr>
<td>Enable User Signals</td>
<td>Allows you to specify the name, width, and type of user signals.</td>
<td>On</td>
</tr>
</tbody>
</table>

**Related Information**

Avalon Streaming Credit Interface Signal Roles on page 243

### 3.4. Interrupt Interfaces

Using individual requests, the interrupt logic can process up to 32 IRQ inputs connected to each interrupt receiver. With this logic, the interrupt sender connected to interrupt receiver_0 is the highest priority with sequential receivers being successively lower priority. You can redefine the priority of interrupt senders by instantiating the IRQ mapper component. For more information refer to [IRQ Mapper](#).

You can define the interrupt sender interface as asynchronous with no associated clock or reset interfaces. You can also define the interrupt receiver interface as asynchronous with no associated clock or reset interfaces. As a result, the receiver does its own synchronization internally. Platform Designer does not insert interrupt synchronizers for such receivers.
For clock crossing adaption on interrupts, Platform Designer inserts a synchronizer, which is clocked with the interrupt end point interface clock when the corresponding starting point interrupt interface has no clock or a different clock (than the end point). Platform Designer inserts the adapter if there is any kind of mismatch between the start and end points. Platform Designer does not insert the adapter if the interrupt receiver does not have an associated clock.

**Related Information**

[IRQ Mapper on page 198](#)

### 3.4.1. Individual Requests IRQ Scheme

In the individual requests IRQ scheme, Platform Designer interconnect passes IRQs directly from the sender to the receiver, without making assumptions about IRQ priority. If multiple senders assert their IRQs simultaneously, the receiver logic determines which IRQ has highest priority, and then responds appropriately.

**Figure 120. Interrupt Controller Mapping IRQs**

Using individual requests, the interrupt controller can process up to 32 IRQ inputs. The interrupt controller generates a 32-bit signal $\text{irq}[31:0]$ to the receiver, and maps slave IRQ signals to the bits of $\text{irq}[31:0]$. Any unassigned bits of $\text{irq}[31:0]$ are disabled.

### 3.4.2. Assigning IRQs in Platform Designer

You assign IRQ connections on the System View tab of Platform Designer. After adding all components to the system, you connect interrupt senders and receivers. You can use the IRQ column to specify an IRQ number with respect to each receiver, or to specify a receiver’s IRQ as unconnected. Platform Designer uses the following three components to implement interrupt handling: IRQ Bridge, IRQ Mapper, and IRQ Clock Crosser.
3.4.2.1. IRQ Bridge

The IRQ Bridge allows you to route interrupt wires between Platform Designer subsystems.

**Figure 121. Platform Designer IRQ Bridge Application**

The peripheral subsystem example below has three interrupt senders that are exported to the top-level of the subsystem. The interrupts are then routed to the CPU subsystem using the IRQ bridge.

![ IRQ Bridge Diagram ]

**Note:**

Nios II BSP tools support the IRQ Bridge. Interrupts connected via an IRQ Bridge appear in the generated `system.h` file. You can use the following properties with the IRQ Bridge, which do not effect Platform Designer interconnect generation. Platform Designer uses these properties to generate the correct IRQ information for downstream tools:

- `set_interface_property <sender port> bridgesToReceiver <receiver port>`— The `<sender port>` of the IP generates a signal that is received on the IP’s `<receiver port>`. Sender ports are single bits. Receivers ports can be multiple bits. Platform Designer requires the `bridgedReceiverOffset` property to identify the `<receiver port>` bit that the `<sender port>` sends.

- `set_interface_property <sender port> bridgedReceiverOffset <port number>`— Indicates the `<port number>` of the receiver port that the `<sender port>` sends.

3.4.2.2. IRQ Mapper

Platform Designer inserts the IRQ Mapper automatically during generation. The IRQ Mapper converts individual interrupt wires to a bus, and then maps the appropriate IRQ priority number onto the bus.
By default, the interrupt sender connected to the receiver0 interface of the IRQ mapper is the highest priority, and sequential receivers are successively lower priority. You can modify the interrupt priority of each IRQ wire by modifying the IRQ priority number in Platform Designer under the IRQ column. The modified priority is reflected in the IRQ_MAP parameter for the auto-inserted IRQ Mapper.

**Figure 122. IRQ Column in Platform Designer**

Circled in the IRQ column are the default interrupt priorities allocated for the CPU subsystem.

### Related Information

**IRQ Bridge** on page 198

### 3.4.2.3. IRQ Clock Crosser

The IRQ Clock Crosser synchronizes interrupt senders and receivers that are in different clock domains. To use this component, connect the clocks for both the interrupt sender and receiver, and for both the interrupt sender and receiver interfaces. Platform Designer automatically inserts this component when it is required.

### 3.5. Clock Interfaces

Clock interfaces define the clocks used by a component. Components can have clock inputs, clock outputs, or both. To update the clock frequency of the component, use the Parameters tab for the clock source.
The **Clock Source** parameters allows you to set the following options:

- **Clock frequency**—The frequency of the output clock from this clock source.
- **Clock frequency is known**—When turned on, the clock frequency is known. When turned off, the frequency is set from outside the system.
  
  *Note:* If turned off, system generation may fail because the components do not receive the necessary clock information. For best results, turn this option on before system generation.

- **Reset synchronous edges**
  - **None**—The reset is asserted and deasserted asynchronously. You can use this setting if you have internal synchronization circuitry that matches the reset required for the IP in the system.
  - **Both**—The reset is asserted and deasserted synchronously.
  - **Deassert**—The reset is deasserted synchronously and asserted asynchronously.

For more information about synchronous design practices, refer to *Recommended Design Practices*

**Related Information**

**Recommended Design Practices**

### 3.5.1. (High Speed Serial Interface) HSSI Clock Interfaces

You can use HSSI Serial Clock and HSSI Bonded Clock interfaces in Platform Designer to enable high speed serial connectivity between clocks that are used by certain IP protocols.

#### 3.5.1.1. HSSI Serial Clock Interface

You can connect the HSSI Serial Clock interface with only similar type of interfaces, for example, you can connect a HSSI Serial Clock Source interface to a HSSI Serial Clock Sink interface.

#### 3.5.1.1.1. HSSI Serial Clock Source

The HSSI Serial Clock interface includes a source in the **Start** direction.

You can instantiate the HSSI Serial Clock Source interface in the **_hw.tcl** file as:

```tcl
add_interface <name> hssi_serial_clock start
```

You can connect the HSSI Serial Clock Source to multiple HSSI Serial Clock Sinks because the HSSI Serial Clock Source supports multiple fan-outs. This Interface has a single **clk** port role limited to a 1 bit width, and a **clockRate** parameter, which is the frequency of the clock driven by the HSSI Serial Clock Source interface.

An unconnected and unexported HSSI Serial Source is valid and does not generate error messages.
### Table 70. HSSI Serial Clock Source Port Roles

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Output</td>
<td>1 bit</td>
<td>A single bit wide port role, which provides synchronization for internal logic.</td>
</tr>
</tbody>
</table>

### Table 71. HSSI Serial Clock Source Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Default</th>
<th>Derived</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clockRate</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The frequency of the clock driven byte HSSI Serial Clock Source interface.</td>
</tr>
</tbody>
</table>

### 3.5.1.1.2. HSSI Serial Clock Sink

The HSSI Serial Clock interface includes a sink in the **End** direction.

You can instantiate the HSSI Serial Clock Sink interface in the `_hw.tcl` file as:

```
add_interface <name> hssi_serial_clock end
```

You can connect the HSSI Serial Clock Sink interface to a single HSSI Serial Clock Source interface; you cannot connect it to multiple sources. This Interface has a single `clk` port role limited to a 1 bit width, and a `clockRate` parameter, which is the frequency of the clock driven by the HSSI Serial Clock Source interface.

An unconnected and unexported HSSI Serial Sink is invalid and generates error messages.

### Table 72. HSSI Serial Clock Sink Port Roles

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Output</td>
<td>1</td>
<td>A single bit wide port role, which provides synchronization for internal logic</td>
</tr>
</tbody>
</table>

### Table 73. HSSI Serial Clock Sink Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Default</th>
<th>Derived</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clockRate</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The frequency of the clock driven by the HSSI Serial Clock Source interface. When you specify a <code>clockRate</code> greater than 0, then this interface can be driven only at that rate.</td>
</tr>
</tbody>
</table>

### 3.5.1.1.3. HSSI Serial Clock Connection

The HSSI Serial Clock Connection defines a connection between a HSSI Serial Clock Source connection point, and a HSSI Serial Clock Sink connection point.

A valid HSSI Serial Clock Connection exists when all the following criteria are satisfied. If the following criteria are not satisfied, Platform Designer generates error messages and the connection is prohibited.

- The starting connection point is an HSSI Serial Clock Source with a single port role `clk` and maximum 1 bit in width. The direction of the starting port is **Output**.
- The ending connection point is an HSSI Serial Clock Sink with a single port role `clk`, and maximum 1 bit in width. The direction of the ending port is **Input**.
- If the parameter, `clockRate` of the HSSI Serial Clock Sink is greater than 0, the connection is only valid if the `clockRate` of the HSSI Serial Clock Source is the same as the `clockRate` of the HSSI Serial Clock Sink.
3.5.1.1.4. HSSI Serial Clock Example

**Example 23. HSSI Serial Clock Interface Example**

You can make connections to declare the HSSI Serial Clock interfaces in the `_hw.tcl`.

```tcl
package require -exact qsys 14.0
set_module_property name hssi_serial_component
set_module_property ELABORATION_CALLBACK elaborate
add_fileset QUARTUS_SYNTH QUARTUS_SYNTH generate
add_fileset SIM_VERILOG SIM_VERILOG generate
add_fileset SIM_VHDL SIM_VHDL generate
set_fileset_property QUARTUS_SYNTH TOP_LEVEL "hssi_serial_component"
set_fileset_property SIM_VERILOG TOP_LEVEL "hssi_serial_component"
set_fileset_property SIM_VHDL TOP_LEVEL "hssi_serial_component"
proc elaborate {} {
  # declaring HSSI Serial Clock Source
  add_interface my_clock_start hssi_serial_clock start
  set_interface_property my_clock_start ENABLED true
  add_interface_port my_clock_start hssi_serial_clock_port_out clk Output 1
  add_interface_port my_clock_start hssi_serial_clock_port_out clk Output 1
  # declaring HSSI Serial Clock Sink
  add_interface my_clock_end hssi_serial_clock end
  set_interface_property my_clock_end ENABLED true
  add_interface_port my_clock_end hssi_serial_clock_port_in clk Input 1
  add_interface_port my_clock_end hssi_serial_clock_port_in clk Input 1
}
proc generate { output_name } {

  add_fileset_file hssi_serial_component.v VERILOG PATH "hssi_serial_component.v"
}
```

**Example 24. HSSI Serial Clock Instantiated in a Composed Component**

If you use the components in a hierarchy, for example, instantiated in a composed component, you can declare the connections as illustrated in this example.

```tcl
add_instance myinst1 hssi_serial_component
add_instance myinst2 hssi_serial_component
# add connection from source of myinst1 to sink of myinst2
add_connection myinst1.my_clock_start myinst2.my_clock_end hssi_serial_clock
# adding connection from source of myinst2 to sink of myinst1
add_connection myinst2.my_clock_start myinst2.my_clock_end hssi_serial_clock
```

3.5.1.2. HSSI Bonded Clock Interface

You can connect the HSSI Bonded Clock interface only with similar type of interfaces, for example, you can connect a HSSI Bonded Clock Source interface to a HSSI Bonded Clock Sink interface.
3.5.1.2.1. HSSI Bonded Clock Source

The HSSI Bonded Clock interface includes a source in the **Start** direction.

You can instantiate the HSSI Bonded Clock Source interface in the `_hw.tcl` file as:

```
add_interface <name> hssi_bonded_clock start
```

You can connect the HSSI Bonded Clock Source to multiple HSSI Bonded Clock Sinks because the HSSI Serial Clock Source supports multiple fanouts. This Interface has a single **clk** port role limited to a width range of 1 to 1024 bits. The HSSI Bonded Clock Source interface has two parameters: **clockRate** and **serializationFactor**.

**clockRate** is the frequency of the clock driven by the HSSI Bonded Clock Source interface, and the **serializationFactor** is the parallel data width that operates the HSSI TX serializer. The serialization factor determines the required frequency and phases of the individual clocks within the HSSI Bonded Clock interface.

An unconnected and unexported HSSI Bonded Source is valid, and does not generate error messages.

Table 74. HSSI Bonded Clock Source Port Roles

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Output</td>
<td>1 to 24 bits</td>
<td>A multiple bit wide port role which provides synchronization for internal logic.</td>
</tr>
</tbody>
</table>

Table 75. HSSI Bonded Clock Source Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Default</th>
<th>Derived</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clockRate</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The frequency of the clock driven byte HSSI Serial Clock Source interface.</td>
</tr>
<tr>
<td>serializationFactor</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The serialization factor is the parallel data width that operates the HSSI TX serializer. The serialization factor determines the necessary frequency and phases of the individual clocks within the HSSI Bonded Clock interface.</td>
</tr>
</tbody>
</table>

3.5.1.2.2. HSSI Bonded Clock Sink

The HSSI Bonded Clock interface includes a sink in the **End** direction.

You can instantiate the HSSI Bonded Clock Sink interface in the `_hw.tcl` file as:

```
add_interface <name> hssi_bonded_clock end
```

You can connect the HSSI Bonded Clock Sink interface to a single HSSI Bonded Clock Source interface; you cannot connect it to multiple sources. This Interface has a single **clk** port role limited to a width range of 1 to 1024 bits. The HSSI Bonded Clock Source interface has two parameters: **clockRate** and **serializationFactor**. **clockRate** is the frequency of the clock driven by the HSSI Bonded Clock Source interface, and the serialization factor is the parallel data width that operates the HSSI TX serializer. The serialization factor determines the required frequency and phases of the individual clocks within the HSSI Bonded Clock interface.

An unconnected and unexported HSSI Bonded Sink is invalid and generates error messages.
### Table 76. HSSI Bonded Clock Source Port Roles

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>Output</td>
<td>1 to 24 bits</td>
<td>A multiple bit wide port role which provides synchronization for internal logic.</td>
</tr>
</tbody>
</table>

### Table 77. HSSI Bonded Clock Source Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Default</th>
<th>Derived</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clockRate</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The frequency of the clock driven byte HSSI Serial Clock Source interface.</td>
</tr>
<tr>
<td>serializationFactor</td>
<td>long</td>
<td>0</td>
<td>No</td>
<td>The serialization factor is the parallel data width that operates the HSSI TX serializer. The serialization factor determines the necessary frequency and phases of the individual clocks within the HSSI Bonded Clock interface.</td>
</tr>
</tbody>
</table>

#### 3.5.1.2.3. HSSI Bonded Clock Connection

The HSSI Bonded Clock Connection defines a connection between a HSSI Bonded Clock Source connection point, and a HSSI Bonded Clock Sink connection point.

A valid HSSI Bonded Clock Connection exists when all the following criteria are satisfied. If the following criteria are not satisfied, Platform Designer generates error messages and the connection is prohibited.

- The starting connection point is an HSSI Bonded Clock Source with a single port role `clk` with a width range of 1 to 24 bits. The direction of the starting port is `Output`.
- The ending connection point is an HSSI Bonded Clock Sink with a single port role `clk` with a width range of 1 to 24 bits. The direction of the ending port is `Input`.
- The width of the starting connection point `clk` must be the same as the width of the ending connection point.
- If the parameter, `clockRate` of the HSSI Bonded Clock Sink greater than 0, then the connection is only valid if the `clockRate` of the HSSI Bonded Clock Source is same as the `clockRate` of the HSSI Bonded Clock Sink.
- If the parameter, `serializationFactor` of the HSSI Bonded Clock Sink is greater than 0, Platform Designer generates a warning if the `serializationFactor` of HSSI Bonded Clock Source is not same as the `serializationFactor` of the HSSI Bonded Clock Sink.

#### 3.5.1.2.4. HSSI Bonded Clock Example

**Example 25. HSSI Bonded Clock Interface Example**

You can make connections to declare the HSSI Bonded Clock interfaces in the `_hw.tcl` file.

```tcl
package require -exact qsys 14.0
set_module_property name hssi_bonded_component
set_module_property ELABORATION_CALLBACK elaborate
add_fileset synthesis QUARTUS_SYNTH generate
add_fileset verilog_simulation SIM_VERILOG generate
set_fileset_property synthesis TOP_LEVEL "hssi_bonded_component"
set_fileset_property verilog_simulation TOP_LEVEL "
```
If you use the components in a hierarchy, for example, instantiated in a composed component, you can declare the connections as illustrated in this example.

**Example 26. HSII Bonded Clock Instantiated in a Composed Component**

```plaintext
class elaborate { 
    add_interface my_clock_start hssi_bonded_clock start 
    set_interface_property my_clock_start ENABLED true 
    add_interface_port my_clock_start hssi_bonded_clock_port_out 
    clk Output 1024 
    add_interface my_clock_end hssi_bonded_clock end 
    set_interface_property my_clock_end ENABLED true 
    add_interface_port my_clock_end hssi_bonded_clock_port_in 
    clk Input 1024 
} 
proc generate { output_name } { 
    add_fileset_file hssi_bonded_component.v VERILOG PATH 
    "hssi_bonded_component.v"
}
```

3. Reset Interfaces

Reset interfaces provide both soft and hard reset functionality. Soft reset logic typically re-initializes registers and memories without powering down the device. Hard reset logic initializes the device after power-on.

You can define separate reset sources for each clock domain, a single reset source for all clocks, or any combination in between. You can choose to create a single global reset domain by clicking **System ➤ Create Global Reset Network**. If your design requires more than one reset domain, you can implement your own reset logic and connectivity. The IP Catalog includes a reset controller, reset sequencer, and a reset bridge to implement the reset functionality. You can also design your own reset logic.

Platform Designer interconnect now supports synchronous reset of registers in the interconnect. Use of synchronous reset can result in higher performance for Intel Stratix 10 designs because Intel Stratix 10 Hyper-Registers lack a reset signal. If a register in your Intel Stratix 10 design uses asynchronous reset, the Compiler cannot implement the register as a Hyper-Register, potentially reducing performance.

When **Use synchronous reset** is set to **True** in the **Domains** tab, all registers in the interconnect use synchronous reset. The **Use synchronous reset** option is enabled by default for Intel Stratix 10 designs, but is disabled by default for all other designs.
Note: If you design your own reset circuitry, you must carefully consider situations which may result in system lockup. For example, if an Avalon memory mapped slave is reset in the middle of a transaction, the Avalon memory mapped master may lockup.

Related Information
Specifying Interconnect Parameters on page 50

3.6.1. Single Global Reset Signal Implemented by Platform Designer

When you select **System ➤ Create Global Reset Network**, the Platform Designer interconnect creates a global reset bus. All the reset requests are ORed together, synchronized to each clock domain, and fed to the reset inputs. The duration of the reset signal is at least one clock period.

The Platform Designer interconnect inserts the system-wide reset under the following conditions:
- The global reset input to the Platform Designer system is asserted.
- Any component asserts its reset request signal.

3.6.2. Reset Controller

Platform Designer automatically inserts a reset controller block if the input reset source does not have a reset request, but the connected reset sink requires a reset request.

The Reset Controller has the following parameters that you can specify to customize its behavior:
- **Number of inputs**—Indicates the number of individual reset interfaces the controller ORs to create a signal reset output.
- **Output reset synchronous edges**—Specifies the level of synchronization. You can select one of the following options:
  - **None**—The reset is asserted and deasserted asynchronously. You can use this setting if you have designed internal synchronization circuitry that matches the reset style required for the IP in the system.
  - **Both**—The reset is asserted and deasserted synchronously.
  - **Deassert**—The reset is deasserted synchronously and asserted asynchronously.
- **Synchronization depth**—Specifies the number of register stages the synchronizer uses to eliminate the propagation of metastable events.
- **Reset request**—Enables reset request generation, which is an early signal that is asserted before reset assertion. The reset request is used by blocks that require protection from asynchronous inputs, for example, M20K blocks.

Platform Designer automatically inserts reset synchronizers under the following conditions:
- More than one reset source is connected to a reset sink
- There is a mismatch between the reset source’s synchronous edges and the reset sinks’ synchronous edges
3.6.3. Reset Bridge

The Reset Bridge allows you to use a reset signal in two or more subsystems of your Platform Designer system. You can connect one reset source to local components, and export one or more to other subsystems, as required.

The Reset Bridge parameters are used to describe the incoming reset and include the following options:

- **Active low reset**—When turned on, reset is asserted low.
- **Synchronous edges**—Specifies the level of synchronization and includes the following options:
  - **None**—The reset is asserted and deasserted asynchronously. Use this setting if you have internal synchronization circuitry.
  - **Both**—The reset is asserted and deasserted synchronously.
  - **Deassert**—The reset is deasserted synchronously, and asserted asynchronously.
- **Number of reset outputs**—The number of reset interfaces that are exported.

*Note:* Platform Designer supports multiple reset sink connections to a single reset source interface. However, there are situations in composed systems where an internally generated reset must be exported from the composed system in addition to being used to connect internal components. In this situation, you must declare one reset output interface as an export, and use another reset output to connect internal components.

3.6.4. Reset Sequencer

The Reset Sequencer allows you to control the assertion and deassertion sequence for Platform Designer system resets.

The Parameter Editor displays the expected assertion and deassertion sequences based on the current settings. You can connect multiple reset sources to the reset sequencer, and then connect the outputs of the Reset Sequencer to components in the system.
Figure 123. Elements and Flow of a Reset Sequencer

3.6.4.1. Reset Sequencer Parameters

Table 78. Reset Sequencer Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of reset outputs</td>
<td>Sets the number of output resets to be sequenced, which is the number of output reset signals defined in the component with a range of 2 to 10.</td>
</tr>
<tr>
<td>Number of reset inputs</td>
<td>Sets the number of input reset signals to be sequenced, which is the number of input reset signals defined in the component with a range of 1 to 10.</td>
</tr>
<tr>
<td>Minimum reset assertion time</td>
<td>Specifies the minimum assertion cycles between the assertion of the last sequenced reset, and the deassertion of the first sequenced reset. The range is 0 to 1023.</td>
</tr>
<tr>
<td>Enable Reset Sequencer CSR</td>
<td>Enables CSR functionality of the Reset Sequencer through an Avalon interface.</td>
</tr>
<tr>
<td>reset_out#</td>
<td>Lists the reset output signals. Set the parameters in the other columns for each reset signal in the table.</td>
</tr>
<tr>
<td>ASRT Seq#</td>
<td>Determines the order of reset assertion. Enter the values 1, 2, 3, etc. to specify the required non-overlapping assertion order. This value determines the ASRT_REMAP value in the component HDL.</td>
</tr>
<tr>
<td>ASRT Cycle#</td>
<td>Number of cycles to wait before assertion of the reset. The value set here corresponds to the ASRT_DELAY value in the component HDL. The range is 0 to 1023.</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSRT Seq#</td>
<td>Determines the reset order of reset deassertion. Enter the values 1, 2, 3, etc. to specify the required non-overlapping deassertion order. This value determines the DSRT_REMAP value in the component HDL.</td>
</tr>
<tr>
<td>DSRT Cycle#/Deglitch#</td>
<td>Number of cycles to wait before deasserting or deglitching the reset. If the USE_DSRT_QUAL parameter is set to 0, specifies the number of cycles to wait before deasserting the reset. If USE_DSRT_QUAL is set to 1, specifies the number of cycles to deglitch the input reset_dsrt_qual signal. This value determines either the DSRT_DELAY, or the DSRT_QUALCNT value in the component HDL, depending on the USE_DSRT_QUAL parameter setting. The range is 0 to 1023.</td>
</tr>
<tr>
<td>USE_DSRT_QUAL</td>
<td>If you set USE_DSRT_QUAL to 1, the deassertion sequence waits for an external input signal for sequence qualification instead of waiting for a fixed delay count. To use a fixed delay count for deassertion, set this parameter to 0.</td>
</tr>
</tbody>
</table>

### 3.6.4.2. Reset Sequencer Timing Diagrams

**Figure 124. Basic Sequencing**

![Basic Sequencing Diagram](image1)

**Figure 125. Sequencing with USE_DSRT_QUAL Set**

![Sequencing with USE_DSRT_QUAL Set Diagram](image2)
3.6.4.3. Reset Sequencer CSR Registers

The Reset Sequencer’s CSR registers provide the following functionality:

- **Support reset logging**
  - Ability to identify which reset is asserted.
  - Ability to determine whether any reset is currently active.

- **Support software triggered resets**
  - Ability to generate reset by writing to the register.
  - Ability to disable assertion or deassertion sequence.

- **Support software sequenced reset**
  - Ability for the software to fully control the assertion/deassertion sequence by writing to registers and stepping through the sequence.

- **Support reset override**
  - Ability to assert a specific component reset through software.

### Table 79. Reset Sequencer CSR Register Map

<table>
<thead>
<tr>
<th>Register</th>
<th>Offset</th>
<th>Width</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Status Register</td>
<td>0x00</td>
<td>32</td>
<td>0x0</td>
<td>The Status register indicates which sources are allowed to cause a reset.</td>
</tr>
<tr>
<td>Interrupt Enable Register</td>
<td>0x04</td>
<td>32</td>
<td>0x0</td>
<td>The Interrupt Enable register bits enable events triggering the IRQ of the reset sequencer.</td>
</tr>
<tr>
<td>Control Register</td>
<td>0x08</td>
<td>32</td>
<td>0x0</td>
<td>The Control register allows you to control the Reset Sequencer.</td>
</tr>
<tr>
<td>Software Sequenced Reset Assert Control Register</td>
<td>0x0C</td>
<td>32</td>
<td>0x3FF</td>
<td>You can program the Software Sequenced Reset Assert control register to control the reset assertion sequence.</td>
</tr>
<tr>
<td>Software Sequenced Reset Deassert Control Register</td>
<td>0x10</td>
<td>32</td>
<td>0x3FF</td>
<td>You can program the Software Sequenced Reset Deassert control register to control the reset deassertion sequence.</td>
</tr>
<tr>
<td>Software Direct Controlled Resets</td>
<td>0x14</td>
<td>32</td>
<td>0x0</td>
<td>You can write a bit to 1 to assert the reset_outN signal, and to 0 to deassert the reset_outN signal.</td>
</tr>
<tr>
<td>Software Reset Masking</td>
<td>0x18</td>
<td>32</td>
<td>0x0</td>
<td>Masking off (writing 1) to a reset_outN &quot;Reset Mask Enable&quot; signal prevents the corresponding reset from being asserted. Writing a bit to 0 to a reset mask enable signal allows assertion of reset_outN.</td>
</tr>
</tbody>
</table>

#### 3.6.4.3.1. Reset Sequencer Status Register

The **Status register** indicates which sources are allowed to cause a reset.

You can clear bits by writing 1 to the bit location. The Reset Sequencer ignores attempts to write bits with a value of 0. If the sequencer is reset (power-on-reset), all bits are cleared, except the power-on-reset bit.
Table 80. Values for the Status Register at Offset 0x00

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RO</td>
<td>0</td>
<td>Reset Active—Indicates that the sequencer is currently active in reset sequence (assertion or deassertion).</td>
</tr>
<tr>
<td>30</td>
<td>RW1C</td>
<td>0</td>
<td>Reset Asserted and waiting for SW to proceed—Set when there is an active reset assertion, and the next sequence is waiting for the software to proceed. Only valid when the Enable SW sequenced reset assert option is turned on.</td>
</tr>
<tr>
<td>29</td>
<td>RW1C</td>
<td>0</td>
<td>Reset Deasserted and waiting for SW to proceed—Set when there is an active reset deassertion, and the next sequence is waiting for the software to proceed. Only valid when the Enable SW sequenced reset deassert option is turned on.</td>
</tr>
<tr>
<td>28-26</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25-16</td>
<td>RW1C</td>
<td>0</td>
<td>Reset deassertion input qualification signal reset_dsrt_qual [9:0] status—Indicates that the reset deassertion’s input signal qualification signal is set. This bit is set on the detection of assertion of the signal.</td>
</tr>
<tr>
<td>15-12</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in9 was triggered—Indicates that reset_in9 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>10</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in8 was triggered—Indicates that reset_in8 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>9</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in7 was triggered—Indicates that reset_in7 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>8</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in6 was triggered—Indicates that reset_in6 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>7</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in5 was triggered—Indicates that reset_in5 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>6</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in4 was triggered—Indicates that reset_in4 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>5</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in3 was triggered—Indicates that reset_in3 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>4</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in2 was triggered—Indicates that reset_in2 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>3</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in1 was triggered—Indicates that reset_in1 triggered the reset. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>2</td>
<td>RW1C</td>
<td>0</td>
<td>reset_in0 was triggered—Indicates that reset_in0 triggered. Software clears this bit by writing 1 to this location.</td>
</tr>
<tr>
<td>1</td>
<td>RW1C</td>
<td>0</td>
<td>Software-triggered reset—Indicates that the software-triggered reset is set by the software, and triggering a reset.</td>
</tr>
<tr>
<td>0</td>
<td>RW1C</td>
<td>0</td>
<td>Power-on-reset was triggered—Asserted whenever the reset to the sequencer is triggered. This bit is NOT reset when sequencer is reset. Software clears this bit by writing 1 to this location.</td>
</tr>
</tbody>
</table>

**Related Information**

[Reset Sequencer CSR Registers](#) on page 210
### 3.6.4.3.2. Reset Sequencer Interrupt Enable Register

The Interrupt Enable register bits enable events triggering the IRQ of the reset sequencer.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on Reset Asserted and waiting for SW to proceed enable. When set, the IRQ is set when the sequencer is waiting for the software to proceed in an assertion sequence.</td>
</tr>
<tr>
<td>29</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on Reset Deasserted and waiting for SW to proceed enable. When set, the IRQ is set when the sequencer is waiting for the software to proceed in a deassertion sequence.</td>
</tr>
<tr>
<td>28:26</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>25:16</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on Reset deassertion input qualification signal reset_dsrt_qual_[9:0] status—When set, the IRQ is set when the reset_dsrt_qual[9:0] status bit (per bit enable) is set.</td>
</tr>
<tr>
<td>15:12</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in9 Enable—When set, the IRQ is set when the reset_in9 trigger status bit is set.</td>
</tr>
<tr>
<td>10</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in8 Enable—When set, the IRQ is set when the reset_in8 trigger status bit is set.</td>
</tr>
<tr>
<td>9</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in7 Enable—When set, the IRQ is set when the reset_in7 trigger status bit is set.</td>
</tr>
<tr>
<td>8</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in6 Enable—When set, the IRQ is set when the reset_in6 trigger status bit is set.</td>
</tr>
<tr>
<td>7</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in5 Enable—When set, the IRQ is set when the reset_in5 trigger status bit is set.</td>
</tr>
<tr>
<td>6</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in4 Enable—When set, the IRQ is set when the reset_in4 trigger status bit is set.</td>
</tr>
<tr>
<td>5</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in3 Enable—When set, the IRQ is set when the reset_in3 trigger status bit is set.</td>
</tr>
<tr>
<td>4</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in2 Enable—When set, the IRQ is set when the reset_in2 trigger status bit is set.</td>
</tr>
<tr>
<td>3</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in1 Enable—When set, the IRQ is set when the reset_in1 trigger status bit is set.</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on reset_in0 Enable—When set, the IRQ is set when the reset_in0 trigger status bit is set.</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on Software triggered reset Enable—When set, the IRQ is set when the software triggered reset status bit is set.</td>
</tr>
<tr>
<td>0</td>
<td>RW</td>
<td>0</td>
<td>Interrupt on Power-On-Reset Enable—When set, the IRQ is set when the power-on-reset status bit is set.</td>
</tr>
</tbody>
</table>

**Related Information**

[Reset Sequencer CSR Registers](#) on page 210
3.6.4.3.3. Reset Sequencer Control Register

The Control register allows you to control the Reset Sequencer.

Table 82. Values for the Control Register at Offset 0x08

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:3</td>
<td>RW</td>
<td>Reserved.</td>
<td>Enable SW sequenced reset assert—Enable a software sequenced reset assert sequence. Timer delays and input qualification are ignored, and only the software can sequence the assert.</td>
</tr>
<tr>
<td>2</td>
<td>RW</td>
<td>0</td>
<td>Enable SW sequenced reset deassert—Enable a software sequenced reset deassert sequence. Timer delays and input qualification are ignored, and only the software can sequence the deassert.</td>
</tr>
<tr>
<td>1</td>
<td>RW</td>
<td>0</td>
<td>Initiate Reset Sequence—To trigger the hardware sequenced warm reset, the Reset Sequencer writes this bit to 1 a single time. The Reset Sequencer verifies that Reset Active is 0 before setting this bit, and always reads the value 0. To monitor this sequence, verify that Reset Active is asserted, and then subsequently deasserted.</td>
</tr>
</tbody>
</table>

Related Information
Reset Sequencer CSR Registers on page 210

3.6.4.3.4. Reset Sequencer Software Sequenced Reset Assert Control Register

You can program the Software Sequenced Reset Assert control register to control the reset assertion sequence.

When the corresponding enable bit is set, the sequencer stops when the desired reset asserts, and then sets the Reset Asserted and waiting for SW to proceed bit. The Reset Sequencer proceeds only after the Reset Asserted and waiting for SW to proceed bit is cleared.

Table 83. Values for the Reset Sequencer Software Sequenced Reset Assert Control Register at Offset 0x0C

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>RW</td>
<td>Reserved.</td>
<td>Per-reset SW sequenced reset assert enable—This is a per-bit enable for SW sequenced reset assert. If the register's bitN is set, the sequencer sets the bit30 of the status register when a resetN is asserted. It then waits for the bit30 of the status register to clear before proceeding with the sequence. By default, all bits are enabled (fully SW sequenced).</td>
</tr>
</tbody>
</table>

Related Information
Reset Sequencer CSR Registers on page 210

3.6.4.3.5. Reset Sequencer Software Sequenced Reset Deassert Control Register

You can program the Software Sequenced Reset Deassert register to control the reset deassertion sequence.
When the corresponding enable bit is set, the sequencer stops when the desired reset asserts, and then sets the Reset Deasserted and waiting for SW to proceed bit. The Reset Sequencer proceeds only after the Reset Deasserted and waiting for SW to proceed bit is cleared.

### Table 84. Values for the Reset Sequencer Software Sequenced Reset Deassert Control Register at Offset 0x10

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0x3FF</td>
<td>Per-reset SW sequenced reset deassert enable—This is a per-bit enable for SW-sequenced reset deassert. If bitN of this register is set, the sequencer sets bit29 of the Status Register when a resetN is asserted. It then waits for the bit29 of the status register to clear before proceeding with the sequence. By default, all bits are enabled (fully SW sequenced).</td>
</tr>
</tbody>
</table>

#### Related Information
Reset Sequencer CSR Registers on page 210

### 3.6.4.3.6. Reset Sequencer Software Direct Controlled Resets

You can write a bit to 1 to assert the reset_outN signal, and to 0 to deassert the reset_outN signal.

### Table 85. Values for the Software Direct Controlled Resets at Offset 0x14

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:26</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25:16</td>
<td>WO</td>
<td>0</td>
<td>Reset Overwrite Trigger Enable—This is a per-bit control trigger bit for the overwrite value to take effect.</td>
</tr>
<tr>
<td>15:10</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:0</td>
<td>WO</td>
<td>0</td>
<td>reset_outN Reset Overwrite Value—This is a per-bit control of the reset_out bit. The Reset Sequencer can use this to forcefully drive the reset to a specific value. A value of 1 sets the reset_out. A value of 0 clears the reset_out. A write to this register only takes effect if the corresponding trigger bit in this register is set.</td>
</tr>
</tbody>
</table>

#### Related Information
Reset Sequencer CSR Registers on page 210

### 3.6.4.3.7. Reset Sequencer Software Reset Masking

Masking off (writing 1) to a reset_outN "Reset Mask Enable" signal prevents the corresponding reset from being asserted. Writing a bit to 0 to a reset mask enable signal allows assertion of reset_outN.
## Table 86. Values for the Reset Sequencer Software Reset Masking at Offset 0x18

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:10</td>
<td></td>
<td>Reserved.</td>
<td>Reserved.</td>
</tr>
<tr>
<td>9:0</td>
<td>RW</td>
<td>0</td>
<td>reset_outN &quot;Reset Mask Enable&quot;—This is a per-bit control to mask off the reset_outN bit. Software Reset Masking prevents the reset bit from being asserted during a reset assertion sequence. If reset_out is already asserted, it does not deassert the reset.</td>
</tr>
</tbody>
</table>

### Related Information

- [Reset Sequencer CSR Registers](#) on page 210
3.6.4.4. Reset Sequencer Software Flows

3.6.4.4.1. Reset Sequencer (Software-Triggered) Flow

Figure 126. Reset Sequencer (Software-Triggered) Flow Diagram

Software clears all pending statuses by writing all 1s to the Status Register.

Software initiates reset by writing a 1 to the Control Register’s initiate reset sequence bit.

IRQ Asserted?

Yes

Software reads Status Register’s reset active

1

keep polling

keep polling

No

keep polling

Software reads Status Register’s SW-triggered reset

1

reset active

0

0

keep polling

keep polling

Reset Sequencer completed initiating a reset through the sequencer.

Software writes 1 to Status Register’s SW-Triggered reset to clear it

Related Information

- Reset Sequencer Status Register on page 210
- Reset Sequencer Control Register on page 213
3.6.4.4.2. Reset Assert Flow

The following flow sequence occurs for a Reset Assert Flow:

- A reset is triggered either by the software, or when input resets to the Reset Sequencer are asserted.
- The IRQ is asserted, if the IRQ is enabled.
- Software reads the Status register to determine which reset was triggered.

3.6.4.4.3. Reset Deassert Flow

The following flow sequence occurs for a Reset Deassert Flow:

- When a reset source is deasserted, or when the reset assert sequence has completed without pending resets asserted, the deassertion flow is initiated.
- The IRQ is asserted, if the IRQ is enabled.
- Software reads the Status Register to determine which reset was triggered.

3.6.4.4.4. Reset Assert (Software Sequenced) Flow

Figure 127. Reset Assert (Software Sequenced) Flow

Related Information

- Reset Sequencer Control Register on page 213
- Reset Sequencer Software Sequenced Reset Assert Control Register on page 213
- Reset Sequencer Interrupt Enable Register on page 212
- Reset Sequencer Status Register on page 210
3.6.4.4.5. Reset Deassert (Software Sequenced) Flow

The sequence and flow is similar to the Reset Assert (SW Sequenced) flow, though, this flow uses the reset deassert registers/bits instead of the reset assert registers/bits.

Related Information
Reset Assert (Software Sequenced) Flow on page 217

3.7. Conduits

You can use the conduit interface type for interfaces that do not fit any of the other interface types, and to group any arbitrary collection of signals. Like other interface types, you can export or connect conduit interfaces.

The PCI Express-to-Ethernet example in Creating a System with Platform Designer is an example of using a conduit interface for export. You can declare an associated clock interface for conduit interfaces in the same way as memory-mapped interfaces with the associatedClock.

To connect two conduit interfaces inside Platform Designer, the following conditions must be met:
- The interfaces must match exactly with the same signal roles and widths.
- The interfaces must be the opposite directions.
- Clocked conduit connections must have matching associatedClocks on each of their endpoint interfaces.

Note: To connect a conduit output to more than one input conduit interface, you can create a custom component. The custom component could have one input that connects to two outputs, and you can use this component between other conduits that you want to connect. For information about the Avalon Conduit interface, refer to the Avalon Interface Specifications

Related Information
- Avalon Interface Specifications
- Creating a System with Platform Designer on page 10

3.8. Interconnect Pipelining

Pipeline stages increase a design's f_{MAX} by reducing the combinational logic depth, at the cost of additional latency and logic.

The Limit interconnect pipeline stages to option in the Interconnect Requirements tab allows you to define the maximum Avalon streaming pipeline stages that Platform Designer can insert during generation. You can specify between 0 to 4 pipeline stages, where 0 means that the interconnect has a combinational datapath. Choosing 3 or 4 pipeline stages may significantly increase the logic utilization of the system.

Platform Designer adds additional latency once on the command path, and once on the response path.
This setting is specific for each Platform Designer system or subsystem, so you can specify a unique interconnect pipeline stage value for each subsystem.

The insertion of pipeline stages depends upon the existence of certain interconnect components. For example, single-slave systems do not have multiplexers; therefore, multiplexer pipelining does not occur. In an extreme case, of a single-master to single-slave system, no pipelining occurs, regardless of the value of the **Limit interconnect pipeline stages to** option.
Figure 128. Pipeline Placement in Arbitration Logic

The example shows the possible placement of up to four potential pipeline stages. Platform Designer places these stages before the input to the demultiplexer, at the output of the multiplexer, between the arbiter and the multiplexer, and at the output of the demultiplexer.

You can manually adjust number of pipeline stages in the Platform Designer Memory-Mapped Interconnect tab.

Related Information
- Previewing the System Interconnect on page 48
- Inserting Pipeline Stages to Increase System Frequency on page 264
3.8.1. Manually Control Pipelining in the Platform Designer Interconnect

The Memory-Mapped Interconnect tab allows you to manipulate pipeline connections in the Platform Designer interconnect.

Consider manually pipelining the interconnect only when changes to the Limit interconnect pipeline stages to option do not improve frequency, and exhausted all other options to achieve timing closure, including the use of a bridge. Perform manual pipelining only in complete systems.

Access the Memory-Mapped Interconnect tab by clicking System ➤ Show System With Platform Designer Interconnect

1. In the Intel Quartus Prime software, compile the design and run timing analysis.
2. From the timing analysis output, identify the critical path through the interconnect and determine the approximate mid-point.
4. In the Memory-Mapped Interconnect tab, select the interconnect module that contains the critical path.
   You can determine the name of the module from the hierarchical node names in the timing report.
5. Click Show Pipelinable Locations. Platform Designer display all possible pipeline locations in the interconnect. Right-click the possible pipeline location to insert or remove a pipeline stage.
6. Locate the possible pipeline location that is closest to the mid-point of the critical path. The names of the blocks in the memory-mapped interconnect tab correspond to the module instance names in the timing report.
7. Right-click the location where you want to insert a pipeline, and then click Insert Pipeline.
8. Regenerate the Platform Designer system, recompile the design, and then rerun timing analysis.
9. If necessary, repeat the manual pipelining process again until the design meets the timing requirements.

Manual pipelining has the following limitations:

- If you make changes to the original system’s connectivity after manually pipelining an interconnect, the inserted pipelines may become invalid. Platform Designer displays warning messages when you generate the system if invalid pipeline stages are detected. You can remove invalid pipeline stages with the Remove Stale Pipelines option in the Memory-Mapped Interconnect tab. Do not make changes to the system’s connectivity after manual pipeline insertion.
- Review manually-inserted pipelines when upgrading to newer versions of Platform Designer. Manually-inserted pipelines in one version of Platform Designer may not be valid in a future version.
3.9. Error Correction Coding (ECC) in Platform Designer Interconnect

Error Correction Coding (ECC) logic allows the Platform Designer interconnect to detect and correct errors. Enabling ECC improves data integrity in memory blocks. Platform Designer supports ECC protection for Read Data FIFO (rdata_FIFO) instances only.

As transistors become smaller, computer hardware is more susceptible to data corruption. Data corruption causes Single Event Upsets (SEUs), and increases the probability of Failures in Time (FIT) rates in computer systems. SEU events without error notification can cause the system to be stuck in an unknown response status, and increase the FIT rate.

Before writing data to the memory device, the ECC logic encodes the data bus with a Hamming code. Then, the ECC logic decodes and performs error checking on the data output.

When you enable ECC, Platform Designer interconnect sends uncorrectable errors arising from memory as DECODEERROR (DECERR) on the Avalon response bus.

![Figure 129. High-Level Implementation of rdata_FIFO with ECC Enabled](image)

Note: Enabling ECC logic may increase logic utilization and cause lower fMAX.

Related Information
- Read and Write Responses on page 166
- Interconnect Requirements

3.10. AMBA 3 AXI Protocol Specification Support (version 1.0)

Platform Designer allows memory-mapped connections between AMBA 3 AXI components, AMBA 3 AXI and AMBA 4 AXI components, and AMBA 3 AXI and Avalon interfaces with unique or exceptional support. Refer to the AMBA 3 Protocol Specifications on the ARM website for more information.

Related Information
- Arm AMBA Protocol Specifications
- Slave Network Interfaces on page 153

3.10.1. Channels

Platform Designer has the following support and restrictions for AMBA 3 AXI channels.
3.10.1.1. Read and Write Address Channels

Most signals are allowed. However, the following limitations are present in Platform Designer 14.0:
- Supports 64-bit addressing.
- ID width limited to 18-bits.
- HPS-FPGA master interface has a 12-bit ID.

3.10.1.2. Write Data, Write Response, and Read Data Channels

Most signals are allowed. However, the following limitations are present in Platform Designer 14.0:
- Data widths limited to a maximum of 1024-bits
- Limited to a fixed byte width of 8-bits

3.10.1.3. Low Power Channel

Low power extensions are not supported in Platform Designer, version 14.0.

3.10.2. Cache Support

AWCACHE and ARCACHE are passed to an AXI slave unmodified.

3.10.2.1. Bufferable

Platform Designer interconnect treats AXI transactions as non-bufferable. All responses must come from the terminal slave.

When connecting to Avalon memory mapped slaves, since they do not have write responses, the following exceptions apply:
- For Avalon memory mapped slaves, the write response are generated by the slave agent once the write transaction is accepted by the slave. The following limitation exists for an Avalon bridge:
- For an Avalon bridge, the response is generated before the write reaches the endpoint; users must be aware of this limitation and avoid multiple paths past the bridge to any endpoint slave, or only perform bufferable transactions to an Avalon bridge.

3.10.2.2. Cacheable (Modifiable)

Platform Designer interconnect acknowledges the cacheable (modifiable) attribute of AXI transactions.

It does not change the address, burst length, or burst size of non-modifiable transactions, with the following exceptions:
- Platform Designer considers a wide transaction to a narrow slave as modifiable because the size requires reduction.
- Platform Designer may consider AXI read and write transactions as modifiable when the destination is an Avalon slave. The AXI transaction may be split into multiple Avalon transactions if the slave is unable to accept the transaction. This may occur because of burst lengths, narrow sizes, or burst types.
Platform Designer ignores all other bits, for example, read allocate or write allocate because the interconnect does not perform caching. By default, Platform Designer considers Avalon master transactions as non-bufferable and non-cacheable, with the allocate bits tied low.

### 3.10.3. Security Support

TrustZone refers to the security extension of the ARM architecture, which includes the concept of "secure" and "non-secure" transactions, and a protocol for processing between the designations.

The interconnect passes the AWPROT and ARPROT signals to the endpoint slave without modification. It does not use or modify the PROT bits.

Refer to Manage System Security in Creating a System with Platform Designer for more information about secure systems and the TrustZone feature.

#### Related Information

Configuring Platform Designer System Security on page 55

### 3.10.4. Atomic Accesses

Exclusive accesses are supported for AXI slaves by passing the lock, transaction ID, and response signals from master to slave, with the limitation that slaves that do not reorder responses. Avalon slaves do not support exclusive accesses, and always return OKAY as a response. Locked accesses are also not supported.

### 3.10.5. Response Signaling

Full response signaling is supported. Avalon slaves always return OKAY as a response.

### 3.10.6. Ordering Model

Platform Designer interconnect provides responses in the same order as the commands are issued.

To prevent reordering, for slaves that accept reordering depths greater than 1, Platform Designer does not transfer the transaction ID from the master, but provides a constant transaction ID of 0. For slaves that do not reorder, Platform Designer allows the transaction ID to be transferred to the slave. To avoid cyclic dependencies, Platform Designer supports a single outstanding slave scheme for both reads and writes. Changing the targeted slave before all responses have returned stalls the master, regardless of transaction ID.

#### 3.10.6.1. AXI and Avalon Ordering

There is a potential read-after-write risk when Avalon masters transact to AXI slaves.

According to the AMBA Protocol Specifications, there is no ordering requirement between reads and writes. However, Avalon has an implicit ordering model that requires transactions from a master to the same slave to be in order. The Avalon interconnect always processes the transactions in order. The interconnect blocks transactions if required. The interconnect prevents writing to the slave when read is pending.
3.10.7. Data Buses

Narrow bus transfers are supported. AXI write strobes can have any pattern that is compatible with the address and size information. Intel recommends that transactions to Avalon slaves follow Avalon byteenable limitations for maximum compatibility.

*Note:* Byte 0 is always bits [7:0] in the interconnect, following AXI's and Avalon's byte (address) invariance scheme.

3.10.8. Unaligned Address Commands

Unaligned address commands are commands with addresses that do not conform to the data width of a slave. Since Avalon memory mapped slaves accept only aligned addresses, Platform Designer modifies unaligned commands from AXI masters to the correct data width. Platform Designer must preserve commands issued by AXI masters when passing the commands to AXI slaves.

*Note:* Unaligned transfers are aligned if downsizing occurs. For example, when downsizing to a bus width narrower than that required by the transaction size, AWSIZE or ARSIZE, the transaction must be modified.

3.10.9. Avalon and AXI Transaction Support

Platform Designer supports transactions between Avalon and AXI interfaces with the following limitations in this section.

**Related Information**

Avalon Interface Specifications

3.10.9.1. Transaction Cannot Cross 4KB Boundaries

When an Avalon master issues a transaction to an AXI slave, the transaction cannot cross 4KB boundaries. Non-bursting Avalon masters already follow this boundary restriction.

When connecting an Avalon memory-mapped interface FPGA master to an AXI slave in Platform Designer, you must ensure that the bursts do not exceed the AXI3 or AXI4 4KB boundary restriction for burst transactions.

3.10.9.2. Adjacent Bytelanes with Partial Width Transactions

The following limitations apply to Avalon to AXI partial width transactions with use of adjacent bytelanes:

- **Avalon interfaces only support adjacent bytelanes if the interface requires more than one byte enable. For example:** 1100, 0011.

- **AXI fully supports use of bytelanes that are not adjacent. For example:** 1010, 0101.

**Related Information**

Avalon Interface Specifications
3.10.9.3. Handling Read Side Effects

Read side effects can occur when more bytes than necessary are read from the slave, and the unwanted data that are read are later inaccessible on subsequent reads. For write commands, the correct byteenable paths are asserted based on the size of the transactions. For read commands, narrow-sized bursts are broken up into multiple non-bursting commands, and each command with the correct byteenable paths asserted.

Platform Designer always assumes that the byteenable is asserted based on the size of the command, not the address of the command. The following scenarios are examples:

- For a 32-bit AXI master that issues a read command with an unaligned address starting at address $0x01$, and a burstcount of 2 to a 32-bit Avalon slave, the starting address is: $0x00$.
- For a 32-bit AXI master that issues a read command with an unaligned address starting at address $0x01$, with 4-bytes to an 8-bit AXI slave, the starting address is: $0x00$.

3.11. AMBA 3 APB Protocol Specification Support (version 1.0)

APB (Advanced Peripheral Bus) interface is optimized for minimal power consumption and reduced interface complexity. You can use APB to interface to peripherals which are low-bandwidth and do not require the high performance of a pipelined bus interface. Signal transitions are sampled at the rising edge of the clock to enable the integration of APB peripherals easily into any design flow.

Platform Designer allows connections between APB components, and AMBA 3 AXI, AMBA 4 AXI, and Avalon memory-mapped interfaces. The following sections describe unique or exceptional APB support in the Platform Designer software.

Related Information

Arm AMBA Protocol Specifications

3.11.1. Bridges

With APB, you cannot use bridge components that use multiple $\text{PSEL}_x$ in Platform Designer. As a workaround, you can group $\text{PSEL}_x$, and then send the packet to the slave directly.

Intel recommends as an alternative that you instantiate the APB bridge and all the APB slaves in Platform Designer. You should then connect the slave side of the bridge to any high speed interface and connect the master side of the bridge to the APB slaves. Platform Designer creates the interconnect on either side of the APB bridge and creates only one $\text{PSEL}$ signal.

Alternatively, you can connect a bridge to the APB bus outside of Platform Designer. Use an Avalon/AXI bridge to export the Avalon/AXI master to the top-level, and then connect this Avalon/AXI interface to the slave side of the APB bridge. Alternatively, instantiate the APB bridge in Platform Designer and export APB master to the top-level, and from there connect to APB bus outside of Platform Designer.
3.11.2. Burst Adaptation

APB is a non-bursting interface. Therefore, for any AXI or Avalon master with bursting support, a burst adapter is inserted before the slave interface and the burst transaction is translated into a series of non-bursting transactions before reaching the APB slave.

3.11.3. Width Adaptation

Platform Designer allows different data width connections with APB. When connecting a wider master to a narrower APB slave, the width adapter converts the wider transactions to a narrower transaction to fit the APB slave data width. APB does not support Write Strobe. Therefore, when you connect a narrower transaction to a wider APB slave, the slave cannot determine which byte lane to write. In this case, the slave data may be overwritten or corrupted.

3.11.4. Error Response

Error responses are returned to the master. Platform Designer performs error mapping if the master is an AMBA 3 AXI or AMBA 4 AXI master, for example, RRESP/BRESP=SLVERR. For the case when the slave does not use SLVERR signal, an OKAY response is sent back to master by default.

3.12. AMBA 4 AXI Memory-Mapped Interface Support (version 2.0)

Platform Designer allows memory-mapped connections between AMBA 4 AXI components, AMBA 4 AXI and AMBA 3 AXI components, and AMBA 4 AXI and Avalon interfaces with unique or exceptional support.

3.12.1. Burst Support

Platform Designer supports INCR bursts up to 256 beats. Platform Designer converts long bursts to multiple bursts in a packet with each burst having a length less than or equal to MAX_BURST when going to AMBA 3 AXI or Avalon slaves.

For narrow-sized transfers, bursts with Avalon slaves as destinations are shortened to multiple non-bursting transactions in order to transmit the correct address to the slaves, since Avalon slaves always perform full-sized datawidth transactions.

Bursts with AMBA 3 AXI slaves as destinations are shortened to multiple bursts, with each burst length less than or equal to 16. Bursts with AMBA 4 AXI slaves as destinations are not shortened.

3.12.2. QoS

Platform Designer routes 4-bit QoS signals (Quality of Service Signaling) on the read and write address channels directly from the master to the slave.

Transactions from AMBA 3 AXI and Avalon masters have a default value of 4'b0000, which indicates that the transactions are not part of the QoS flow. QoS values are not used for slaves that do not support QoS.

For Platform Designer 14.0, there are no programmable QoS registers or compile-time QoS options for a master that overrides its real or default value.
3.12.3. Regions

For Platform Designer 14.0, there is no support for the optional regions feature. AMBA 4 AXI slaves with AXREGION signals are allowed. AXREGION signals are driven with the default value of 0x0, and are limited to one entry in a master's address map.

3.12.4. Write Response Dependency

Write response dependency as specified in the Arm AMBA Protocol Specifications for AMBA 4 AXI is not supported.

Related Information
Arm AMBA Protocol Specifications

3.12.5. AWCACHE and ARCACHE

For AMBA 4 AXI, Platform Designer meets the requirement for modifiable and non-modifiable transactions. The modifiable bit refers to ARCACHE[1] and AWCACHE[1].

3.12.6. Width Adaptation and Data Packing in Platform Designer

Data packing applies only to systems where the data width of masters is less than the data width of slaves.

The following rules apply:

• Data packing is supported when masters and slaves are Avalon memory mapped.
• Data packing is not supported when any master or slave is an AMBA 3 AXI, AMBA 4 AXI, or APB component.

For example, for a read/write command with a 32-bit master connected to a 64-bit slave, and a transaction of 2 burstcounts, Platform Designer sends 2 separate read/write commands to access the 64-bit data width of the slave. Data packing is only supported if the system does not contain AMBA 3 AXI, AMBA 4 AXI, or APB masters or slaves.

3.12.7. Ordering Model

Out of order support is not implemented in Platform Designer, version 14.0. Platform Designer processes AXI slaves as device non-bufferable memory types.

The following describes the required behavior for the device non-bufferable memory type:

• Write response must be obtained from the final destination.
• Read data must be obtained from the final destination.
• Transaction characteristics must not be modified.
• Reads must not be pre-fetched. Writes must not be merged.
• Non-modifiable read and write transactions.
(AWCACHE[1] = 0 or ARCACHE[1] = 0) from the same ID to the same slave must remain ordered. The interconnect always provides responses in the same order as the commands issued. Slaves that support reordering provide a constant transaction ID to prevent reordering. AXI slaves that do not reorder are provided with transaction IDs, which allows exclusive accesses to be used for such slaves.

3.12.8. Read and Write Allocate

Read and write allocate does not apply to Platform Designer interconnect, which does not have caching features, and always receives responses from an endpoint.

3.12.9. Locked Transactions

Locked transactions are not supported for Platform Designer, version 14.0.

3.12.10. Memory Types

For AMBA 4 AXI, Platform Designer processes transactions as though the endpoint is a device memory type. For device memory types, using non-bufferable transactions to force previous bufferable transactions to finish is irrelevant, because Platform Designer interconnect always identifies transactions as being non-bufferable.

3.12.11. Mismatched Attributes

There are rules for how multiple masters issue cache values to a shared memory region. The interconnect meets requirements if signals are not modified.

3.12.12. Signals

Platform Designer supports up to 64-bits for the BUSER, WUSER and RUSER sideband signals. AMBA 4 AXI allows some signals to be omitted from interfaces by aligning them with the default values as defined in the AMBA Protocol Specifications on the ARM website.

Related Information
Arm AMBA Protocol Specifications

3.13. AMBA 4 AXI Streaming Interface Support (version 1.0)

3.13.1. Connection Points

Platform Designer allows you to connect an AMBA 4 AXI-Stream interface to another AMBA 4 AXI-Stream interface.

The connection is point-to-point without adaptation and must be between an axi4stream_master and axi4stream_slave. Connected interfaces must have the same port roles and widths.

Non matching master to slave connections, and multiple masters to multiple slaves connections are not supported.
3.13.1.1. AMBA 4 AXI Streaming Connection Point Parameters

Table 87. AMBA 4 AXI Streaming Connection Point Parameters

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>associatedClock</td>
<td>string</td>
<td>Name of associated clock interface.</td>
</tr>
<tr>
<td>associatedReset</td>
<td>string</td>
<td>Name of associated reset interface</td>
</tr>
</tbody>
</table>

3.13.1.2. AMBA 4 AXI Streaming Connection Point Signals

Table 88. AMBA 4 AXI-Stream Connection Point Signals

<table>
<thead>
<tr>
<th>Port Role</th>
<th>Width</th>
<th>Master Direction</th>
<th>Slave Direction</th>
<th>Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>tvalid</td>
<td>1</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>tready</td>
<td>1</td>
<td>Input</td>
<td>Output</td>
<td>No</td>
</tr>
<tr>
<td>tdata(4)</td>
<td>8:4096</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tstrb</td>
<td>1:512</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tkeep</td>
<td>1:512</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tid(5)</td>
<td>1:8</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tdest(6)</td>
<td>1:4</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tuser(7)</td>
<td>1:4096</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tlast</td>
<td>1</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
</tbody>
</table>

3.13.2. Adaptation

AMBA 4 AXI-Stream adaptation support is not available. AMBA 4 AXI-Stream master and slave interface signals and widths must match.


AMBA 4 AXI-Lite is a sub-set of AMBA 4 AXI. It is suitable for simpler control register-style interfaces that do not require the full functionality of AMBA 4 AXI.

---

(4) integer in multiple of bytes  
(5) maximum 8-bits  
(6) maximum 4-bits  
(7) number of bits in multiple of the number of bytes of tdata
Platform Designer 14.0 supports the following AMBA 4 AXI-Lite features:

- Transactions with a burst length of 1.
- Data accesses use the full width of a data bus (32-bit or 64-bit) for data accesses, and no narrow-size transactions.
- Non-modifiable and non-bufferable accesses.
- No exclusive accesses.

### 3.14.1. AMBA 4 AXI-Lite Signals

Platform Designer supports all AMBA 4 AXI-Lite interface signals. All signals are required.

<table>
<thead>
<tr>
<th>Global</th>
<th>Write Address Channel</th>
<th>Write Data Channel</th>
<th>Write Response Channel</th>
<th>Read Address Channel</th>
<th>Read Data Channel</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACLK</td>
<td>AWVALID</td>
<td>WVALID</td>
<td>BVALID</td>
<td>ARVALID</td>
<td>RVALID</td>
</tr>
<tr>
<td>ARESETn</td>
<td>AWREADY</td>
<td>WREADY</td>
<td>BREADY</td>
<td>ARREADY</td>
<td>RREADY</td>
</tr>
<tr>
<td>-</td>
<td>AWADDR</td>
<td>WDATA</td>
<td>BRESP</td>
<td>ARADDR</td>
<td>RDATA</td>
</tr>
<tr>
<td>-</td>
<td>AWPROT</td>
<td>WSTRB</td>
<td>-</td>
<td>ARPROT</td>
<td>RRESP</td>
</tr>
</tbody>
</table>

### 3.14.2. AMBA 4 AXI-Lite Bus Width

AMBA 4 AXI-Lite masters or slaves must have either 32-bit or 64-bit bus widths. Platform Designer interconnect inserts a width adapter if a master and slave pair have different widths.

### 3.14.3. AMBA 4 AXI-Lite Outstanding Transactions

AXI-Lite supports outstanding transactions. The options to control outstanding transactions is set in the parameter editor for the selected component.

### 3.14.4. AMBA 4 AXI-Lite IDs

AMBA 4 AXI-Lite does not support IDs. Platform Designer performs ID reflection inside the slave agent.
3.14.5. Connections Between AMBA 3 AXI, AMBA 4 AXI and AMBA 4 AXI-Lite

3.14.5.1. AMBA 4 AXI-Lite Slave Requirements

For an AMBA 4 AXI-Lite slave side, the master can be any master interface type, such as an Avalon (with bursting), AMBA 3 AXI, or AMBA 4 AXI. Platform Designer allows the following connections and inserts adapters, if needed.

- **Burst adapter**—Avalon and AMBA 3 AXI and AMBA 4 AXI bursting masters require a burst adapter to shorten the burst length to 1 before sending a transaction to an AMBA 4 AXI-Lite slave.
- Platform Designer interconnect uses a width adapter for mismatched data widths.
- Platform Designer interconnect performs ID reflection inside the slave agent.
- An AMBA 4 AXI-Lite slave must have an address width of at least 12-bits.
- AMBA 4 AXI-Lite does not have the $AXSIZE$ parameter. Narrow master to a wide AMBA 4 AXI-Lite slave is not supported. For masters that support narrow-sized bursts, for example, AMBA 3 AXI and AMBA 4 AXI, a burst to an AMBA 4 AXI-Lite slave must have a burst size equal to or greater than the slave's burst size.

3.14.5.2. AMBA 4 AXI-Lite Data Packing

Platform Designer interconnect does not support AMBA 4 AXI-Lite data packing.

3.14.6. AMBA 4 AXI-Lite Response Merging

When Platform Designer interconnect merges $SLVERR$ and $DECERR$, the error responses are not sticky. The response is based on priority and the master always sees a $DECERR$. When $SLVERR$ and $DECERR$ are merged, it is based on their priorities, not stickiness. $DECERR$ receives priority in this case, even if $SLVERR$ returns first.

3.15. Port Roles (Interface Signal Types)

Each interface defines signal roles and their behavior. Many signal roles are optional, allowing IP component designers the flexibility to select only the signal roles necessary to implement the required functionality.

3.15.1. AXI Master Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>araddr</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arburst</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>arcache</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>arid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>arlen</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>arlock</td>
<td>output</td>
<td>2</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>arprot</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>arready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>arsize</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>aruser</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>awaddr</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awburst</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>awcache</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>awid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>awlen</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>awlock</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>awprot</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>awready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>awsize</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>awuserid</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>bid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>bready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>bresp</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>bvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rdata</td>
<td>input</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>rid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>rlast</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rresp</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>rvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wdata</td>
<td>output</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>wid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>wlast</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>wready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wstrb</td>
<td>output</td>
<td>1, 2, 4, 8, 16, 32, 64, 128</td>
</tr>
<tr>
<td>wvalid</td>
<td>output</td>
<td>1</td>
</tr>
</tbody>
</table>
### 3.15.2. AXI Slave Interface Signal Types

#### Table 91. AXI Slave Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>araddr</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arburst</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>arcache</td>
<td>input</td>
<td>4</td>
</tr>
<tr>
<td>arid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>arlen</td>
<td>input</td>
<td>4</td>
</tr>
<tr>
<td>arlock</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>arprot</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>arready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>arsize</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>aruser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>awaddr</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awburst</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>awcache</td>
<td>input</td>
<td>4</td>
</tr>
<tr>
<td>awid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>awlen</td>
<td>input</td>
<td>4</td>
</tr>
<tr>
<td>awlock</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>awprot</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>awready</td>
<td>output</td>
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<tr>
<td>awsize</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>awuser</td>
<td>input</td>
<td>1 - 64</td>
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<tr>
<td>awvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>bid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>bready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>bresp</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>bvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rdata</td>
<td>output</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>rid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>rlast</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rresp</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>rvalid</td>
<td>output</td>
<td>1</td>
</tr>
</tbody>
</table>

*continued...*
### 3.15.3. AMBA 4 AXI Master Interface Signal Types

Table 92. AMBA 4 AXI Master Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>wdata</td>
<td>input</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>wid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>wlast</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>wstrb</td>
<td>input</td>
<td>1, 2, 4, 8, 16, 32, 64, 128</td>
</tr>
<tr>
<td>wvalid</td>
<td>input</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>araddr</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arburst</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>arcache</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>arid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>arlen</td>
<td>output</td>
<td>8</td>
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<td>output</td>
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<tr>
<td>arprot</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>arready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>arregion</td>
<td>output</td>
<td>1 - 4</td>
</tr>
<tr>
<td>arsize</td>
<td>output</td>
<td>3</td>
</tr>
<tr>
<td>aruser</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>awaddr</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awburst</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>awcache</td>
<td>output</td>
<td>4</td>
</tr>
<tr>
<td>awid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>awlen</td>
<td>output</td>
<td>8</td>
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<td>awlock</td>
<td>output</td>
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<tr>
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</tr>
<tr>
<td>awqos</td>
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<td>output</td>
<td>3</td>
</tr>
<tr>
<td>awuser</td>
<td>output</td>
<td>1 - 64</td>
</tr>
</tbody>
</table>

*continued...*
### 3.15.4. AMBA 4 AXI Slave Interface Signal Types

#### Table 93. AMBA 4 AXI Slave Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>awvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>bid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>bready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>bresp</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>buser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>bvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rdata</td>
<td>input</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>rid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>rlast</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rresp</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>ruser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>rvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wdata</td>
<td>output</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>wid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>wlast</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>wready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wstrb</td>
<td>output</td>
<td>1, 2, 4, 8, 16, 32, 64, 128</td>
</tr>
<tr>
<td>wuser</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>wvalid</td>
<td>output</td>
<td>1</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>arsize</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>aruser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>arvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>awaddr</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awburst</td>
<td>input</td>
<td>2</td>
</tr>
<tr>
<td>awcache</td>
<td>input</td>
<td>4</td>
</tr>
<tr>
<td>awid</td>
<td>input</td>
<td>1 - 18</td>
</tr>
<tr>
<td>awlen</td>
<td>input</td>
<td>8</td>
</tr>
<tr>
<td>awlock</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>awprot</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>awqos</td>
<td>input</td>
<td>1 - 4</td>
</tr>
<tr>
<td>awready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>awregion</td>
<td>input</td>
<td>1 - 4</td>
</tr>
<tr>
<td>awsize</td>
<td>input</td>
<td>3</td>
</tr>
<tr>
<td>awuser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>awvalid</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>bid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>bready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>bresp</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>bvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rdata</td>
<td>output</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>rid</td>
<td>output</td>
<td>1 - 18</td>
</tr>
<tr>
<td>rlast</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>rready</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>rresp</td>
<td>output</td>
<td>2</td>
</tr>
<tr>
<td>ruser</td>
<td>output</td>
<td>1 - 64</td>
</tr>
<tr>
<td>rvalid</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>wdata</td>
<td>input</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
</tr>
<tr>
<td>wlast</td>
<td>input</td>
<td>1</td>
</tr>
<tr>
<td>wready</td>
<td>output</td>
<td>1</td>
</tr>
<tr>
<td>wstrb</td>
<td>input</td>
<td>1, 2, 4, 8, 16, 32, 64, 128</td>
</tr>
<tr>
<td>wuser</td>
<td>input</td>
<td>1 - 64</td>
</tr>
<tr>
<td>wvalid</td>
<td>input</td>
<td>1</td>
</tr>
</tbody>
</table>
3.15.5. AMBA 4 AXI-Stream Master and Slave Interface Signal Types

Table 94. AMBA 4 AXI-Stream Master and Slave Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Master Direction</th>
<th>Slave Direction</th>
<th>Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>tvalid</td>
<td>1</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>tready</td>
<td>1</td>
<td>Input</td>
<td>Output</td>
<td>No</td>
</tr>
<tr>
<td>tdata</td>
<td>8:4096</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tstrb</td>
<td>1:512</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tkeep</td>
<td>1:512</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tid</td>
<td>1:8</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tdest</td>
<td>1:4</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tuser</td>
<td>1</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
<tr>
<td>tlast</td>
<td>1:4096</td>
<td>Output</td>
<td>Input</td>
<td>No</td>
</tr>
</tbody>
</table>

3.15.6. ACE-Lite Interface Signal Roles

Table 95. ACE-Lite Interface Signal Roles

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Master Direction</th>
<th>Slave Direction</th>
<th>Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>arsnoop</td>
<td>4 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>ardomain</td>
<td>2 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>arbar</td>
<td>2 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>awsnoop</td>
<td>3 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>awdomain</td>
<td>2 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>awbar</td>
<td>2 bits</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
<tr>
<td>awunique</td>
<td>1 bit</td>
<td>Output</td>
<td>Input</td>
<td>Yes</td>
</tr>
</tbody>
</table>

3.15.7. APB Interface Signal Types

Table 96. APB Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Direction APB Master</th>
<th>Direction APB Slave</th>
<th>Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>paddr</td>
<td>[1:32]</td>
<td>output</td>
<td>input</td>
<td>yes</td>
</tr>
<tr>
<td>psel</td>
<td>[1:16]</td>
<td>output</td>
<td>input</td>
<td>yes</td>
</tr>
<tr>
<td>penable</td>
<td>1</td>
<td>output</td>
<td>input</td>
<td>yes</td>
</tr>
<tr>
<td>pwrite</td>
<td>1</td>
<td>output</td>
<td>input</td>
<td>yes</td>
</tr>
<tr>
<td>pwdata</td>
<td>[1:32]</td>
<td>output</td>
<td>input</td>
<td>yes</td>
</tr>
<tr>
<td>prdata</td>
<td>[1:32]</td>
<td>input</td>
<td>output</td>
<td>yes</td>
</tr>
</tbody>
</table>

continued...
3.15.8. Avalon Memory Mapped Interface Signal Roles

Signal roles define the signal types that Avalon memory mapped master and slave ports allow.

This specification does not require all signals to exist in an Avalon memory mapped interface. There is no one signal that is always required. The minimum requirements for an Avalon memory mapped interface are `readdata` for a read-only interface, or `writedata` and `write` for a write-only interface.

The following table lists signal roles for the Avalon memory mapped interface:

### Table 97. Avalon Memory Mapped Signal Roles

Some Avalon memory mapped signals can be active high or active low. When active low, the signal name ends with `_n`.

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fundamental Signals</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>address</td>
<td>1 - 64</td>
<td>Master → Slave</td>
<td>No</td>
<td>Masters: By default, the address signal represents a byte address. The value of the address must align to the data width. To write to specific bytes within a data word, the master must use the byteenable signal. Refer to the addressUnits interface property for word addressing. Slaves: By default, the interconnect translates the byte address into a word address in the slave’s address space. From the perspective of the slave, each slave access is for a word of data. For example, address = 0 selects the first word of the slave. address = 1 selects the second word of the slave. Refer to the addressUnits interface property for byte addressing.</td>
</tr>
<tr>
<td>byteenable</td>
<td>2, 4, 8, 16, 32, 64, 128</td>
<td>Master → Slave</td>
<td>No</td>
<td>Enables one or more specific byte lanes during transfers on interfaces of width greater than 8 bits. Each bit in byteenable corresponds to a byte in writedata and readdata. The master bit <code>&lt;n&gt;</code> of byteenable indicates whether byte <code>&lt;n&gt;</code> is being written to. During writes, byteenables specify which bytes are being written to. Other bytes should be ignored by the slave. During reads, byteenables indicate which bytes the master is reading. Slaves that simply return readdata with no side effects are free to ignore byteenables during reads. If an interface does not have a byteenable signal, the transfer proceeds as if all byteenables are asserted. When more than one bit of the byteenable signal is asserted, all asserted lanes are adjacent.</td>
</tr>
<tr>
<td>debugaccess</td>
<td>1</td>
<td>Master → Slave</td>
<td>No</td>
<td>When asserted, allows the Nios II processor to write on-chip memories configured as ROMs.</td>
</tr>
<tr>
<td>read</td>
<td>1</td>
<td>Master → Slave</td>
<td>No</td>
<td>Asserted to indicate a read transfer. If present, readdata is required.</td>
</tr>
<tr>
<td>read_n</td>
<td></td>
<td></td>
<td></td>
<td>continued...</td>
</tr>
<tr>
<td>Signal Role</td>
<td>Width</td>
<td>Direction</td>
<td>Required</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>----------------</td>
<td>--------------</td>
<td>----------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>readdata</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
<td>Slave → Master</td>
<td>No</td>
<td>The readdata driven from the slave to the master in response to a read transfer. Required for interfaces that support reads.</td>
</tr>
<tr>
<td>response</td>
<td>2</td>
<td>Slave → Master</td>
<td>No</td>
<td>The response signal is an optional signal that carries the response status. Note: Because the signal is shared, an interface cannot issue or accept a write response and a read response in the same clock cycle.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 00: OKAY—Successful response for a transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 01: RESERVED—Encoding is reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 10: SLAVEERROR—Error from an endpoint slave. Indicates an unsuccessful transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 11: DECODEERROR—Indicates attempted access to an undefined location.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For read responses:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• One response is sent with each readdata. A read burst length of N results in N responses. Fewer responses are not valid, even in the event of an error. The response signal value may be different for each readdata in the burst.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The interface must have read control signals. Pipeline support is possible with the readdatavalid signal.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• On read errors, the corresponding readdata is &quot;don't care&quot;.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>For write responses:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• One write response must be sent for each write command. A write burst results in only one response, which must be sent after the final write transfer in the burst is accepted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• If writeresponsevalid is present, all write commands must be completed with write responses.</td>
</tr>
<tr>
<td>write</td>
<td>1</td>
<td>Master → Slave</td>
<td>No</td>
<td>Asserted to indicate a write transfer. If present, writedata is required.</td>
</tr>
<tr>
<td>write_n</td>
<td></td>
<td>Slave</td>
<td></td>
<td>Data for write transfers. The width must be the same as the width of readdata if both are present. Required for interfaces that support writes.</td>
</tr>
<tr>
<td>writedata</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024</td>
<td>Master → Slave</td>
<td>No</td>
<td>Data for write transfers. The width must be the same as the width of readdata if both are present. Required for interfaces that support writes.</td>
</tr>
</tbody>
</table>

**Wait-State Signals**

<table>
<thead>
<tr>
<th>Signal</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>lock</td>
<td>1</td>
<td>Master → Slave</td>
<td>No</td>
<td>lock ensures that once a master wins arbitration, the winning master maintains access to the slave for multiple transactions. Lock asserts coincident with the first read or write of a locked sequence of transactions. Lock deasserts on the final transaction of a locked sequence of transactions. Lock assertion does not guarantee that arbitration is won. After the lock-asserting master has been granted, that master retains grant until lock is deasserted. A master equipped with lock cannot be a burst master. Arbitration priority values for lock-equipped masters are ignored.</td>
</tr>
</tbody>
</table>

*continued...*
Lock is particularly useful for read-modify-write (RMW) operations. The typical read-modify-write operation includes the following steps:

1. Master A asserts lock and reads 32-bit data that has multiple bit fields.
2. Master A deasserts lock, changes one bit field, and writes the 32-bit data back.

Lock prevents master B from performing a write between Master A's read and write.

### Pipeline Signals

**readdatavalid**

- **Width**: 1
- **Direction**: Slave → Master
- **Required**: No

Used for variable-latency, pipelined read transfers. When asserted, indicates that the `readdata` signal contains valid data. For a read burst with `burstcount` value `<n>`, the `readdatavalid` signal must be asserted `<n>` times, once for each `readdata` item. There must be at least one cycle of latency between acceptance of the `read` and assertion of `readdatavalid`. For a timing diagram illustrating the `readdatavalid` signal, refer to the figure in *Pipelined Read Transfer with Variable Latency*.

A slave may assert `readdatavalid` to transfer data to the master independently of whether the slave is stalling a new command with `waitrequest`.

Required if the master supports pipelined reads. Bursting masters with read functionality must include the `readdatavalid` signal.

**writeresponsevalid**

- **Width**: 1
- **Direction**: Slave → Master
- **Required**: No

An optional signal. If present, the interface issues write responses for write commands. When asserted, the value on the response signal is a valid write response. `writeresponsevalid` is only asserted one clock cycle or more after the write command is accepted. There is at least a one clock cycle latency from command acceptance to assertion of `writeresponsevalid`.

A write command is considered accepted when the last beat of the burst is issued to the slave and `waitrequest` is low. `writeresponsevalid` can be asserted one or more clock cycles after the last beat of the burst has been issued.

### Burst Signals

**burstcount**

- **Width**: 1 - 11
- **Direction**: Master → Slave
- **Required**: No

Used by bursting masters to indicate the number of transfers in each burst. The value of the maximum `burstcount` parameter must be a power of 2. A `burstcount` interface of width `<n>` can

---

**waitrequest**

- **Width**: 1
- **Direction**: Slave → Master
- **Required**: No

A slave asserts `waitrequest` when unable to respond to a `read` or `write` request. Forces the master to wait until the interconnect is ready to proceed with the transfer. At the start of all transfers, a master initiates the transfer and waits until `waitrequest` is deasserted. A master must make no assumption about the assertion state of `waitrequest` when the master is idle; `waitrequest` may be high or low, depending on system properties.

When `waitrequest` is asserted, master control signals to the slave must remain constant except for `beginbursttransfer`. For a timing diagram illustrating the `beginbursttransfer` signal, refer to the figure in *Read Bursts*.

An Avalon memory mapped slave may assert `waitrequest` during idle cycles. An Avalon memory mapped master may initiate a transaction when `waitrequest` is asserted and wait for that signal to be deasserted. To avoid system lockup, a slave device should assert `waitrequest` when in reset.

**Pipeline Signals**

- **readdatavalid**
- **writevalid**

---

**Burst Signals**

- **burstcount**

---

**Signal Role** | **Width** | **Direction** | **Required** | **Description**
--- | --- | --- | --- | ---
Lock | 1 | Slave → Master | No | A slave asserts `waitrequest` when unable to respond to a `read` or `write` request. Forces the master to wait until the interconnect is ready to proceed with the transfer. At the start of all transfers, a master initiates the transfer and waits until `waitrequest` is deasserted. A master must make no assumption about the assertion state of `waitrequest` when the master is idle; `waitrequest` may be high or low, depending on system properties.

When `waitrequest` is asserted, master control signals to the slave must remain constant except for `beginbursttransfer`. For a timing diagram illustrating the `beginbursttransfer` signal, refer to the figure in *Read Bursts*.

An Avalon memory mapped slave may assert `waitrequest` during idle cycles. An Avalon memory mapped master may initiate a transaction when `waitrequest` is asserted and wait for that signal to be deasserted. To avoid system lockup, a slave device should assert `waitrequest` when in reset.

**Pipeline Signals**

- **readdatavalid**
- **writevalid**

---

**Burst Signals**

- **burstcount**
encode a max burst of size $2^{(n-1)}$. For example, a 4-bit burstcount signal can support a maximum burst count of 8. The minimum burstcount is 1. The constantBurstBehavior property controls the timing of the burstcount signal. Bursting masters with read functionality must include the readdatavalid signal.

For bursting masters and slaves using byte addresses, the following restriction applies to the width of the address:

$$<\text{address}_w> = <\text{burstcount}_w> + \log_2(<\text{symbols_per_word_of_interface}>)$$

For bursting masters and slaves using word addresses, the $\log_2$ term above is omitted.

**beginbursttransfer** is optional. A slave can always internally calculate the start of the next write burst transaction by counting data transfers.

**Warning:** do not use this signal. This signal exists to support legacy memory controllers.

### 3.15.9. Avalon Streaming Interface Signal Roles

Each signal in an Avalon streaming source or sink interface corresponds to one Avalon streaming signal role. An Avalon streaming interface may contain only one instance of each signal role. All Avalon streaming signal roles apply to both sources and sinks and have the same meaning for both.

#### Table 98. Avalon Streaming Interface Signals

In the following table, all signal roles are active high.

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fundamental Signals</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>channel</td>
<td>1 – 128</td>
<td>Source → Sink</td>
<td>No</td>
<td>The channel number for data being transferred on the current cycle. If an interface supports the channel signal, the interface must also define the maxChannel parameter.</td>
</tr>
<tr>
<td>data</td>
<td>1 – 8,192</td>
<td>Source → Sink</td>
<td>No</td>
<td>The data signal from the source to the sink, typically carries the bulk of the information being transferred. Parameters further define the contents and format of the data signal.</td>
</tr>
<tr>
<td>error</td>
<td>1 – 256</td>
<td>Source → Sink</td>
<td>No</td>
<td>A bit mask to mark errors affecting the data being transferred in the current cycle. A single bit of the error signal masks each of the errors the component recognizes. The errorDescriptor defines the error signal properties.</td>
</tr>
</tbody>
</table>
### 3.15.10. Avalon Streaming Credit Interface Signal Roles

Each signal in an Avalon Streaming Credit source or sink interface corresponds to one Avalon Streaming Credit signal role. An Avalon Streaming Credit interface may contain only one instance of each signal role. All Avalon Streaming Credit signal roles apply to both sources and sinks and have the same meaning for both.

#### Table 99. Avalon Streaming Credit Interface Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Direction</th>
<th>Width</th>
<th>Optional / Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>update</td>
<td>Sink to source</td>
<td>1</td>
<td>Required</td>
<td>Sink sends update and source updates the available credit counter. Sink sends update to source when a transaction is popped from its buffer. Credit counter in source is increased by the value on the credit bus from sink to source.</td>
</tr>
<tr>
<td>credit</td>
<td>Sink to source</td>
<td>1-9</td>
<td>Required</td>
<td>Indicates additional credit available at sink when update is asserted. This bus carries a value as specified by the sink. Width of the credit bus is ceilog2(MAX_CREDIT + 1). Sink sends available credit value on this bus which indicates the number of transactions it can accept. Source captures credit value only if update signal is asserted.</td>
</tr>
</tbody>
</table>
### Signal Name | Direction | Width | Optional / Required | Description
--- | --- | --- | --- | ---
**return_credit** | Source to sink | 1 | Required | Asserted by source to return 1 credit back to sink.  
*Note:* For more details, refer to Section 6.2.3 *Returning the Credits.*

data | Source to sink | 1-16368 | Required | Data is divided into symbols as per existing Avalon Streaming definition.
*valid* | Source to sink | 1 | Required | Asserted by the source to qualify all other source to sink signals. Source can assert *valid* only when the credit available to it is greater than 0.
*error* | Source to sink | 1-256 | Optional | A bit mask used to mark errors affecting the data being transferred in the current cycle. A single bit in error is used for each of the errors recognized by the component, as defined by the *errorDescriptor* property.
*channel* | Source to sink | 1-128 | Optional | The channel number for data being transferred on the current cycle. If an interface supports the *channel* signal, it must also define the *maxChannel* parameter.

**Packet Transfer Signals**

| Signal Name | Direction | Width | Optional / Required | Description
--- | --- | --- | --- | ---
*startofpacket* | Source to sink | 1 | Optional | Asserted by the source to mark the start of a packet.
*endofpacket* | Source to sink | 1 | Optional | Asserted by the source to mark the end of a packet.
*empty* | Source to sink | ceil(log2(NUM_SYMBOLS)) | Optional | Indicates the number of symbols that are empty, that is, do not represent valid data. The *empty* signal is not used on interfaces where there is one symbol per beat.

**User Signals**

| Signal Name | Direction | Width | Optional / Required | Description
--- | --- | --- | --- | ---
*<Per-Packet User Signals>* | Source to sink | 1-16368 | Optional | Any number of per-packet user signals can be present on source and sink interfaces. Source sets value of this signal when *startofpacket* is asserted. Source should not change the value of this signal until start of new packet. More details are in the User Signal section.
*<Per-Symbol User Signals>* | Source to sink | 1-16368 | Optional | Any number of per-symbol user signals can be present on source and sink. More details are in the User Signal section.

### 3.15.10.1. Synchronous Interface

All transfers of an Avalon Streaming connection occur synchronous to the rising edge of the associated clock signal. All outputs from a source interface to a sink interface, including the *data*, *channel*, and *error* signals, must be registered on the rising edge of clock. Inputs to a sink interface do not have to be registered. Registering signals at the source facilitates high-frequency operation.
Table 100.  Avalon Streaming Credit Interface Properties

<table>
<thead>
<tr>
<th>Property Name</th>
<th>Default Value</th>
<th>Legal Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>associatedClock</td>
<td>1</td>
<td>Clock interface</td>
<td>The name of the Avalon Clock interface to which this Avalon Streaming interface is synchronous.</td>
</tr>
<tr>
<td>associatedReset</td>
<td>1</td>
<td>Reset interface</td>
<td>The name of the Avalon Reset interface to which this Avalon Streaming interface is synchronous.</td>
</tr>
<tr>
<td>dataBitsPerSymbol</td>
<td>8</td>
<td>1 – 16368</td>
<td>Defines the number of bits per symbol. For example, byte-oriented interfaces have 8-bit symbols. This value is not restricted to be a power of 2.</td>
</tr>
<tr>
<td>symbolsPerBeat</td>
<td>1</td>
<td>1 – 16368</td>
<td>The number of symbols that are transferred on every valid cycle.</td>
</tr>
<tr>
<td>maxCredit</td>
<td>256</td>
<td>1-256</td>
<td>The maximum number of credits that a data interface can support.</td>
</tr>
<tr>
<td>errorDescriptor</td>
<td>0</td>
<td>List of strings</td>
<td>A list of words that describe the error associated with each bit of the error signal. The length of the list must be the same as the number of bits in the error signal. The first word in the list applies to the highest order bit. For example, “crc, overflow” means that bit[1] of error indicates a CRC error. Bit[0] indicates an overflow error.</td>
</tr>
<tr>
<td>firstSymbolInHighOrderBits</td>
<td>true</td>
<td>true, false</td>
<td>When true, the first-order symbol is driven to the most significant bits of the data interface. The highest-order symbol is labeled D0 in this specification. When this property is set to false, the first symbol appears on the low bits. D0 appears at data[7:0]. For a 32-bit bus, if true, D0 appears on bits[31:24].</td>
</tr>
<tr>
<td>maxChannel</td>
<td>0</td>
<td>0</td>
<td>The maximum number of channels that a data interface can support.</td>
</tr>
</tbody>
</table>

3.15.10.2. Typical Data Transfers

This section defines the transfer of data from a source interface to a sink interface. In all cases, the data source and the data sink must comply with the specification. It is not the responsibility of the data sink to detect source protocol errors.

The below figure shows the signals that are typically used in an Avalon Streaming Credit interface.
Figure 130. Typical Avalon Streaming Credit Signals

As this figure indicates, a typical Avalon Streaming Credit source interface drives the valid, data, error, and channel signals to the sink. The sink drives update and credit signals.

Figure 131. Typical Credit and Data Transfer

The above figure shows a typical credit and data transfer between source and sink. There can be an arbitrary delay between the sink asserting update and source receiving the update. Similarly, there can be an arbitrary delay between source asserting valid for data and sink receiving that data. Delay on credit path from sink to source and data path from source to sink need not be equal. These delays can be 0 cycle as well, i.e. when the sink asserts update, it is seen by the source in the same cycle. Conversely, when the source asserts valid, it is seen by the sink in the same cycle. If source has zero credits, it cannot assert valid. Transferred credits are cumulative. If sink has transferred credits equal to its maxCredit property, and has not received any data, it cannot assert update until it receives at least 1 data or has received a return_credit pulse from the source.

Sink cannot backpressure data from source if sink has provided credits to the source, i.e. sink must accept data from source if there are outstanding credits. Source cannot assert valid if it has not received any credit or exhausted the credits received, i.e. already sent the data in lieu of credits received.
If source has zero credits, source cannot start the data transfer in the same cycle it receives credits. Similarly, if sink has transferred credits equal to its maxCredit property and it receives data, sink cannot send an update in the same cycle as it received data. These restrictions have been put in place to avoid combinational loops in the implementation.

### 3.15.10.3. Returning the Credits

Avalon Streaming Credit protocol supports a `return_credit` signal. This is used by source to return the credits back to sink. Every cycle this signal is asserted, it indicates source is giving back 1 credit. If source wants to return multiple credits, this signal needs to be asserted for multiple cycles. For example, if source wants to return 10 outstanding credits, it asserts `return_credit` signal for 10 cycles. Sink should account for returned credits in its internal credit maintenance counters. Credits can be returned by source at any point in time as long as it has credits greater than 0.

The below figure exemplifies source returning credits. As shown in the figure, `outstanding_credit` is an internal counter for the source. When source returns credits, this counter is decremented.

**Figure 132. Source Returning Credits**

![Image of source returning credits]

**Note:** Although the diagram above shows the returning of credits when `valid` is deasserted, `return_credit` can also be asserted while `valid` is asserted. In this case, source effectively spends 2 credits: one for `valid`, and one for `return_credit`.

### 3.15.11. Avalon Streaming Credit User Signals

User signals are optional sideband signals which flow along with data. They are considered valid only when data is valid. Given that user signals do not have any defined meaning or purpose, caution must be used while using these signals. It is the responsibility of the system designer to make sure that two IPs connected to each other agree on the roles of the user signals.

Two types of user signals are being proposed: per-symbol user signals and per-packet user signals.
3.15.11.1. Per-Symbol User Signal

As the name suggests, the data defines a per-symbol user signal \(\text{symbol\_user}\) per symbol. Each symbol in the data can have a user signal. For example, if the number of symbols in the data is 8, and \text{symbol\_user} width is 2 bits, the total width of the \text{symbol\_user} signal is 16 bits.

\(\text{Symbol\_user}\) is valid only when data is valid. Source can change this signal every cycle when data is valid. Sink can disregard the value of \text{symbol\_user} bits for empty symbols.

If a source which has this signal is connected to a sink which does not have this signal on its interface, the signal from source remains dangling in the generated interconnect.

If a source which does not have this signal is connected to a sink which has this signal on its interface, the sink’s input user signal ties to 0.

If both source and sink have equal number of symbols in the data, then the user signals for both must have equal widths. Otherwise, they cannot be connected.

If a wide source is connected to a narrow sink, and both have per-symbol user signals, then both must have equal bits of user signal associated with each symbol. For example, if a 16-symbol source has 2 bits of user signal associated with each symbol (for a total of 32 bits of user signal), then a 4-symbol sink must have an 8-bit wide user signal (2 bits associated with each symbol). A data format adapter can convert the 16-symbol source data to 4-symbol sink data, and 32-bit user signal to 8-bit user signal. The data format adapter maintains the association of symbols with corresponding user signal bits.

Similarly, if a narrow source is connected to a wide sink, and both have per-symbol user signals, then both must have equal bits of user signal associated with each symbol. For example, if a 4-symbol source has 2 bits of user signal associated with each symbol (for a total of 8 bits of user signal), then a 16-symbol sink must have a 32-bit wide user signal (2 bits associated with each symbol). A data format adapter can convert the 4-symbol source data to 16-symbol sink data, and 8-bit user signal to 32-bit user signal. The data format adapter maintains the association of symbols with corresponding user signal bits. If the packet is smaller than the ratio of data widths, the data format adapter sets the value of empty accordingly. Sink should disregard the value of user bits associated with empty symbols.

3.15.11.2. Per-Packet User Signal

In addition to \text{symbol\_user}, per-packet user signals (\text{packet\_user}) can also be declared on the interface. \text{Packet\_user} can be of arbitrary width. Unlike \text{symbol\_user}, \text{packet\_user} must remain constant throughout the packet, i.e. its value should be set at the start of the packet and must remain the same until the end of the packet. This restriction makes the implementation of the data format adapter simpler as it eliminates the option to replicate or chop (wide source, narrow sink) or concatenate (narrow source, wide sink) \text{packet\_user}.

If a source has \text{packet\_user} and sink does not, the \text{packet\_user} from source remains dangling. In such a case, the system designer must be careful and not transmit any critical control information on this signal as it is completely or partially ignored.
If a source does not have `packet_user` and the sink does, the `packet_user` to sink is tied to 0.

### 3.15.12. Avalon Clock Source Signal Roles

An Avalon Clock source interface drives a clock signal out of a component.

**Table 101. Clock Source Signal Roles**

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>1</td>
<td>Output</td>
<td>Yes</td>
<td>An output clock signal.</td>
</tr>
</tbody>
</table>

### 3.15.13. Avalon Clock Sink Signal Roles

A clock sink provides a timing reference for other interfaces and internal logic.

**Table 102. Clock Sink Signal Roles**

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>1</td>
<td>Input</td>
<td>Yes</td>
<td>A clock signal. Provides synchronization for internal logic and for other interfaces.</td>
</tr>
</tbody>
</table>

### 3.15.14. Avalon Conduit Signal Roles

**Table 103. Conduit Signal Roles**

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;any&gt;</td>
<td>&lt;n&gt;</td>
<td>In, out, or bidirectional</td>
<td>A conduit interface consists of one or more input, output, or bidirectional signals of arbitrary width. Conduits can have any user-specified role. You can connect compatible Conduit interfaces inside a Platform Designer system provided the roles and widths match and the directions are opposite.</td>
</tr>
</tbody>
</table>

### 3.15.15. Avalon Tristate Conduit Signal Roles

The following table lists the signal defined for the Avalon Tristate Conduit interface. All Avalon-TC signals apply to both masters and slaves and have the same meaning for both

**Table 104. Tristate Conduit Interface Signal Roles**

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
</table>
| request     | 1     | Master → Slave | Yes | The meaning of request depends on the state of the grant signal, as the following rules dictate.  
  When request is asserted and grant is deasserted, request is requesting access for the current cycle.  
  When request is asserted and grant is asserted, request is requesting access for the next cycle.  
  Consequently, request should be deasserted on the final cycle of an access.  
  The request signal deasserts in the last cycle of a bus access. The request signal can reassert immediately following the final cycle of a transfer. |

*continued...*
This protocol makes both rearbitration and continuous bus access possible if no other masters are requesting access. Once asserted, request must remain asserted until granted. Consequently, the shortest bus access is 2 cycles. Refer to *Tristate Conduit Arbitration Timing* for an example of arbitration timing.

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>grant</td>
<td>1</td>
<td>Slave → Master</td>
<td>Yes</td>
<td>When asserted, indicates that a tristate conduit master has access to perform transactions. The grant signal asserts in response to the request signal. The grant signal remains asserted until 1 cycle following the deassertion of request.</td>
</tr>
<tr>
<td>&lt;name&gt;_in</td>
<td>1 – 1024</td>
<td>Slave → Master</td>
<td>No</td>
<td>The input signal of a logical tristate signal.</td>
</tr>
<tr>
<td>&lt;name&gt;_out</td>
<td>1 – 1024</td>
<td>Master → Slave</td>
<td>No</td>
<td>The output signal of a logical tristate signal.</td>
</tr>
<tr>
<td>&lt;name&gt;_outen</td>
<td>1</td>
<td>Master → Slave</td>
<td>No</td>
<td>The output enable for a logical tristate signal.</td>
</tr>
</tbody>
</table>
3.15.16. Avalon Tri-State Slave Interface Signal Types

Table 105. Tri-state Slave Interface Signal Types

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>address</td>
<td>1 - 32</td>
<td>input</td>
<td>No</td>
<td>Address lines to the slave port. Specifies a byte offset into the slave’s address space.</td>
</tr>
<tr>
<td>read</td>
<td>1</td>
<td>input</td>
<td>No</td>
<td>Read-request signal. Not required if the slave port never outputs data. If present, data must also be used.</td>
</tr>
<tr>
<td>write</td>
<td>1</td>
<td>input</td>
<td>No</td>
<td>Write-request signal. Not required if the slave port never receives data from a master. If present, data must also be present, and writebyteenable cannot be present.</td>
</tr>
<tr>
<td>chipselect</td>
<td>1</td>
<td>input</td>
<td>No</td>
<td>When present, the slave port ignores all Avalon memory mapped signals unless chipselect is asserted. chipselect is always present in combination with read or write</td>
</tr>
<tr>
<td>outputenable</td>
<td>1</td>
<td>input</td>
<td>Yes</td>
<td>Output-enable signal. When deasserted, a tri-state slave port must not drive its data lines otherwise data contention may occur.</td>
</tr>
<tr>
<td>data</td>
<td>8,16, 32, 64, 128, 256, 512, 1024</td>
<td>bidir</td>
<td>No</td>
<td>Bidirectional data. During write transfers, the FPGA drives the data lines. During read transfers the slave device drives the data lines, and the FPGA captures the data signals and provides them to the master.</td>
</tr>
<tr>
<td>byteenable</td>
<td>2, 4, 8,16, 32, 64, 128</td>
<td>input</td>
<td>No</td>
<td>Enables specific byte lanes during transfers. Each bit in byteenable corresponds to a byte lane in data. During writes, byteenable specifies which bytes the master is writing to the slave. During reads, byteenable indicates which bytes the master is reading. Slaves that simply return data with no side effects are free to ignore byteenable during reads. When more than one byte lane is asserted, all asserted lanes are guaranteed to be adjacent. The number of adjacent lines must be a power of 2, and the specified bytes must be aligned on an address boundary for the size of the data. The following are legal values for a 32-bit slave:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1111 writes full 32 bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0011 writes lower 2 bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1100 writes upper 2 bytes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0001 writes byte 0 only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0010 writes byte 1 only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0100 writes byte 2 only</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1000 writes byte 3 only</td>
</tr>
</tbody>
</table>
### 3.15.17. Avalon Interrupt Sender Signal Roles

Table 106. Interrupt Sender Signal Roles

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>irq</td>
<td>1–32</td>
<td>Output</td>
<td>Yes</td>
<td>Interrupt Request. An interrupt sender drives an interrupt signal to an interrupt receiver.</td>
</tr>
<tr>
<td>irq_n</td>
<td>1–32</td>
<td>Output</td>
<td>Yes</td>
<td>irq is an &lt;n&gt;-bit vector, where each bit corresponds directly to one IRQ sender with no inherent assumption of priority.</td>
</tr>
</tbody>
</table>

### 3.15.18. Avalon Interrupt Receiver Signal Roles

Table 107. Interrupt Receiver Signal Roles

<table>
<thead>
<tr>
<th>Signal Role</th>
<th>Width</th>
<th>Direction</th>
<th>Required</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>irq</td>
<td>1–32</td>
<td>Input</td>
<td>Yes</td>
<td>irq is an &lt;n&gt;-bit vector, where each bit corresponds directly to one IRQ sender with no inherent assumption of priority.</td>
</tr>
</tbody>
</table>

### 3.16. Platform Designer Interconnect Revision History

The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020.06.26</td>
<td>20.1</td>
<td>Removed incorrect statement about compile time option to enforce strict ordering from the &quot;AXI and Avalon Ordering&quot; topic.</td>
</tr>
<tr>
<td>2020.05.08</td>
<td>20.1</td>
<td>Added some clarification for the timing behavior of the signal writeresponsevalid to the Avalon Memory-Mapped Interface Signal Roles section. Updated the bus widths for the data and empty signals in the Avalon Streaming Interface Signal Roles section.</td>
</tr>
</tbody>
</table>
| 2020.05.01       | 20.1                       | • Updated "Avalon Streaming Credit Interface Signal Roles" to indicate that return_credit is required.  
                      • Added "Avalon Streaming Credit Interfaces" section.  
                      • Added "Avalon Streaming Credit Interface Signal Roles" topic.  
                      • Added "Avalon Streaming Credit User Signals" topic. |
| 2019.11.11       | 19.1.0                     | • Added note to "Burst Adaptation: AXI to Avalon" about AXI3 and AXI4  
                      4KB boundary restriction for burst transactions.  
                      • Added "Adjacent Bytelanes with Partial Width Transactions" topic. |
| 2019.06.19       | 19.1.0                     | • Corrected statement about preventing reordering in "Ordering Model." |
| 2019.04.01       | 19.1.0                     | • Described new default use of synchronous reset option for Intel Stratix  
                      10 designs in "Reset Interfaces." |

continued...
<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.12.10</td>
<td>18.1.0</td>
<td>• Replaced references to System Contents tab with new System View tab.</td>
</tr>
</tbody>
</table>
| 2018.09.24       | 18.1.0                      | • Updated location of *Limit interconnect pipeline stages to* option in Platform Designer GUI.  
In Avalon Memory-Mapped Interface Signal Roles, added consecutive byte-enable support.  
Specified minimum duration of reset that the Platform Design Interconnect requires to work correctly. |
| 2018.06.15       | 18.0.0                      | Clarified behavior of Error Correction Coding (ECC) in Interconnect. |
| 2018.05.07       | 18.0.0                      | • Added support for *waitrequestAllowance* adapter.  
• Added support for ACE-Lite connections. |
| 2017.11.06       | 17.1.0                      | • Changed instances of Qsys Pro to Platform Designer  
• Updated information about the Reset Sequencer. |
| 2016.10.31       | 16.1.0                      | • Implemented Intel rebranding.  
• Implemented Qsys rebranding. |
| 2015.11.02       | 15.1.0                      | Changed instances of Quartus II to Quartus Prime. |
| 2015.05.04       | 15.0.0                      | • Fixed Priority Arbitration.  
• Added topic: *Read and Write Responses.*  
• Added topic: *Error Correction Coding (ECC) in Qsys Interconnect.*  
• Added: *response [1:0], Avalon Memory-Mapped Interface Signal Roles.*  
• Added *writeresponsevalid, Avalon Memory-Mapped Interface Signal Roles.* |
| December 2014    | 14.1.0                      | • Read error responses, Avalon Memory-Mapped Interface Signal, response.  
• Burst Adapter Implementation Options: Generic converter (slower, lower area), Per-burst-type converter (faster, higher area). |
| August 2014      | 14.0a10.0                   | • Updated Qsys Packet Format for Memory-Mapped Master and Slave Interfaces table, *Protection.*  
• Streaming Interface renamed to Avalon Streaming Interfaces.  
• Added *Response Merging under Memory-Mapped Interfaces.* |
| June 2014        | 14.0.0                      | • AXI4-Lite support.  
• AXI4-Stream support.  
• Avalon streaming adapter parameters.  
• IRQ Bridge.  
• Handling Read Side Effects note added. |
| November 2013    | 13.1.0                      | • HSSI clock support.  
• Reset Sequencer.  
• Interconnect pipelining. |
| May 2013         | 13.0.0                      | • AMBA APB support.  
• Auto-inserted Avalon streaming adapters feature.  
• Moved Address Span Extender to the Qsys System Design Components chapter. |
| November 2012    | 12.1.0                      | • AMBA AXI4 support. |
| June 2012        | 12.0.0                      | • AMBA AXI3 support.  
• Avalon streaming adapters.  
• Address Span Extender. |

*continued...*
<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 2011</td>
<td>11.0.1</td>
<td>Template update.</td>
</tr>
<tr>
<td>May 2011</td>
<td>11.0.0</td>
<td>Removed beta status.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.1.0</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
4. Optimizing Platform Designer System Performance

Platform Designer provides tools that allow you to optimize the performance of the system interconnect for Intel FPGA designs. This chapter presents techniques that leverage the available tools and the trade-offs of each implementation.

Note: Intel now refers to Qsys Pro as Platform Designer.

The foundation of any system is the interconnect logic that connects hardware blocks or components. Creating interconnect logic is time consuming and prone to errors, and existing interconnect logic is difficult to modify when design requirements change. The Platform Designer system integration tool addresses these issues and provides an automatically generated and optimized interconnect designed to satisfy the system requirements.

Platform Designer supports Avalon, AMBA 3 AXI (version 1.0), AMBA 4 AXI (version 2.0), AMBA 4 AXI-Lite (version 2.0), AMBA 4 AXI-Stream (version 1.0), and AMBA 3 APB (version 1.0) interface specifications.

Note: Recommended Intel practices may improve clock frequency, throughput, logic utilization, or power consumption of a Platform Designer design. When you design a Platform Designer system, use your knowledge of the design intent and goals to further optimize system performance beyond the automated optimization available in Platform Designer.

Related Information
- Creating a System with Platform Designer on page 10
- Creating Platform Designer Components on page 90
- Platform Designer Interconnect on page 143
- Avalon Interface Specifications
- AMBA Protocol Specifications

4.1. Designing with Avalon and AXI Interfaces

Platform Designer Avalon and AXI interconnect for memory-mapped interfaces is flexible, partial crossbar logic that connects master and slave interfaces.

Avalon Streaming links connect point-to-point, unidirectional interfaces and are typically used in data stream applications. Each pair of components is connected without any requirement to arbitrate between the data source and sink.

Because Platform Designer supports multiplexed memory-mapped and streaming connections, you can implement systems that use multiplexed logic for control and streaming for data in a single design.
4.1.1. Designing Streaming Components

When you design streaming component interfaces, you must consider integration and communication for each component in the system. One common consideration is buffering data internally to accommodate latency between components.

For example, if the component's Avalon streaming output or source of streaming data is back-pressured because the ready signal is deasserted, then the component must back-pressure its input or sink interface to avoid overflow.

You can use a FIFO to back-pressure internally on the output side of the component so that the input can accept more data even if the output is back-pressured. Then, you can use the FIFO almost full flag to back-pressure the sink interface or input data when the FIFO has only enough space to satisfy the internal latency. You can drive the data valid signal of the output or source interface with the FIFO not empty flag when that data is available.

4.1.2. Designing Memory-Mapped Components

When designing with memory-mapped components, you can implement any component that contains multiple registers mapped to memory locations, for example, a set of four output registers to support software read back from logic. Components that implement read and write memory-mapped transactions require three main building blocks: an address decoder, a register file, and a read multiplexer.

The decoder enables the appropriate 32-bit or 64-bit register for writes. For reads, the address bits drive the multiplexer selection bits. The read signal registers the data from the multiplexer, adding a pipeline stage so that the component can achieve a higher clock frequency.
This slave component has four write wait states and one read wait state. Alternatively, if you want high throughput, you may set both the read and write wait states to zero, and then specify a read latency of one, because the component also supports pipelined reads.

4.2. Using Hierarchy in Systems

You can use hierarchy to sub-divide a system into smaller subsystems that you can then connect in a top-level Platform Designer system. Additionally, if a design contains one or more identical functional units, the functional unit can be defined as a subsystem and instantiated multiple times within a top-level system.
Hierarchy can simplify verification control of slaves connected to each master in a memory-mapped system. Before you implement subsystems in your design, you should plan the system hierarchical blocks at the top-level, using the following guidelines:

- **Plan shared resources**—Determine the best location for shared resources in the system hierarchy. For example, if two subsystems share resources, add the components that use those resources to a higher-level system for easy access.

- **Plan shared address space between subsystems**—Planning the address space ensures you can set appropriate sizes for bridges between subsystems.

- **Plan how much latency you may need to add to your system**—When you add an Avalon Memory Mapped Pipeline Bridge between subsystems, you may add latency to the overall system. You can reduce the added latency by parameterizing the bridge with zero cycles of latency, and by turning off the pipeline command and response signals.

![Avalon Memory Mapped Pipeline Bridge](image)

**Figure 134. Avalon Memory Mapped Pipeline Bridge**
In this example, two Nios II processor subsystems share resources for message passing. Bridges in each subsystem export the Nios II data master to the top-level system that includes the mutex (mutual exclusion component) and shared memory component (which could be another on-chip RAM, or a controller for an off-chip RAM device).
You can also design systems that process multiple data channels by instantiating the same subsystem for each channel. This approach is easier to maintain than a larger, non-hierarchical system. Additionally, such systems are easier to scale because you can calculate the required resources as a multiple of the subsystem requirements.

4.3. Using Concurrency in Memory-Mapped Systems

Platform Designer interconnect uses parallel hardware in FPGAs, which allows you to design concurrency into your system and process transactions simultaneously.
4.3.1. Implementing Concurrency With Multiple Masters

Implementing concurrency requires multiple masters in a Platform Designer system. Systems that include a processor contain at least two master interfaces because the processors include separate instruction and data masters. You can categorize master components as follows:

- General purpose processors, such as Nios II processors
- DMA (direct memory access) engines
- Communication interfaces, such as PCI Express

Because Platform Designer generates an interconnect with slave-side arbitration, every master interface in a system can issue transfers concurrently, if they are not posting transfers to the same slave. Concurrency is limited by the number of master interfaces sharing any particular slave interface. If a design requires higher data throughput, you can increase the number of master and slave interfaces to increase the number of transfers that occur simultaneously. The example below shows a system with three master interfaces.

**Figure 137. Avalon Multiple Master Parallel Access**

In this Avalon example, the DMA engine operates with Avalon memory mapped read and write masters. The yellow lines represent active simultaneous connections.
Figure 138. AXI Multiple Master Parallel Access

In this example, the DMA engine operates with a single master, because in AXI, the write and read channels on the master are independent and can process transactions simultaneously. There is concurrency between the read and write channels, with the yellow lines representing concurrent datapaths.

4.3.2. Implementing Concurrency With Multiple Slaves

You can create multiple slave interfaces for a particular function to increase concurrency in your design.
In this example, there are two channel processing systems. In the first, four hosts must arbitrate for the single slave interface of the channel processor. In the second, each host drives a dedicated slave interface, allowing all master interfaces to simultaneously access the slave interfaces of the component. Arbitration is not necessary when there is a single host and slave interface.
4.3.3. Implementing Concurrency with DMA Engines

In some systems, you can use DMA engines to increase throughput. You can use a DMA engine to transfer blocks of data between interfaces, which then frees the CPU from doing this task. A DMA engine transfers data between a programmed start and end address without intervention, and the data throughput is dictated by the components connected to the DMA. Factors that affect data throughput include data width and clock frequency.

Figure 140. Single or Dual DMA Channels

In this example, the system can sustain more concurrent read and write operations by including more DMA engines. Accesses to the read and write buffers in the top system are split between two DMA engines, as shown in the Dual DMA Channels at the bottom of the figure.

The DMA engine operates with Avalon memory mapped write and read masters. An AXI DMA typically has only one master, because in AXI, the write and read channels on the master are independent and can process transactions simultaneously.

4.4. Inserting Pipeline Stages to Increase System Frequency

Adding pipeline stages may increase the $f_{\text{MAX}}$ of the design by reducing the combinational logic depth, at the cost of additional latency and logic utilization.

Platform Designer provides the Limit interconnect pipeline stages to option on the Interconnect Requirements tab to automatically add pipeline stages to the Platform Designer interconnect when you generate a system.

The Limit interconnect pipeline stages to parameter in the Interconnect Requirements tab allows you to define the maximum Avalon streaming pipeline stages that Platform Designer can insert during generation. You can specify between 0 to 4 pipeline stages, where 0 means that the interconnect has a combinational datapath. You can specify a unique interconnect pipeline stage value for each subsystem.

For more information, refer to Interconnect Pipelining.
4.5. Using Bridges

You can use bridges to increase system frequency, minimize generated Platform Designer logic, minimize adapter logic, and to structure system topology when you want to control where Platform Designer adds pipelining. You can also use bridges with arbiters when there is concurrency in the system.

An Avalon bridge has an Avalon memory mapped slave interface and an Avalon memory mapped master interface. You can have many components connected to the bridge slave interface, or many components connected to the bridge master interface. You can also have a single component connected to a single bridge slave or master interface.

You can configure the data width of the bridge, which can affect how Platform Designer generates bus sizing logic in the interconnect. Both interfaces support Avalon memory mapped pipelined transfers with variable latency, and can also support configurable burst lengths.

Transfers to the bridge slave interface are propagated to the master interface, which connects to components downstream from the bridge. Bridges can provide more control over interconnect pipelining than the Limit interconnect pipeline stages to option.

Note: You can use Avalon bridges between AXI interfaces, and between Avalon domains. Platform Designer automatically creates interconnect logic between the AXI and Avalon interfaces, so you do not have to explicitly instantiate bridges between these domains. For more discussion about the benefits and disadvantages of shared and separate domains, refer to the Platform Designer Interconnect.

Related Information
- Bridges on page 302
- AMBA 3 APB Protocol Specification Support (version 1.0) on page 226

4.5.1. Using Bridges to Increase System Frequency

In Platform Designer, you can introduce interconnect pipeline stages or pipeline bridges to increase clock frequency in your system. Bridges control the system interconnect topology and allow you to subdivide the interconnect, giving you more control over pipelining and clock crossing functionality.

4.5.1.1. Inserting Pipeline Bridges

You can insert an Avalon memory mapped pipeline bridge to insert registers in the path between the bridges and its master and slaves. If a critical register-to-register delay occurs in the interconnect, a pipeline bridge can help reduce this delay and improve system $f_{MAX}$.

The Avalon memory mapped pipeline bridge component integrates into any Platform Designer system. The pipeline bridge options can increase logic utilization and read latency. The change in topology may also reduce concurrency if multiple masters arbitrate for the bridge. You can use the Avalon memory mapped pipeline bridge to
control topology without adding a pipeline stage. A pipeline bridge that does not add a pipeline stage is optimal in some latency-sensitive applications. For example, a CPU may benefit from minimal latency when accessing memory.

**Figure 141. Avalon Memory Mapped Pipeline Bridge**

![Avalon Memory Mapped Pipeline Bridge Diagram]

4.5.1.1.1. Implementing Command Pipelining (Master-to-Slave)

When multiple masters share a slave device, you can use command pipelining to improve performance.

The arbitration logic for the slave interface must multiplex the *address*, *writedata*, and *burstcount* signals. The multiplexer width increases proportionally with the number of masters connecting to a single slave interface. The increased multiplexer width may become a timing critical path in the system. If a single pipeline bridge does not provide enough pipelining, you can instantiate multiple instances of the bridge in a tree structure to increase the pipelining and further reduce the width of the multiplexer at the slave interface.
4.5.1.1.2. Implementing Response Pipelining (Slave-to-Master)

When masters connect to multiple slaves that support read transfers, you can use slave-to-master pipelining to improve performance.
The interconnect inserts a multiplexer for every read datapath back to the master. As the number of slaves supporting read transfers connecting to the master increases, the width of the read data multiplexer also increases. If the performance increase is insufficient with one bridge, you can use multiple bridges in a tree structure to improve $f_{\text{MAX}}$.

### 4.5.1.2. Using Clock Crossing Bridges

The clock crossing bridge contains a pair of clock crossing FIFOs, which isolate the master and slave interfaces in separate, asynchronous clock domains. Transfers to the slave interface are propagated to the master interface.

When you use a FIFO clock crossing bridge for the clock domain crossing, you add data buffering. Buffering allows pipelined read masters to post multiple reads to the bridge, even if the slaves downstream from the bridge do not support pipelined transfers.

You can also use a clock crossing bridge to place high and low frequency components in separate clock domains. If you limit the fast clock domain to the portion of your design that requires high performance, you may achieve a higher $f_{\text{MAX}}$ for this portion of the design. For example, the majority of processor peripherals in embedded designs do not need to operate at high frequencies, therefore, you do not need to use a high-frequency clock for these components. When you compile a design with the Intel Quartus Prime software, compilation may take more time when the clock frequency requirements are difficult to meet because the Fitter needs more time to place registers to achieve the required $f_{\text{MAX}}$. To reduce the amount of effort that the Fitter uses on low priority and low performance components, you can place these behind a clock crossing bridge operating at a lower frequency, allowing the Fitter to increase the effort placed on the higher priority and higher frequency datapaths.

### 4.5.2. Using Bridges to Minimize Design Logic

Bridges can reduce interconnect logic by reducing the amount of arbitration and multiplexer logic that Platform Designer generates. This reduction occurs because bridges limit the number of concurrent transfers that can occur.

#### 4.5.2.1. Avoiding Speed Optimizations That Increase Logic

You can add an additional pipeline stage with a pipeline bridge between masters and slaves to reduce the amount of combinational logic between registers, which can increase system performance. If you can increase the $f_{\text{MAX}}$ of your design logic, you may be able to turn off the Intel Quartus Prime software optimization settings, such as the **Perform register duplication** setting. Register duplication creates duplicate registers in two or more physical locations in the FPGA to reduce register-to-register delays. You may also want to choose **Speed** for the optimization method, which typically results in higher logic utilization due to logic duplication. By making use of the registers or FIFOs available in the bridges, you can increase the design speed and avoid needless logic duplication or speed optimizations, thereby reducing the logic utilization of the design.
4.5.2.2. Limiting Concurrency

The amount of logic generated for the interconnect often increases as the system becomes larger because Platform Designer creates arbitration logic for every slave interface that is shared by multiple master interfaces. Platform Designer inserts multiplexer logic between master interfaces that connect to multiple slave interfaces if both support read datapaths.

Most embedded processor designs contain components that are either incapable of supporting high data throughput, or do not need to be accessed frequently. These components can contain master or slave interfaces. Because the interconnect supports concurrent accesses, you may want to limit concurrency by inserting bridges into the datapath to limit the amount of arbitration and multiplexer logic generated.

For example, if a system contains three master and three slave interfaces that are interconnected, Platform Designer generates three arbiters and three multiplexers for the read datapath. If these masters do not require a significant amount of simultaneous throughput, you can reduce the resources that your design consumes by connecting the three masters to a pipeline bridge. The bridge controls the three slave interfaces and reduces the interconnect into a bus structure. Platform Designer creates one arbitration block between the bridge and the three masters, and a single read datapath multiplexer between the bridge and three slaves, and prevents concurrency. This implementation is similar to a standard bus architecture.

You should not use this method for high throughput datapaths to ensure that you do not limit overall system performance.
4.5.3. Using Bridges to Minimize Adapter Logic

Platform Designer generates adapter logic for clock crossing, width adaptation, and burst support when there is a mismatch between the clock domains, widths, or bursting capabilities of the master and slave interface pairs.

Platform Designer creates burst adapters when the maximum burst length of the master is greater than the master burst length of the slave. The adapter logic creates extra logic resources, which can be substantial when your system contains master interfaces connected to many components that do not share the same characteristics. By placing bridges in your design, you can reduce the amount of adapter logic that Platform Designer generates.

4.5.3.1. Determining Effective Placement of Bridges

To determine the effective placement of a bridge, you should initially analyze each master in your system to determine if the connected slave devices support different bursting capabilities or operate in a different clock domain. The maximum burstcount of a component is visible as the burstcount signal in the HDL file of the component.
The maximum burst length is \(2^{(\text{width}(\text{burstcount}-1))}\), therefore, if the \text{burstcount} width is four bits, the maximum burst length is eight. If no \text{burstcount} signal is present, the component does not support bursting or has a burst length of 1.

To determine if the system requires a clock crossing adapter between the master and slave interfaces, check the \text{Clock} column for the master and slave interfaces. If the clock is different for the master and slave interfaces, Platform Designer inserts a clock crossing adapter between them. To avoid creating multiple adapters, you can place the components containing slave interfaces behind a bridge so that Platform Designer creates a single adapter. By placing multiple components with the same burst or clock characteristics behind a bridge, you limit concurrency and the number of adapters.

You can also use a bridge to separate AXI and Avalon domains to minimize burst adaptation logic. For example, if there are multiple Avalon slaves that are connected to an AXI master, you can consider inserting a bridge to access the adaptation logic once before the bridge, instead of once per slave. This implementation results in latency, and you would also lose concurrency between reads and writes.

### 4.5.3.2. Changing the Response Buffer Depth

When you use automatic clock-crossing adapters, Platform Designer determines the required depth of FIFO buffering based on the slave properties. If a slave has a high \text{Maximum Pending Reads} parameter, the resulting deep response buffer FIFO that Platform Designer inserts between the master and slave can consume a lot of device resources. To control the response FIFO depth, you can use a clock crossing bridge and manually adjust its FIFO depth to trade off throughput with smaller memory utilization.

For example, if you have masters that cannot saturate the slave, you do not need response buffering. Using a bridge reduces the FIFO memory depth and reduces the \text{Maximum Pending Reads} available from the slave.

### 4.5.4. Considering the Effects of Using Bridges

Before you use pipeline or clock crossing bridges in a design, you should carefully consider their effects. Bridges can have any combination of consequences on your design, which could be positive or negative. Benchmarking your system before and after inserting bridges can help you determine the impact to the design.

#### 4.5.4.1. Increased Latency

Adding a bridge to a design has an effect on the read latency between the master and the slave. Depending on the system requirements and the type of master and slave, this latency increase may not be acceptable in your design.

##### 4.5.4.1.1. Acceptable Latency Increase

For a pipeline bridge, Platform Designer adds a cycle of latency for each pipeline option that is enabled. The buffering in the clock crossing bridge also adds latency. If you use a pipelined or burst master that posts many read transfers, the increase in latency does not impact performance significantly because the latency increase is very small compared to the length of the data transfer.
For example, if you use a pipelined read master such as a DMA controller to read data from a component with a fixed read latency of four clock cycles, but only perform a single word transfer, the overhead is three clock cycles out of the total of four. This is true when there is no additional pipeline latency in the interconnect. The read throughput is only 25%.

**Figure 144. Low-Efficiency Read Transfer**

However, if 100 words of data are transferred without interruptions, the overhead is three cycles out of the total of 103 clock cycles. This corresponds to a read efficiency of approximately 97% when there is no additional pipeline latency in the interconnect. Adding a pipeline bridge to this read path adds two extra clock cycles of latency. The transfer requires 105 cycles to complete, corresponding to an efficiency of approximately 94%. Although the efficiency decreased by 3%, adding the bridge may increase the \( f_{\text{MAX}} \) by 5%. For example, if the clock frequency can be increased, the overall throughput would improve. As the number of words transferred increases, the efficiency increases to nearly 100%, whether or not a pipeline bridge is present.

**Figure 145. High Efficiency Read Transfer**

### 4.5.4.1.2. Unacceptable Latency Increase

Processors are sensitive to high latency read times and typically retrieve data for use in calculations that cannot proceed until the data arrives. Before adding a bridge to the datapath of a processor instruction or data master, determine whether the clock frequency increase justifies the added latency.

A Nios II processor instruction master has a cache memory with a read latency of four cycles, which is eight sequential words of data return for each read. At 100 MHz, the first read takes 40 ns to complete. Each successive word takes 10 ns so that eight reads complete in 110 ns.
Adding a clock crossing bridge allows the memory to operate at 125 MHz. However, this increase in frequency is negated by the increase in latency because if the clock crossing bridge adds six clock cycles of latency at 100 MHz, then the memory continues to operate with a read latency of four clock cycles. Consequently, the first read from memory takes 100 ns, and each successive word takes 10 ns because reads arrive at the frequency of the processor, which is 100 MHz. In total, eight reads complete after 170 ns. Although the memory operates at a higher clock frequency, the frequency at which the master operates limits the throughput.

**4.5.4.2. Limited Concurrency**

Placing a bridge between multiple master and slave interfaces limits the number of concurrent transfers your system can initiate. This limitation is the same when connecting multiple master interfaces to a single slave interface. The slave interface of the bridge is shared by all the masters and, as a result, Platform Designer creates arbitration logic. If the components placed behind a bridge are infrequently accessed, this concurrency limitation may be acceptable.

Bridges can have a negative impact on system performance if you use them inappropriately. For example, if multiple memories are used by several masters, you should not place the memory components behind a bridge. The bridge limits memory performance by preventing concurrent memory accesses. Placing multiple memory components behind a bridge can cause the separate slave interfaces to appear as one large memory to the masters accessing the bridge; all masters must access the same slave interface.
A memory subsystem with one bridge that acts as a single slave interface for the Avalon memory mapped Nios II and DMA masters, which results in a bottleneck architecture. The bridge acts as a bottleneck between the two masters and the memories.

If the $f_{\text{MAX}}$ of your memory interfaces is low and you want to use a pipeline bridge between subsystems, you can place each memory behind its own bridge, which increases the $f_{\text{MAX}}$ of the system without sacrificing concurrency.
4.5.4.3. Address Space Translation

The slave interface of a pipeline or clock crossing bridge has a base address and address span. You can set the base address, or allow Platform Designer to set it automatically. The address of the slave interface is the base offset address of all the components connected to the bridge. The address of components connected to the bridge is the sum of the base offset and the address of that component.

The master interface of the bridge drives only the address bits that represent the offset from the base address of the bridge slave interface. Any time a master accesses a slave through a bridge, both addresses must be added together; otherwise the transfer fails. The Address Map tab displays the addresses of the slaves connected to each master and includes address translations caused by system bridges.
In this example, the Nios II processor connects to a bridge located at base address 0x1000, a slave connects to the bridge master interface at an offset of 0x20, and the processor performs a write transfer to the fourth 32-bit or 64-bit word within the slave. Nios II drives the address 0x102C to interconnect, which is within the address range of the bridge. The bridge master interface drives 0x2C, which is within the address range of the slave, and the transfer completes.

### 4.5.4.4. Address Coherency

To simplify the system design, all masters should access slaves at the same location. In many systems, a processor passes buffer locations to other mastering components, such as a DMA controller. If the processor and DMA controller do not access the slave at the same location, Platform Designer must compensate for the differences.

A Nios II processor and DMA controller access a slave interface located at address 0x20. The processor connects directly to the slave interface. The DMA controller connects to a pipeline bridge located at address 0x1000, which then connects to the slave interface. Because the DMA controller accesses the pipeline bridge first, it must drive 0x1020 to access the first location of the slave interface. Because the processor accesses the slave from a different location, you must maintain two base addresses for the slave device.

To avoid the requirement for two addresses, you can add an additional bridge to the system, set its base address to 0x1000, and then disable all the pipelining options in the second bridge so that the bridge has minimal impact on system timing and...
resource utilization. Because this second bridge has the same base address as the original bridge, the processor and DMA controller access the slave interface with the same address range.

**Figure 152. Address Translation Corrected With Bridge**

4.6. Increasing Transfer Throughput

Increasing the transfer efficiency of the master and slave interfaces in your system increases the throughput of your design. Designs with strict cost or power requirements benefit from increasing the transfer efficiency because you can then use less expensive, lower frequency devices. Designs requiring high performance also benefit from increased transfer efficiency because increased efficiency improves the performance of frequency–limited hardware.

Throughput is the number of symbols (such as bytes) of data that Platform Designer can transfer in a given clock cycle. Read latency is the number of clock cycles between the address and data phase of a transaction. For example, a read latency of two means that the data is valid two cycles after the address is posted. If the master must wait for one request to finish before the next begins, such as with a processor, then the read latency is very important to the overall throughput.

You can measure throughput and latency in simulation by observing the waveforms, or using the verification IP monitors.

**Related Information**

- Avalon Verification IP Suite User Guide
4.6.1. Using Pipelined Transfers

Pipelined transfers increase the read efficiency by allowing a master to post multiple reads before data from an earlier read returns. Masters that support pipelined transfers post transfers continuously, relying on the readdatavalid signal to indicate valid data. Slaves support pipelined transfers by including the readdatavalid signal or operating with a fixed read latency.

AXI masters declare how many outstanding writes and reads it can issue with the writeIssuingCapability and readIssuingCapability parameters. In the same way, a slave can declare how many reads it can accept with the readAcceptanceCapability parameter. AXI masters with a read issuing capability greater than one are pipelined in the same way as Avalon masters and the readdatavalid signal.

4.6.1.1. Using the Maximum Pending Reads Parameter

If you create a custom component with a slave interface supporting variable-latency reads, you must specify the Maximum Pending Reads parameter in the Component Editor. Platform Designer uses this parameter to generate the appropriate interconnect and represent the maximum number of read transfers that your pipelined slave component can process. If the number of reads presented to the slave interface exceeds the Maximum Pending Reads parameter, then the slave interface must assert waitrequest.

Optimizing the value of the Maximum Pending Reads parameter requires an understanding of the latencies of your custom components. This parameter should be based on the component’s highest read latency for the various logic paths inside the component. For example, if your pipelined component has two modes, one requiring two clock cycles and the other five, set the Maximum Pending Reads parameter to 5 to allow your component to pipeline five transfers, and eliminating dead cycles after the initial five-cycle latency.

You can also determine the correct value for the Maximum Pending Reads parameter by monitoring the number of reads that are pending during system simulation or while running the hardware. To use this method, set the parameter to a high value and use a master that issues read requests on every clock. You can use a DMA for this task if the data is written to a location that does not frequently assert waitrequest. If you implement this method, you can observe your component with a logic analyzer or built-in monitoring hardware.

Choosing the correct value for the Maximum Pending Reads parameter of your custom pipelined read component is important. If you underestimate the parameter value, you may cause a master interface to stall with a waitrequest until the slave responds to an earlier read request and frees a FIFO position.

The Maximum Pending Reads parameter controls the depth of the response FIFO inserted into the interconnect for each master connected to the slave. This FIFO does not use significant hardware resources. Overestimating the Maximum Pending Reads parameter results in a slight increase in hardware utilization. For these reasons, if you are not sure of the optimal value, you should overestimate this value.

If your system includes a bridge, you must set the Maximum Pending Reads parameter on the bridge as well. To allow maximum throughput, this value should be equal to or greater than the Maximum Pending Reads value for the connected slave that has the highest value. You can limit the maximum pending reads of a slave and...
reduce the buffer depth by reducing the parameter value on the bridge if the high throughput is not required. If you do not know the **Maximum Pending Reads** value for all the slave components, you can monitor the number of reads that are pending during system simulation while running the hardware. To use this method, set the **Maximum Pending Reads** parameter to a high value and use a master that issues read requests on every clock, such as a DMA. Then, reduce the number of maximum pending reads of the bridge until the bridge reduces the performance of any masters accessing the bridge.

### 4.6.2. Arbitration Shares and Bursts

Arbitration shares provide control over the arbitration process. By default, the arbitration algorithm allocates evenly, with all masters receiving one share.

You can adjust the arbitration process by assigning a larger number of shares to masters that need greater throughput. The larger the arbitration share, the more transfers are allocated to the master to access a slave. The masters get uninterrupted access to the slave for its number of shares when the master is reading or writing.

If a master cannot post a transfer, and other masters are waiting to gain access to a particular slave, the arbiter grants access to another master. This mechanism prevents a master from wasting arbitration cycles if it cannot post back-to-back transfers. A bursting transaction contains multiple beats (or words) of data, starting from a single address. Bursts allow a master to maintain access to a slave for more than a single word transfer. If a bursting master posts a write transfer with a burst length of eight, it is guaranteed arbitration for eight write cycles.

You can assign arbitration shares to an Avalon memory mapped bursting master and AXI masters (which are always considered a bursting master). Each share consists of one burst transaction (such as multi cycle write), and allows a master to complete a number of bursts before arbitration switches to the next master.

**Related Information**

Arbitration on page 155

### 4.6.2.1. Differences Between Arbitration Shares and Bursts

The following three key characteristics distinguish arbitration shares and bursts:

- **Arbitration Lock**
- **Sequential Addressing**
- **Burst Adapters**

**Arbitration Lock**

When a master posts a burst transfer, the arbitration is locked for that master; consequently, the bursting master should be capable of sustaining transfers for the duration of the locked period. If, after the fourth write, the master deasserts the write signal (Avalon memory mapped write or AXI \texttt{wvalid}) for fifty cycles, all other masters continue to wait for access during this stalled period.

To avoid wasted bandwidth, your master designs should wait until a full burst transfer is ready before requesting access to a slave device. Alternatively, you can avoid wasted bandwidth by posting \texttt{burstcounts} equal to the amount of data that is ready.
For example, if you create a custom bursting write master with a maximum
burstcount of eight, but only three words of data are ready, you can present a
burstcount of three. This strategy does not result in optimal use of the system band
width if the slave is capable of handling a larger burst; however, this strategy prevents
stalling and allows access for other masters in the system.

**Sequential Addressing**

An Avalon memory mapped burst transfer includes a base address and a
burstcount, which represents the number of words of data that are transferred,
starting from the base address and incrementing sequentially. Burst transfers are
common for processors, DMAs, and buffer processing accelerators; however,
sometimes a master must access non-sequential addresses. Consequently, a bursting
master must set the burstcount to the number of sequential addresses, and then
reset the burstcount for the next location.

The arbitration share algorithm has no restrictions on addresses; therefore, your
custom master can update the address it presents to the interconnect for every read
or write transaction.

**Burst Adapters**

Platform Designer allows you to create systems that mix bursting and non-bursting
master and slave interfaces. This design strategy allows you to connect bursting
master and slave interfaces that support different maximum burst lengths, with
Platform Designer generating burst adapters when appropriate.

Platform Designer inserts a burst adapter whenever a master interface burst length
exceeds the burst length of the slave interface, or if the master issues a burst type
that the slave cannot support. For example, if you connect an AXI master to an Avalon
slave, a burst adapter is inserted. Platform Designer assigns non-bursting masters and
slave interfaces a burst length of one. The burst adapter divides long bursts into
shorter bursts. As a result, the burst adapter adds logic to the address and
burstcount paths between the master and slave interfaces.

**4.6.2.2. Choosing Avalon Memory Mapped Interface Types**

To avoid inefficient Avalon memory mapped transfers, custom master or slave
interfaces must use the appropriate simple, pipelined, or burst interfaces.

**4.6.2.2.1. Simple Avalon Memory Mapped Interfaces**

Simple interface transfers do not support pipelining or bursting for reads or writes;
consequently, their performance is limited. Simple interfaces are appropriate for
transfers between masters and infrequently used slave interfaces. In Platform
Designer, the PIO, UART, and Timer include slave interfaces that use simple transfers.

**4.6.2.2.2. Pipelined Avalon Memory Mapped Interfaces**

Pipelined read transfers allow a pipelined master interface to start multiple read
transfers in succession without waiting for prior transfers to complete. Pipelined
transfers allow master-slave pairs to achieve higher throughput, even though the
slave port may require one or more cycles of latency to return data for each transfer.
In many systems, read throughput becomes inadequate if simple reads are used and pipelined transfers can increase throughput. If you define a component with a fixed read latency, Platform Designer automatically provides the pipelining logic necessary to support pipelined reads. You can use fixed latency pipelining as the default design starting point for slave interfaces. If your slave interface has a variable latency response time, use the \texttt{readdatavalid} signal to indicate when valid data is available. The interconnect implements read response FIFO buffering to handle the maximum number of pending read requests.

To use components that support pipelined read transfers, and to use a pipelined system interconnect efficiently, your system must contain pipelined masters. You can use pipelined masters as the default starting point for new master components. Use the \texttt{readdatavalid} signal for these master interfaces.

Because master and slaves sometimes have mismatched pipeline latency, the interconnect contains logic to reconcile the differences.

<table>
<thead>
<tr>
<th>Table 108. Pipeline Latency in a Master-Slave Pair</th>
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<tbody>
<tr>
<td>Master</td>
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<td>No pipeline</td>
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4.6.2.2.3. Burst Avalon MemoryMapped Interfaces

Burst transfers are commonly used for latent memories such as SDRAM and off-chip communication interfaces, such as PCI Express. To use a burst-capable slave interface efficiently, you must connect to a bursting master. Components that require bursting to operate efficiently typically have an overhead penalty associated with short bursts or non-bursting transfers.

You can use a burst-capable slave interface if you know that your component requires sequential transfers to operate efficiently. Because SDRAM memories incur a penalty when switching banks or rows, performance improves when SDRAM memories are accessed sequentially with bursts.

Architectures that use the same signals to transfer address and data also benefit from bursting. Whenever an address is transferred over shared address and data signals, the throughput of the data transfer is reduced. Because the address phase adds overhead, using large bursts increases the throughput of the connection.
4.6.2.3. Avalon Memory Mapped Burst Master Example

**Figure 153. Avalon Bursting Write Master**

This example shows the architecture of a bursting write master that receives data from a FIFO and writes the contents to memory. You can use a bursting master as a starting point for your own bursting components, such as custom DMAs, hardware accelerators, or off-chip communication interfaces.

The master performs word accesses and writes to sequential memory locations. When go is asserted, the start_address and transfer_length are registered. On the next clock cycle, the control logic asserts burst_begin, which synchronizes the internal control signals in addition to the master_address and master_burstcount presented to the interconnect. The timing of these two signals is important because during bursting write transfers byteenable and burstcount must be held constant for the entire burst.

To avoid inefficient writes, the master posts a burst when enough data is buffered in the FIFO. To maximize the burst efficiency, the master should stall only when a slave asserts waitrequest. In this example, the FIFO's used signal tracks the number of words of data that are stored in the FIFO and determines when enough data has been buffered.

The address register increments after every word transfer, and the length register decrements after every word transfer. The address remains constant throughout the burst. Because a transfer is not guaranteed to complete on burst boundaries, additional logic is necessary to recognize the completion of short bursts and complete the transfer.
4.7. Reducing Logic Utilization

You can minimize logic size of Platform Designer systems. Typically, there is a trade-off between logic utilization and performance. Reducing logic utilization applies to both Avalon and AXI interfaces.

4.7.1. Minimizing Interconnect Logic to Reduce Logic Unitization

In Platform Designer, changes to the connections between master and slave reduce the amount of interconnect logic required in the system.

4.7.1.1. Creating Dedicated Master and Slave Connections to Minimize Interconnect Logic

You can create a system where a master interface connects to a single slave interface. This configuration eliminates address decoding, arbitration, and return data multiplexing, which simplifies the interconnect. Dedicated master-to-slave connections attain the same clock frequencies as Avalon streaming connections.

Typically, these one-to-one connections include an Avalon memory-mapped bridge or hardware accelerator. For example, if you insert a pipeline bridge between a slave and all other master interfaces, the logic between the bridge master and slave interface is reduced to wires. If a hardware accelerator connects only to a dedicated memory, no system interconnect logic is generated between the master and slave pair.

4.7.1.2. Removing Unnecessary Connections to Minimize Interconnect Logic

The number of connections between master and slave interfaces affects the $f_{\text{MAX}}$ of your system. Every master interface that you connect to a slave interface increases the width of the multiplexer width. As a multiplexer width increases, so does the logic depth and width that implements the multiplexer in the FPGA. To improve system performance, connect masters and slaves only when necessary.

When you connect a master interface to many slave interfaces, the multiplexer for the read data signal grows. Avalon typically uses a readdata signal. AXI read data signals add a response status and last indicator to the read response channel using rdata, rresp, and rlast. Additionally, bridges help control the depth of multiplexers.

4.7.1.3. Simplifying Address Decode Logic

If address code logic is in the critical path, you may be able to change the address map to simplify the decode logic. Experiment with different address maps, including a one-hot encoding, to see if results improve.
4.7.2. Minimizing Arbitration Logic by Consolidating Multiple Interfaces

As the number of components in a design increases, the amount of logic required to implement the interconnect also increases. The number of arbitration blocks increases for every slave interface that is shared by multiple master interfaces. The width of the read data multiplexer increases as the number of slave interfaces supporting read transfers increases on a per master interface basis. For these reasons, consider implementing multiple blocks of logic as a single interface to reduce interconnect logic utilization.

4.7.2.1. Logic Consolidation Trade-Offs

You should consider the following trade-offs before making modifications to your system or interfaces:

- Consider the impact on concurrency that results when you consolidate components. When a system has four master components and four slave interfaces, it can initiate four concurrent accesses. If you consolidate the four slave interfaces into a single interface, then the four masters must compete for access. Consequently, you should only combine low priority interfaces such as low speed parallel I/O devices if the combination does not impact the performance.

- Determine whether consolidation introduces new decode and multiplexing logic for the slave interface that the interconnect previously included. If an interface contains multiple read and write address locations, the interface already contains the necessary decode and multiplexing logic. When you consolidate interfaces, you typically reuse the decoder and multiplexer blocks already present in one of the original interfaces; however, combining interfaces may simply move the decode and multiplexer logic, rather than eliminate duplication.

- Consider whether consolidating interfaces makes the design complicated. If so, you should not consolidate interfaces.

Related Information
Using Concurrency in Memory-Mapped Systems on page 260

4.7.2.2. Consolidating Interfaces

The following example shows a system with a mix of components, each having different burst capabilities: a Nios II/e core, a Nios II/f core, and an external processor, which off-loads some processing tasks to the Nios II/f core.

The Nios II/f core supports a maximum burst size of eight. The external processor interface supports a maximum burst length of 64. The Nios II/e core does not support bursting. The memory in the system is SDRAM with an Avalon maximum burst length of two.
Platform Designer automatically inserts burst adapters to compensate for burst length mismatches. The adapters reduce bursts to a single transfer, or the length of two transfers. For the external processor interface connecting to DDR SDRAM, a burst of 64 words is divided into 32 burst transfers, each with a burst length of two. When you generate a system, Platform Designer inserts burst adapters based on maximum burstcount values; consequently, the interconnect logic includes burst adapters between masters and slave pairs that do not require bursting, if the master is capable of bursts.

In this example, Platform Designer inserts a burst adapter between the Nios II processors and the timer, system ID, and PIO peripherals. These components do not support bursting and the Nios II processor performs a single word read and write accesses to these components.
To reduce the number of adapters, you can add pipeline bridges. The pipeline bridge, between the Nios II/f core and the peripherals that do not support bursts, eliminates three burst adapters from the previous example. A second pipeline bridge between the Nios II/f core and the DDR SDRAM, with its maximum burst size set to eight, eliminates another burst adapter, as shown below.

**4.7.3. Reducing Logic Utilization With Multiple Clock Domains**

You specify clock domains in Platform Designer on the **System View** tab. Clock sources can be driven by external input signals to Platform Designer, or by PLLs inside Platform Designer. Clock domains are differentiated based on the name of the clock. You can create multiple asynchronous clocks with the same frequency.

Platform Designer generates Clock Domain Crossing (CDC) logic that hides the details of interfacing components operating in different clock domains. The interconnect supports the memory-mapped protocol with each port independently, and therefore
masters do not need to incorporate clock adapters in order to interface to slaves on a different domain. Platform Designer interconnect logic propagates transfers across clock domain boundaries automatically.

Clock-domain adapters provide the following benefits:

- Allows component interfaces to operate at different clock frequencies.
- Eliminates the need to design CDC hardware.
- Allows each memory-mapped port to operate in only one clock domain, which reduces design complexity of components.
- Enables masters to access any slave without communication with the slave clock domain.
- Allows you to focus performance optimization efforts on components that require fast clock speed.

A clock domain adapter consists of two finite state machines (FSM), one in each clock domain, that use a hand-shaking protocol to propagate transfer control signals (read_request, write_request, and the master waitrequest signals) across the clock boundary.

**Figure 156. Clock Crossing Adapter**

This example illustrates a clock domain adapter between one master and one slave. The synchronizer blocks use multiple stages of flipflops to eliminate the propagation of meta-stable events on the control signals that enter the handshake FSMs. The CDC logic works with any clock ratio.
The typical sequence of events for a transfer across the CDC logic is as follows:

- The master asserts address, data, and control signals.
- The master handshake FSM captures the control signals and immediately forces the master to wait. The FSM uses only the control signals, not address and data. For example, the master simply holds the address signal constant until the slave side has safely captured it.
- The master handshake FSM initiates a transfer request to the slave handshake FSM.
- The transfer request is synchronized to the slave clock domain.
- The slave handshake FSM processes the request, performing the requested transfer with the slave.
- When the slave transfer completes, the slave handshake FSM sends an acknowledge back to the master handshake FSM. The acknowledge is synchronized back to the master clock domain.
- The master handshake FSM completes the transaction by releasing the master from the wait condition.

Transfers proceed as normal on the slave and the master side, without a special protocol to handle crossing clock domains. From the perspective of a slave, there is nothing different about a transfer initiated by a master in a different clock domain. From the perspective of a master, a transfer across clock domains simply requires extra clock cycles. Similar to other transfer delay cases (for example, arbitration delay or wait states on the slave side), the Platform Designer forces the master to wait until the transfer terminates. As a result, pipeline master ports do not benefit from pipelining when performing transfers to a different clock domain.

Platform Designer automatically determines where to insert CDC logic based on the system and the connections between components, and places CDC logic to maintain the highest transfer rate for all components. Platform Designer evaluates the need for CDC logic for each master and slave pair independently, and generates CDC logic wherever necessary.

**Related Information**

Avalon Memory-Mapped Design Optimizations

### 4.7.4. Duration of Transfers Crossing Clock Domains

CDC logic extends the duration of master transfers across clock domain boundaries. In the worst case, which is for reads, each transfer is extended by five master clock cycles and five slave clock cycles. Assuming the default value of 2 for the master domain synchronizer length and the slave domain synchronizer length, the components of this delay are the following:

- Four additional master clock cycles, due to the master-side clock synchronizer.
- Four additional slave clock cycles, due to the slave-side clock synchronizer.
- One additional clock in each direction, due to potential metastable events as the control signals cross clock domains.
Note: Systems that require a higher performance clock should use the Avalon memory mapped clock crossing bridge instead of the automatically inserted CDC logic. The clock crossing bridge includes a buffering mechanism so that multiple reads and writes can be pipelined. After paying the initial penalty for the first read or write, there is no additional latency penalty for pending reads and writes, increasing throughput by up to four times, at the expense of added logic resources.

4.8. Reducing Power Consumption

Platform Designer provides various low power design changes that enable you to reduce the power consumption of the interconnect and custom components.

4.8.1. Reducing Power Consumption With Multiple Clock Domains

When you use multiple clock domains, you should put non-critical logic in the slower clock domain. Platform Designer automatically reconciles data crossing over asynchronous clock domains by inserting clock crossing logic (handshake or FIFO).

You can use clock crossing in Platform Designer to reduce the clock frequency of the logic that does not require a high frequency clock, which allows you to reduce power consumption. You can use either handshaking clock crossing bridges or handshaking clock crossing adapters to separate clock domains.

You can use the clock crossing bridge to connect master interfaces operating at a higher frequency to slave interfaces running at a lower frequency. Only connect low throughput or low priority components to a clock crossing bridge that operates at a reduced clock frequency. The following are examples of low throughput or low priority components:

- PIOs
- UARTs (JTAG or RS-232)
- System identification (SysID)
- Timers
- PLL (instantiated within Platform Designer)
- Serial peripheral interface (SPI)
- EPCS controller
- Tristate bridge and the components connected to the bridge

By reducing the clock frequency of the components connected to the bridge, you reduce the dynamic power consumption of the design. Dynamic power is a function of toggle rates and decreasing the clock frequency decreases the toggle rate.
Figure 157. Reducing Power Utilization Using a Bridge to Separate Clock Domains
Platform Designer automatically inserts clock crossing adapters between master and slave interfaces that operate at different clock frequencies. You can choose the type of clock crossing adapter in the Platform Designer **Project Settings** tab. Adapters do not appear in the **Connections** column because you do not insert them. The following clock crossing adapter types are available in Platform Designer:

- **Handshake**—Uses a simple handshaking protocol to propagate transfer control signals and responses across the clock boundary. This adapter uses fewer hardware resources because each transfer is safely propagated to the target domain before the next transfer begins. The Handshake adapter is appropriate for systems with low throughput requirements.

- **FIFO**—Uses dual-clock FIFOs for synchronization. The latency of the FIFO adapter is approximately two clock cycles more than the handshake clock crossing component, but the FIFO-based adapter can sustain higher throughput because it supports multiple transactions simultaneously. The FIFO adapter requires more resources, and is appropriate for memory-mapped transfers requiring high throughput across clock domains.

- **Auto**—Platform Designer specifies the appropriate FIFO adapter for bursting links and the Handshake adapter for all other links.

Because the clock crossing bridge uses FIFOs to implement the clock crossing logic, it buffers transfers and data. Clock crossing adapters are not pipelined, so that each transaction is blocking until the transaction completes. Blocking transactions may lower the throughput substantially; consequently, if you want to reduce power consumption without limiting the throughput significantly, you should use the clock crossing bridge or the FIFO clock crossing adapter. However, if the design requires single read transfers, a clock crossing adapter is preferable because the latency is lower.

The clock crossing bridge requires few logic resources other than on-chip memory. The number of on-chip memory blocks used is proportional to the address span, data width, buffering depth, and bursting capabilities of the bridge. The clock crossing adapter does not use on-chip memory and requires a moderate number of logic resources. The address span, data width, and the bursting capabilities of the clock crossing adapter determine the resource utilization of the device.

When you decide to use a clock crossing bridge or clock crossing adapter, you must consider the effects of throughput and memory utilization in the design. If on-chip memory resources are limited, you may be forced to choose the clock crossing adapter. Using the clock crossing bridge to reduce the power of a single component may not justify using more resources. However, if you can place all of the low priority components behind a single clock crossing bridge, you may reduce power consumption in the design.

**Related Information**

Power Optimization
4.8.2. Reducing Power Consumption by Minimizing Toggle Rates

A Platform Designer system consumes power whenever logic transitions between on and off states. When the state is held constant between clock edges, no charging or discharging occurs. You can use the following design methodologies to reduce the toggle rates of your design:

- Registering component boundaries
- Using clock enable signals
- Inserting bridges

Platform Designer interconnect is uniquely combinational when no adapters or bridges are present and there is no interconnect pipelining. When a slave interface is not selected by a master, various signals may toggle and propagate into the component. By registering the boundary of your component at the master or slave interface, you can minimize the toggling of the interconnect and your component. In addition, registering boundaries can improve operating frequency. When you register the signals at the interface level, you must ensure that the component continues to operate within the interface standard specification.

Avalon memory mapped **waitrequest** is a difficult signal to synchronize when you add registers to your component. The **waitrequest** signal must be asserted during the same clock cycle that a master asserts read or write to in order to prolong the transfer. A master interface can read the **waitrequest** signal too early and post more reads and writes prematurely.

**Note:** There is no direct AXI equivalent for **waitrequest** and **burstcount**, though the AMBA Protocol Specification implies that the AXI **ready** signal cannot depend combinatorially on the AXI **valid** signal. Therefore, Platform Designer typically buffers AXI component boundaries for the **ready** signal.

For slave interfaces, the interconnect manages the **begintransfer** signal, which is asserted during the first clock cycle of any read or write transfer. If the **waitrequest** is one clock cycle late, you can logically OR the **waitrequest** and the **begintransfer** signals to form a new **waitrequest** signal that is properly synchronized. Alternatively, the component can assert **waitrequest** before it is selected, guaranteeing that the **waitrequest** is already asserted during the first clock cycle of a transfer.
Using Clock Enables

You can use clock enables to hold the logic in a steady state, and the write and read signals as clock enables for slave components. Even if you add registers to your component boundaries, the interface can potentially toggle without the use of clock enables. You can also use the clock enable to disable combinational portions of the component.

For example, you can use an active high clock enable to mask the inputs into the combinational logic to prevent it from toggling when the component is inactive. Before preventing inactive logic from toggling, you must determine if the masking causes the circuit to function differently. If masking causes a functional failure, it may be possible to use a register stage to hold the combinational logic constant between clock cycles.

Inserting Bridges

You can use bridges to reduce toggle rates, if you do not want to modify the component by using boundary registers or clock enables. A bridge acts as a repeater where transfers to the slave interface are repeated on the master interface. If the bridge is not accessed, the components connected to its master interface are also not accessed. The master interface of the bridge remains idle until a master accesses the bridge slave interface.

Bridges can also reduce the toggle rates of signals that are inputs to other master interfaces. These signals are typically readdata, readdatavalid, and waitrequest. Slave interfaces that support read accesses drive the readdata, readdatavalid, and waitrequest signals. A bridge inserts either a register or clock crossing FIFO between the slave interface and the master to reduce the toggle rate of the master input signals.

4.8.3. Reducing Power Consumption by Disabling Logic

There are typically two types of low power modes: volatile and non-volatile. A volatile low power mode holds the component in a reset state. When the logic is reactivated, the previous operational state is lost. A non-volatile low power mode restores the previous operational state. You can use either software-controlled or hardware-controlled sleep modes to disable a component in order to reduce power consumption.
Software-Controlled Sleep Mode

To design a component that supports software-controlled sleep mode, create a single memory-mapped location that enables and disables logic by writing a zero or one. You can use the register’s output as a clock enable or reset, depending on whether the component has non-volatile requirements. The slave interface must remain active during sleep mode so that the enable bit is set when the component needs to be activated.

If multiple masters can access a component that supports sleep mode, you can use the Mutex Intel FPGA IP to provide mutually exclusive accesses to your component. You can also build in the logic to re-enable the component on the very first access by any master in your system. If the component requires multiple clock cycles to re-activate, then it must assert a wait request to prolong the transfer as it exits sleep mode.

Hardware-Controlled Sleep Mode

Alternatively, you can implement a timer in your component that automatically causes the component to enter a sleep mode based on a timeout value specified in clock cycles between read or write accesses. Each access resets the timer to the timeout value. Each cycle with no accesses decrements the timeout value by one. If the counter reaches zero, the hardware enters sleep mode until the next access.

Figure 159. Hardware-Controlled Sleep Components

This example provides a schematic for the hardware-controlled sleep mode. If restoring the component to an active state takes a long time, use a long timeout value so that the component is not continuously entering and exiting sleep mode. The slave interface must remain functional while the rest of the component is in sleep mode. When the component exits sleep mode, the component must assert the waitrequest signal until it is ready for read or write accesses.

Related Information
Mutex Core

4.9. Reset Polarity and Synchronization in Platform Designer

When you add a component interface with a reset signal, Platform Designer defines its polarity as reset(active-high) or reset_n (active-low).
You can view the polarity status of a reset signal by selecting the signal in the Hierarchy tab, and then view its expanded definition in the open Parameters and Block Symbol tabs. When you generate your component, Platform Designer interconnect automatically inverts polarities as needed.

**Figure 160. Reset Signal (Active-High)**

**Figure 161. Reset Signal Active-Low**
Each Platform Designer component has its own requirements for reset synchronization. Some blocks have internal synchronization and have no requirements, whereas other blocks require an externally synchronized reset. You can define how resets are synchronized in your Platform Designer system with the **Synchronous edges** parameter. In the clock source or reset bridge component, set the value of the **Synchronous edges** parameter to one of the following, depending on how the reset is externally synchronized:

- **None**—There is no synchronization on this reset.
- **Both**—The reset is synchronously asserted and deasserted with respect to the input clock.
- **Deassert**—The reset is synchronously asserted with respect to the input clock, and asynchronously deasserted.

**Figure 162. Synchronous Edges Parameter**

You can combine multiple reset sources to reset a particular component.
When you generate your component, Platform Designer inserts adapters to synchronize or invert resets if there are mismatches in polarity or synchronization between the source and destination. You can view inserted adapters on the Memory-Mapped Interconnect tab with the System ➤ Show System with Platform Designer Interconnect command.

Figure 164. Platform Designer Interconnect
4.10. Optimizing Platform Designer System Performance Design Examples

- Avalon Pipelined Read Master Example on page 298
- Multiplexer Examples on page 300

4.10.1. Avalon Pipelined Read Master Example

For a high throughput system using the Avalon memory mapped standard, you can design a pipelined read master that allows a system to issue multiple read requests before data returns. Pipelined read masters hide the latency of read operations by posting reads as frequently as every clock cycle. You can use this type of master when the address logic is not dependent on the data returning.

4.10.1.1. Avalon Pipelined Read Master Example Design Requirements

You must carefully design the logic for the control and datapaths of pipelined read masters. The control logic must extend a read cycle whenever the waitrequest signal is asserted. This logic must also control the master address, byteenable, and read signals. To achieve maximum throughput, pipelined read masters should post reads continuously while waitrequest is deasserted. While read is asserted, the address presented to the interconnect is stored.

The datapath logic includes the readdata and readdatavalid signals. If your master can accept data on every clock cycle, you can register the data with the readdatavalid as an enable bit. If your master cannot process a continuous stream of read data, it must buffer the data in a FIFO. The control logic must stop issuing reads when the FIFO reaches a predetermined fill level to prevent FIFO overflow.

4.10.1.2. Expected Throughput Improvement

The throughput improvement that you can achieve with a pipelined read master is typically directly proportional to the pipeline depth of the interconnect and the slave interface. For example, if the total latency is two cycles, you can double the throughput by inserting a pipelined read master, assuming the slave interface also supports pipeline transfers. If either the master or slave does not support pipelined read transfers, then the interconnect asserts waitrequest until the transfer completes. You can also gain throughput when there are some cycles of overhead before a read response.

Where reads are not pipelined, the throughput is reduced. When both the master and slave interfaces support pipelined read transfers, data flows in a continuous stream after the initial latency. You can use a pipelined read master that stores data in a FIFO to implement a custom DMA, hardware accelerator, or off-chip communication interface.
This example shows a pipelined read master that stores data in a FIFO. The master performs word accesses that are word-aligned and reads from sequential memory addresses. The transfer length is a multiple of the word size.

When the go bit is asserted, the master registers the start_address and transfer_length signals. The master begins issuing reads continuously on the next clock cycle until the length register reaches zero. In this example, the word size is four bytes so that the address always increments by four, and the length decrements by four. The read signal remains asserted unless the FIFO fills to a predetermined level. The address register increments and the length register decrements if the length has not reached 0 and a read is posted.

The master posts a read transfer every time the read signal is asserted and the waitrequest is deasserted. The master issues reads until the entire buffer has been read or waitrequest is asserted. An optional tracking block monitors the done bit. When the length register reaches zero, some reads are outstanding. The tracking logic prevents assertion of done until the last read completes, and monitors the number of reads posted to the interconnect so that it does not exceed the space remaining in the readdata FIFO. This example includes a counter that verifies that the following conditions are met:

- If a read is posted and readdatavalid is deasserted, the counter increments.
- If a read is not posted and readdatavalid is asserted, the counter decrements.
When the length register and the tracking logic counter reach zero, all the reads have completed and the done bit is asserted. The done bit is important if a second master overwrites the memory locations that the pipelined read master accesses. This bit guarantees that the reads have completed before the original data is overwritten.

4.10.2. Multiplexer Examples

You can combine adapters with streaming components to create datapaths whose input and output streams have different properties. The following examples demonstrate datapaths in which the output stream exhibits higher performance than the input stream.

The diagram below illustrates a datapath that uses the dual clock version of the on-chip FIFO memory to boost the frequency of input data from 100 MHz to 110 MHz by sampling two input streams at differential rates. The on-chip FIFO memory has an input clock frequency of 100 MHz, and an output clock frequency of 110 MHz. The channel multiplexer runs at 110 MHz and samples one input stream 27.3 percent of the time, and the second 72.7 percent of the time. You must know what the typical and maximum input channel utilizations are before for this type of design. For example, if the first channel hits 50% utilization, the output stream exceeds 100% utilization.

Figure 166. Datapath that Doubles the Clock Frequency

The diagram below illustrates a datapath that uses a data format adapter and Avalon streaming channel multiplexer to merge the 8-bit 100 MHz input from two streaming data sources into a single 16-bit 100 MHz streaming output. This example shows an output with double the throughput of each interface with a corresponding doubling of the data width.

Figure 167. Datapath to Double Data Width and Maintain Original Frequency

The diagram below illustrates a datapath that uses the dual clock version of the on-chip FIFO memory and Avalon streaming channel multiplexer to merge the 100 MHz input from two streaming data sources into a single 200 MHz streaming output. This example shows an output with double the throughput of each interface with a corresponding doubling of the clock frequency.
4.11. Optimizing Platform Designer System Performance Revision History

The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2018.12.15</td>
<td>18.1.0</td>
<td>• Replaced references to System Contents tab with new System View tab.</td>
</tr>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>• Changed instances of Qsys Pro to Platform Designer</td>
</tr>
</tbody>
</table>
| 2016.10.31       | 16.1.0                      | • Implemented Intel rebranding.  
                   |                             | • Implemented Qsys rebranding. |
| 2015.11.02       | 15.1.0                      | • Added: Reset Polarity and Synchronization in Qsys.  
                   |                             | • Changed instances of Quartus II to Quartus Prime. |
| 2015.05.04       | 15.0.0                      | * Multiplexer Examples, rearranged description text for the figures. |
| May 2013         | 13.0.0                      | AMBA APB support. |
| November 2012    | 12.1.0                      | AMBA AXI4 support. |
| June 2012        | 12.0.0                      | AMBA AXI3 support. |
| November 2011    | 11.1.0                      | New document release. |
5. Platform Designer System Design Components

You can use Platform Designer IP components to create Platform Designer systems. Platform Designer interfaces include components appropriate for streaming high-speed data, reading and writing registers and memory, controlling off-chip devices, and transporting data between components.

Note: Intel now refers to Qsys Pro as Platform Designer.

Platform Designer supports Avalon, AMBA 3 AXI (version 1.0), AMBA 4 AXI (version 2.0), AMBA 4 AXI-Lite (version 2.0), AMBA 4 AXI-Stream (version 1.0), and AMBA 3 APB (version 1.0) interface specifications.

Related Information
- Creating a System with Platform Designer on page 10
- Platform Designer Interconnect on page 143
- AMBA Protocol Specifications
- Embedded Peripherals IP User Guide
- Avalon Interface Specifications

5.1. Bridges

Bridges affect the way Platform Designer transports data between components. You can insert bridges between master and slave interfaces to control the topology of a Platform Designer system, which affects the interconnect that Platform Designer generates. You can also use bridges to separate components into different clock domains to isolate clock domain crossing logic.

A bridge has one slave interface and one master interface. In Platform Designer, one or more master interfaces from other components connect to the bridge slave. The bridge master connects to one or more slave interfaces on other components.
Figure 169. Using a Bridge in a Platform Designer System

In this example, three masters have logical connections to three slaves, although physically each master connects only to the bridge. Transfers initiated to the slave propagate to the master in the same order in which the transfers are initiated on the slave.

5.1.1. Clock Bridge Intel FPGA IP

The Clock Bridge Intel FPGA IP connects a clock source to multiple clock input interfaces. You can use the clock bridge to connect a clock source that is outside the Platform Designer system. Create the connection through an exported interface, and then connect to multiple clock input interfaces.

Clock outputs match fan-out performance without the use of a bridge. You require a bridge only when you want a clock from an exported source to connect internally to more than one source.
5.1.2. Avalon Memory Mapped Clock Crossing Bridge Intel FPGA IP

The Avalon Memory Mapped Clock Crossing Bridge Intel FPGA IP transfers Avalon-MM commands and responses between different clock domains. You can also use the Avalon Memory Mapped Clock Crossing Bridge between AXI masters and slaves of different clock domains.

The Avalon Memory Mapped Clock Crossing Bridge uses asynchronous FIFOs to implement clock crossing logic. The bridge parameters control the depth of the command and response FIFOs in both the master and slave clock domains. If the number of active reads exceeds the depth of the response FIFO, the Clock Crossing Bridge stops sending reads.

To maintain throughput for high-performance applications, increase the response FIFO depth from the default minimum depth, which is twice the maximum burst size.

Note: When you use the FIFO-based clock crossing a Platform Designer system, the DC FIFO is automatically inserted in the Platform Designer system. The reset inputs for the DC FIFO connect to the reset sources for the connected master and slave components on either side of the DC FIFO. For this configuration, you must assert both the resets on the master and the slave sides at the same time to ensure the DC FIFO resets properly. Alternatively, you can drive both resets from the same reset source to guarantee that the DC FIFO resets properly.
Note: The clock crossing bridge includes appropriate SDC constraints for its internal asynchronous FIFOs. For these SDC constraints to work correctly, do not set false paths on the pointer crossings in the FIFOs. Do not split the bridge’s clocks into separate clock groups when you declare SDC constraints; the split has the same effect as setting false paths.

5.1.2.1. Avalon Memory Mapped Clock Crossing Bridge Example

In the example shown below, the Avalon Memory Mapped Clock Crossing bridges separate slave components into two groups. The Avalon Memory Mapped Clock Crossing Bridge places the low performance slave components behind a single bridge and clocks the components at a lower speed. The bridge places the high-performance components behind a second bridge and clocks it at a higher speed.

By inserting clock-crossing bridges, you simplify the Platform Designer interconnect and allow the Intel Quartus Prime Fitter to optimize paths that require minimal propagation delay.

Figure 171. Avalon Memory Mapped Clock Crossing Bridge
### 5.1.2.2. Avalon Memory Mapped Clock Crossing Bridge Parameters

Table 109. Avalon Memory Mapped Clock Crossing Bridge Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data width</td>
<td>8, 16, 32, 64, 128, 256, 512, 1024 bits</td>
<td>Determines the data width of the interfaces on the bridge, and affects the size of both FIFOs. For the highest bandwidth, set Data width to be as wide as the widest master that connects to the bridge.</td>
</tr>
<tr>
<td>Symbol width</td>
<td>1, 2, 4, 8, 16, 32, 64 (bits)</td>
<td>Number of bits per symbol. For example, byte-oriented interfaces have 8-bit symbols.</td>
</tr>
<tr>
<td>Address width</td>
<td>1-32 bits</td>
<td>The address bits needed to address the downstream slaves.</td>
</tr>
<tr>
<td>Use automatically-determined address width</td>
<td>-</td>
<td>The minimum bridge address width that is required to address the downstream slaves.</td>
</tr>
<tr>
<td>Maximum burst size</td>
<td>1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024 bits</td>
<td>Determines the maximum length of bursts that the bridge supports.</td>
</tr>
<tr>
<td>Command FIFO depth</td>
<td>2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384 bits</td>
<td>Command (master-to-slave) FIFO depth.</td>
</tr>
<tr>
<td>Respond FIFO depth</td>
<td>2, 4, 8,16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384 bits</td>
<td>Slave-to-master FIFO depth.</td>
</tr>
<tr>
<td>Master clock domain synchronizer depth</td>
<td>2, 3, 4, 5 bits</td>
<td>The number of pipeline stages in the clock crossing logic in the issuing master to target slave direction. Increasing this value leads to a larger mean time between failures (MTBF). You can determine the MTBF for a design by running a timing analysis.</td>
</tr>
<tr>
<td>Slave clock domain synchronizer depth</td>
<td>2, 3, 4, 5 bits</td>
<td>The number of pipeline stages in the clock crossing logic in the target slave to master direction. Increasing this value leads to a larger meantime between failures (MTBF). You can determine the MTBF for a design by running a timing analysis.</td>
</tr>
</tbody>
</table>

### 5.1.3. Avalon Memory Mapped Pipeline Bridge Intel FPGA IP

The Avalon Memory Mapped Pipeline Bridge Intel FPGA IP inserts a register stage in the Avalon memory mapped command and response paths. The bridge accepts commands on its slave port and propagates the commands to its master port. The pipeline bridge provides separate parameters to turn on pipelining for command and response signals.

The **Maximum pending read transactions** parameter is the maximum number of pending reads that the Avalon Memory Mapped bridge can queue up. To determine the best value for this parameter, review this same option for the bridge’s connected slaves and identify the highest value of the parameter, and then add the internal buffering requirements of the Avalon Memory Mapped bridge. In general, the value is between 4 and 32. The limit for maximum queued transactions is 64.

You can use the Avalon Memory Mapped bridge to export a single Avalon memory mapped slave interface to control multiple Avalon memory mapped slave devices. The pipelining feature is optional.
Figure 172. Avalon Memory Mapped Pipeline Bridge IP and XAUI PHY Transceiver IP

In this example, the bridge transfers commands received on its slave interface to its master port.

Because the slave interface is exported to the pins of the device, having a single slave port, rather than separate ports for each slave device, reduces the pin count of the FPGA.

5.1.4. Avalon Memory Mapped Unaligned Burst Expansion Bridge Intel FPGA IP

The Avalon Memory Mapped Unaligned Burst Expansion Bridge Intel FPGA IP aligns read burst transactions from masters connected to its slave interface, to the address space of slaves connected to its master interface. This alignment ensures that all read burst transactions are delivered to the slave as a single transaction.
You can use the Avalon Unaligned Burst Expansion Bridge to align read burst transactions from masters that have narrower data widths than the target slaves. Using the bridge for this purpose improves bandwidth utilization for the master-slave pair, and ensures that unaligned bursts are processed as single transactions rather than multiple transactions.

**Note:** Do not use the Avalon Memory Mapped Unaligned Burst Expansion Bridge if any connected slave has read side effects from reading addresses that are exposed to any connected master's address map. This bridge can cause read side effects due to alignment modification to read burst transaction addresses.

**Note:** The Avalon Memory Mapped Unaligned Burst Expansion Bridge does not support VHDL simulation.

### 5.1.4.1. Using the Avalon Memory Mapped Unaligned Burst Expansion Bridge

When a master sends a read burst transaction to a slave, the Avalon Memory Mapped Unaligned Burst Expansion Bridge initially determines whether the start address of the read burst transaction is aligned to the slave's memory address space. If the base address is aligned, the bridge does not change the base address. If the base address is not aligned, the bridge aligns the base address to the nearest aligned address that is less than the requested base address.

The Avalon Memory Mapped Unaligned Burst Expansion Bridge then determines whether the final word requested by the master is the last word at the slave read burst address. If a single slave address contains multiple words, all those words must be requested for a single read burst transaction to occur.

- If the final word requested by the master is the last word at the slave read burst address, the bridge does not modify the burst length of the read burst command to the slave.
- If the final word requested by the master is not the last word at the slave read burst address, the bridge increases the burst length of the read burst command to the slave. The final word requested by the modified read burst command is then the last word at the slave read burst address.
The bridge stores information about each aligned read burst command that it sends to slaves connected to a master interface. When a read response is received on the master interface, the bridge determines if the base address or burst length of the issued read burst command was altered.

If the bridge alters either the base address or the burst length of the issued read burst command, it receives response words that the master did not request. The bridge suppresses words that it receives from the aligned burst response that are not part of the original read burst command from the master.

5.1.4.2. Avalon Memory Mapped Unaligned Burst Expansion Bridge Parameters

Table 110. Avalon Memory Mapped Unaligned Burst Expansion Bridge Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data width</td>
<td>Data width of the master connected to the bridge.</td>
</tr>
<tr>
<td>Address width (in WORDS)</td>
<td>The address width of the master connected to the bridge.</td>
</tr>
<tr>
<td>Burstcount width</td>
<td>The burstcount signal width of the master connected to the bridge.</td>
</tr>
<tr>
<td>Maximum pending read transactions</td>
<td>The Maximum pending read transactions parameter is the maximum number of pending reads that the Avalon Memory Mapped bridge can queue up. To determine the best value for this parameter, review this same option for the bridge's connected slaves and identify the highest value of the parameter, and then add the internal buffering requirements of the Avalon Memory Mapped bridge. In general, the value is between 4 and 32. The limit for maximum queued transactions is 64.</td>
</tr>
<tr>
<td>Width of slave to optimize for</td>
<td>The data width of the connected slave. Supported values are: 16, 32, 64, 128, 256, 512, 1024, 2048, and 4096 bits. Note: If you connect multiple slaves, all slaves must have the same data width.</td>
</tr>
<tr>
<td>Pipeline command signals</td>
<td>When turned on, the command path is pipelined, minimizing the bridge's critical path at the expense of increased logic usage and latency.</td>
</tr>
</tbody>
</table>
### 5.1.4.3. Avalon Memory Mapped Unaligned Burst Expansion Bridge Example

#### Figure 175. Unaligned Burst Expansion Bridge

The example below shows an unaligned read burst command from a master that the Avalon Memory Mapped Unaligned Burst Expansion Bridge converts to an aligned request for a connected slave, and the suppression of words due to the aligned read burst command. In this example, a 32-bit master requests an 8-beat burst of 32-bit words from a 64-bit slave with a start address that is not 64-bit aligned.

<table>
<thead>
<tr>
<th>Transaction 1</th>
<th>Without Avalon-MM Unaligned Burst Expansion Bridge</th>
<th>With Avalon-MM Unaligned Burst Expansion Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0, 1</td>
<td>0, 1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X*</td>
</tr>
<tr>
<td>2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>4</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>5</td>
<td>A, B</td>
<td>A, B</td>
</tr>
<tr>
<td>6</td>
<td>C, D</td>
<td>C, D</td>
</tr>
<tr>
<td>7</td>
<td>E, F</td>
<td>E, F</td>
</tr>
<tr>
<td>8</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>9</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Because the target slave has a 64-bit data width, address 1 is unaligned in the slave's address space. As a result, several smaller burst transactions are needed to request the data associated with the master's read burst command.

With an Avalon memory mapped Unaligned Burst Expansion Bridge in place, the bridge issues a new read burst command to the target slave beginning at address 0 with burst length 10, which requests data up to the word stored at address 9.

When the bridge receives the word corresponding to address 0, it suppresses it from the master, and then delivers the words corresponding to addresses 1 through 8 to the master. When the bridge receives the word corresponding to address 9, it suppresses that word from the master.

### 5.1.5. Bridges Between Avalon and AXI Interfaces

When designing a Platform Designer system, you can make connections between AXI and Avalon interfaces without the use of explicitly-instantiated bridges; the interconnect provides all necessary bridging logic. However, this does not prevent the use of explicit bridges to separate the AXI and Avalon domains.
Figure 176. Avalon Memory Mapped Pipeline Bridge Between Avalon Memory-Mapped and AXI Domains

Using an explicit Avalon memory mapped bridge to separate the AXI and Avalon domains reduces the amount of bridging logic in the interconnect at the expense of concurrency.

5.1.6. AXI Bridge Intel FPGA IP

With an AXI bridge, you can influence the placement of resource-intensive components, such as the width and burst adapters. Depending on its use, an AXI bridge may reduce throughput and concurrency, in return for higher $f_{\text{MAX}}$ and less logic.

You can use an AXI Bridge Intel FPGA IP to group different parts of your Platform Designer system. Other parts of the system can then connect to the bridge interface instead of to multiple separate master or slave interfaces. You can also use an AXI bridge to export AXI interfaces from Platform Designer systems.

Example 27. Reducing the Number of Adapters by Adding a Bridge

The figure shows a system with a single AXI master and three AXI slaves. It also has various interconnect components, such as routers, demultiplexers, and multiplexers. Two of the slaves have a narrower data width than the master; 16-bit slaves versus a 32-bit master.
Four width adapters (0 - 3) and four burst adapters (0 - 3) are inserted between the master and slaves for transaction adaptation for the example system.

In this system, Platform Designer interconnect creates four width adapters and four burst adapters to access the two slaves.

You can improve resource usage by adding an AXI bridge. Then, Platform Designer needs to add only two width adapters and two burst adapters; one pair for the read channels, and another pair for the write channel.
By inserting an AXI bridge, the interconnect is divided into two domains (interconnect_0 and interconnect_1). Notice the reduction in the number of width adapters from 4 to 2 after the bridge insertion. The same process applies for burst adapters.

Even though this system includes more components, the overall system performance improves because there are fewer resource-intensive width and burst adapters.

5.1.6.1. AXI Bridge Signal Types

Based on parameter selections that you make for the AXI Bridge component, Platform Designer instantiates either the AMBA 3 AXI or AMBA 3 AXI master and slave interfaces into the component.
Note: In AMBA 3 AXI, aw/aruser accommodates sideband signal usage by hard processor systems (HPS).

Table 111. Sets of Signals for the AXI Bridge Based on the Protocol

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>AMBA 3 AXI</th>
<th>AMBA 3 AXI</th>
</tr>
</thead>
<tbody>
<tr>
<td>awid / arid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awaddr / araddr</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awlen / arlen</td>
<td>yes (4-bit)</td>
<td>yes (8-bit)</td>
</tr>
<tr>
<td>awsize / arsize</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awburst / arburst</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awlock / arlock</td>
<td>yes</td>
<td>yes (1-bit optional)</td>
</tr>
<tr>
<td>awcache / arcache</td>
<td>yes (2-bit)</td>
<td>yes (optional)</td>
</tr>
<tr>
<td>awprot / arprot</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awuser / aruser</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awvalid / arvalid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awready / arready</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>awqos / arqos</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>awregion / arregion</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>wid</td>
<td>yes</td>
<td>no (optional)</td>
</tr>
<tr>
<td>wdata / rdata</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wstrb</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wlast / rvalid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wvalid / rvalid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wready / rready</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>wuser / ruser</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>bid / rid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>bresp / rresp</td>
<td>yes</td>
<td>yes (optional)</td>
</tr>
<tr>
<td>bvalid</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>bready</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>

5.1.6.2. AXI Bridge Parameters

In the parameter editor, you can customize the parameters for the AXI bridge according to the requirements of your design.
Table 112. AXI Bridge Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Type</th>
<th>Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI Version</td>
<td>string</td>
<td>AMBA 3, AXI or AMBA 3 AXI</td>
<td>Specifies the AXI version and signals that Platform Designer generates for the slave and master interfaces of the bridge.</td>
</tr>
<tr>
<td>Data Width</td>
<td>integer</td>
<td>8:1024</td>
<td>Controls the width of the data for the master and slave interfaces.</td>
</tr>
<tr>
<td>Address Width</td>
<td>integer</td>
<td>1-64 bits</td>
<td>Controls the width of the address for the master and slave interfaces.</td>
</tr>
<tr>
<td>AWUSER Width</td>
<td>integer</td>
<td>1-64 bits</td>
<td>Controls the width of the write address channel sideband signals of the master and slave interfaces.</td>
</tr>
<tr>
<td>ARUSER Width</td>
<td>integer</td>
<td>1-64 bits</td>
<td>Controls the width of the read address channel sideband signals of the master and slave interfaces.</td>
</tr>
<tr>
<td>WUSER Width</td>
<td>integer</td>
<td>1-64 bits</td>
<td>Controls the width of the write data channel sideband signals of the master and slave interfaces.</td>
</tr>
<tr>
<td>RUSER Width</td>
<td>integer</td>
<td>1-16 bits</td>
<td>Controls the width of the read data channel sideband signals of the master and slave interfaces.</td>
</tr>
<tr>
<td>BUSER Width</td>
<td>integer</td>
<td>1-16 bits</td>
<td>Controls the width of the write response channel sideband signals of the master and slave interfaces.</td>
</tr>
</tbody>
</table>
5.1.6.3. AXI Bridge Slave and Master Interface Parameters

Table 113. AXI Bridge Slave and Master Interface Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID Width</td>
<td>Controls the width of the thread ID of the master and slave interfaces.</td>
</tr>
<tr>
<td>Write/Read/Combined Acceptance Capability</td>
<td>Controls the depth of the FIFO that Platform Designer needs in the interconnect agents based on the maximum pending commands that the slave interface accepts.</td>
</tr>
<tr>
<td>Write/Read/Combined Issuing Capability</td>
<td>Controls the depth of the FIFO that Platform Designer needs in the interconnect agents based on the maximum pending commands that the master interface issues. Issuing capability must follow acceptance capability to avoid unnecessary creation of FIFOs in the bridge.</td>
</tr>
</tbody>
</table>

Note: Maximum acceptance/issuing capability is a model-only parameter and does not influence the bridge HDL. The bridge does not backpressure when this limit is reached. Downstream components or the interconnect must apply backpressure.

5.1.7. AXI Timeout Bridge Intel FPGA IP

The AXI Timeout Bridge Intel FPGA IP allows your system to recover when it freezes, and facilitates debugging. You can place an AXI Timeout Bridge between a single master and a single slave if you know that the slave may time out and cause your system to freeze. If a slave does not accept a command or respond to a command it accepted, its master can wait indefinitely.

Figure 180. AXI Timeout Bridge

For a domain with multiple masters and slaves, placement of an AXI Timeout Bridge in your design may be beneficial in the following scenarios:

- To recover from a freeze, place the bridge near the slave. If the master attempts to communicate with a slave that freezes, the AXI Timeout Bridge frees the master by generating error responses. The master is then able to communicate with another slave.

- When debugging your system, place the AXI Timeout Bridge near the master. This placement enables you to identify the origin of the burst, and to obtain the full address from the master. Additionally, placing an AXI Timeout Bridge near the master enables you to identify the target slave for the burst.

Note: If you place the bridge at the slave’s side and you have multiple slaves connected to the same master, you do not get the full address.
5.1.7.1. AXI Timeout Bridge Stages

A timeout occurs when the internal timer in the bridge exceeds the specified number of cycles within which a burst must complete from start to end.
When a timeout occurs, the AXI Timeout Bridge asserts an interrupt and reports the burst that caused the timeout to the Configuration and Status Register (CSR).

The bridge then generates error responses back to the master on behalf of the unresponsive slave. This stage frees the master and certifies the unresponsive slave as dysfunctional.

The AXI Timeout Bridge accepts subsequent write addresses, write data, and read addresses to the dysfunctional slave. The bridge does not accept outstanding write responses, and read data from the dysfunctional slave is not passed through to the master.

The awvalid, wvalid, bready, arvalid, and rready ports are held low at the master interface of the bridge.

Note: After a timeout, awvalid, wvalid, and arvalid may be dropped before they are accepted by awready at the master interface. While the behavior violates the AXI specification, it occurs only on an interface connected to the slave which has been certified dysfunctional by the AXI Timeout Bridge.

Write channel refers to the AXI write address, data and response channels. Similarly, read channel refers to the AXI read address and data channels. AXI write and read channels are independent of each other. However, when a timeout occurs on either channel, the bridge generates error responses on both channels.
Table 114. Burst Start and End Definitions for the AXI Timeout Bridge

<table>
<thead>
<tr>
<th>Channel</th>
<th>Start</th>
<th>End</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write</td>
<td>When an address is issued. First cycle of awvalid, even if data of the same burst is issued before the address (first cycle of wvalid).</td>
<td>When the response is issued. First cycle of bvalid.</td>
</tr>
<tr>
<td>Read</td>
<td>When an address is issued. First cycle of arvalid.</td>
<td>When the last data is issued. First cycle of rvalid and rlast.</td>
</tr>
</tbody>
</table>

The AXI Timeout Bridge has four required interfaces: Master, Slave, Configuration and Status Register (CSR) (AMBA 3 AXI-Lite), and Interrupt. Platform Designer allows the AXI Timeout Bridge to connect to any AMBA 3 AXI, AMBA 3 AXI, or Avalon master or slave interface. Avalon masters must utilize the bridge's interrupt output to detect a timeout.

The bridge slave interface accepts write addresses, write data, and read addresses, and then generates the SLVERR response at the write response and read data channels. Do not use buser, rdata and ruser at this stage of processing.

To resume normal operation, the dysfunctional slave must be reset and the bridge notified of the change in status via the CSR. Once the CSR notifies the bridge that the slave is ready, the bridge does not accept new commands until all outstanding bursts are responded to with an error response.

The CSR has a 4-bit address width and a 32-bit data width. The CSR reports status and address information when the bridge asserts an interrupt.

Table 115. CSR Interrupt Status Information for the AXI Timeout Bridge

<table>
<thead>
<tr>
<th>Address</th>
<th>Attribute</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>write-only</td>
<td>Slave is reset</td>
</tr>
<tr>
<td>0x4</td>
<td>read-only</td>
<td>Timed out operation</td>
</tr>
<tr>
<td>0x8 through 0xF</td>
<td>read-only</td>
<td>Timed out address</td>
</tr>
</tbody>
</table>

5.1.7.2. AXI Timeout Bridge Parameters

Table 116. AXI Timeout Bridge Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID width</td>
<td>The width of awid, bid, arid, or rid.</td>
</tr>
<tr>
<td>Address width</td>
<td>The width of awaddr or araddr.</td>
</tr>
<tr>
<td>Data width</td>
<td>The width of wdata or rdata.</td>
</tr>
<tr>
<td>User width</td>
<td>The width of awuser, wuser, buser, aruser, or ruser.</td>
</tr>
<tr>
<td>Maximum number of outstanding writes</td>
<td>The expected maximum number of outstanding writes.</td>
</tr>
<tr>
<td>Maximum number of outstanding reads</td>
<td>The expected maximum number of outstanding reads.</td>
</tr>
<tr>
<td>Maximum number of cycles</td>
<td>The number of cycles within which a burst must complete.</td>
</tr>
</tbody>
</table>
5.1.8. Address Span Extender Intel FPGA IP

The Address Span Extender Intel FPGA IP allows memory-mapped master interfaces to access a larger or smaller address map than the width of their address signals allows. The Address Span Extender IP splits the addressable space into multiple separate windows, so that the master can access the appropriate part of the memory through the window.

The Address Span Extender does not limit master and slave widths to a 32-bit and 64-bit configuration. You can use the Address Span Extender with 1-64 bit address windows.

Figure 183. Address Span Extender Intel FPGA IP

If a processor can address only 2 GB of an address span, and your system contains 4 GB of memory, the Address Span Extender can provide two, 2 GB windows in the 4 GB memory address space. This issue sometimes occurs with Intel SoC devices.

For example, an HPS subsystem in an SoC device can address only 1 GB of an address span within the FPGA, using the HPS-to-FPGA bridge. The Address Span Extender enables the SoC device to address all the address space in the FPGA using multiple 1 GB windows.

5.1.8.1. CTRL Register Layout

The control registers consist of one 64-bit register for each window, where you specify the window’s base address. For example, if `CTRL_BASE` is the base address of the control register, and address span extender contains two windows (0 and 1), then window 0’s control register starts at `CTRL_BASE`, and window 1’s control register starts at `CTRL_BASE + 8` (using byte addresses).
5.1.8.2. Address Span Extender Parameters

Table 117. Address Span Extender Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Datapath Width</td>
<td>Width of write data and read data signals.</td>
</tr>
<tr>
<td>Expanded Master Byte Address Width</td>
<td>Width of the master byte address port. That is, the address span size of all the downstream slaves that attach to the address span extender.</td>
</tr>
<tr>
<td>Slave Word Address Width</td>
<td>Width of the slave word address port. That is, the address span size of the downstream slaves that the upstream master accesses.</td>
</tr>
<tr>
<td>Burstcount Width</td>
<td>Burst count port width of the downstream slave and the upstream master that attach to the address span extender.</td>
</tr>
<tr>
<td>Number of sub-windows</td>
<td>The slave port can represent one or more windows in the master address span. You can subdivide the slave address span into ( N ) equal spans in ( N ) sub-windows. A remapping register in the CSR slave represents each sub-window, and configures the base address that each sub-window remaps to. The address span extender replaces the upper bits of the address with the stored index value in the remapping register before the master initiates a transaction.</td>
</tr>
<tr>
<td>Enable Slave Control Port</td>
<td>Dictates run-time control over the sub-window indexes. If you can define static re-mappings that do not need any change, you do not need to enable this CSR slave.</td>
</tr>
<tr>
<td>Maximum Pending Reads</td>
<td>Sets the bridge slave's <code>maximumPendingReadTransactions</code> property. In certain system configurations, you must increase this value to improve performance. This value usually aligns with the properties of the downstream slaves that you attach to this bridge.</td>
</tr>
</tbody>
</table>

5.1.8.3. Calculating the Address Span Extender Slave Address

The diagram describes how Platform Designer calculates the slave address. In this example, the address span extender is configured with a 28-bit address space for slaves. The upper 2 bits \([27:26]\) are used to select the control registers.

The lower 26 bits \([25:0]\) originate from the address span extender’s data port, and are the offset into a particular window.

Figure 184. Address Span Extender
5.1.8.4. Using the Address Span Extender

This example shows when and how to use address span extender component in your Platform Designer design.

Figure 185. Block Diagram with Address Span Extender

In the above design, a 32-bit master shares 4 GB SDRAM with an external streaming interface. The master has the path to access streaming data from the SDRAM DDR memory. However, if you connect the whole 32-bit address bus of the master to the SDRAM DDR memory, you cannot connect the master to peripherals such as LED or UART. To avoid this situation, you can implement the address span extender between the master and DDR memory. The address span extender allows the master to access the SDRAM DDR memory and the peripherals at the same time.

To implement address span extender for the above example, you can divide the address window of the address span extender into two sub-windows of 512 MB each. The sub-window 0 is for the master program area. You can dynamically map the sub-window 1 to any area other than the program area.

You can change the offset of the address window by setting the base address of sub-window 1 to the control register of the address span extender. However, you must make sure that the sub-window address span masks the base address. You can choose any arbitrary base address. If you set the value 0xa000_0000 to the control register, Platform Designer maps the sub-window 1 to 0xa000_0000.
Table 118. CSR Mapping Table

<table>
<thead>
<tr>
<th>Address</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8000_0000</td>
<td>0x0000_0000</td>
</tr>
<tr>
<td>0x8000_0008</td>
<td>0xa000_0000</td>
</tr>
</tbody>
</table>

Figure 186. Memory mapping for Address Span Extender

The table below indicates the Platform Designer parameter settings for this address span extender example.

Table 119. Parameter Settings for the Address Span Extender Example

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Datapath Width</td>
<td>32 bits</td>
<td>The CPU has 32-bits data width and the SDRAM DDR memory has 512-bits data width. Since the transaction between the master and SDRAM DDR memory is minimal, set the datapath width to align with the upstream master.</td>
</tr>
<tr>
<td>Expanded Master Byte Address</td>
<td>32 bits</td>
<td>The address span extender has a 4 GB address span.</td>
</tr>
<tr>
<td>Slave Word Address Width</td>
<td>18 bits</td>
<td>There are two 512 MB sub-windows in reserve for the master. The number of bytes over the data word width in the Datapath Properties (4 bytes for this example) accounts for the slave address.</td>
</tr>
<tr>
<td>Burstcount Width</td>
<td>4 bits</td>
<td>The address span extender must handle up to 8 words burst in this example.</td>
</tr>
<tr>
<td>Number of sub-windows</td>
<td>2</td>
<td>Address window of the address span extender has two sub-windows of 512 MB each.</td>
</tr>
<tr>
<td>Enable Slave Control Port</td>
<td>true</td>
<td>The address span extender component must have control to change the base address of the sub-window.</td>
</tr>
<tr>
<td>Maximum Pending Reads</td>
<td>4</td>
<td>This number is the same as SDRAM DDR memory burst count.</td>
</tr>
</tbody>
</table>
Note: You can view the address span extender connections in the System View tab. The windowed slave port and control port connect to the master. The expanded master port connects to the SDRAM DDR memory.

5.1.8.5. Alternate Options for the Address Span Extender

You can set parameters for the address span extender with an initial fixed address value. Enter an address for the Reset Default for Master Window option, and select True for the Disable Slave Control Port option. This allows the address span extender to function as a fixed, non-programmable component.

Each sub-window is equal in size and stacks sequentially in the windowed slave interface's address space. To control the fixed address bits of a particular sub-window, you can write to the sub-window's register in the register control slave interface. Platform Designer structures the logic so that Platform Designer can optimize and remove bits that are not needed.
If Burstcount Width is greater than 1, Platform Designer processes the read burst in a single cycle, and assumes all byteenable signals are asserted on every cycle.

5.1.8.6. Nios II Support

If the address span extender window is fixed, for example, the Disable Slave Control Port option is turned on, then the address span extender performs as a bridge. Components on the slave side of the address span extender that are within the window are visible to the Nios II processor. Components partially within a window appear to the Nios II processor as if they have a reduced span. For example, a memory partially within a window appears as having a smaller size.

You can also use the address span extender to provide a window for the Nios II processor, so that the HPS memory map is visible to the Nios II processor. This technique allows the Nios II processor to communicate with HPS peripherals.

In the example, a Nios II processor has an address span extender from address 0x40000 to 0x80000. There is a window within the address span extender starting at 0x100000. Within the address span extender’s address space there is a slave at base address 0x110000. The slave appears to the Nios II processor as being at address:

\[
\text{Effective Slave Base Address} = 0x110000 - 0x100000 + 0x40000 = 0x050000
\]

Figure 188. Nios II Support and the Address Span Extender

The address span extender window is dynamic. For example, when the Disable Slave Control Port option is turned off, the Nios II processor is unable to see components on the slave side of the address span extender.

5.2. Error Response Slave Intel FPGA IP

The Error Response Slave IP provides a predictable error response service for master interfaces that attempt to access an undefined memory region.

The Error Response Slave is an AMBA 3 AXI component, and appears in the Platform Designer IP Catalog under Platform Designer Interconnect.
To comply with the AXI protocol, the interconnect logic must return the DECERR error response in cases where the interconnect cannot decode slave access. Therefore, an AXI system with address space not fully decoded to slave interfaces requires the Error Response Slave.

The Error Response Slave behaves like any other component in the system, and connects to other components via translation and adaptation interconnect logic. Connecting an Error Response Slave to masters of different data widths, including Avalon or AXI-Lite masters, can increase resource usage.

An Error Response Slave can connect to clock, reset, and IRQ signals as well as AMBA 3 AXI and AMBA 4 AXI master interfaces without instantiating a bridge. When you connect an Error Response Slave to a master, the Error Response Slave accepts cycles sent from the master, and returns the DECERR error response. On the AXI interface, the Error Response Slave supports only a read and write acceptance of capability 1, and does not support write data interleaving. The Error Response Slave can return responses when simultaneously targeted by a read and write cycle, because its read and write channels are independent.

An optional Avalon interface on the Error Response Slave provides information in a set of CSR registers. CSR registers log the required information when returning an error response.

- To set the Error Response Slave as the default slave for a master interface in your system, connect the slave to the master in your Platform Designer system.
- A system can contain more than one Error Response Slave.
- As a best practice, instantiate separate Error Response Slave components for each AXI master in your system.

**Related Information**

- [AMBA 3 AXI Protocol Specification Support (version 1.0)](page 222)
- [Designating a Default Slave](page 330)

### 5.2.1. Error Response Slave Parameters

**Figure 189. Error Response Slave Parameter Editor**
If you turn on **Enable CSR Support (for error logging)** more parameters become available.

**Figure 190. Error Response Slave Parameter Editor with Enabled CSR Support**

```
Table 120. Error Response Slave Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI master ID width</td>
<td>1-8 bits</td>
<td>Specifies the master ID width for error logging.</td>
</tr>
<tr>
<td>AXI address width</td>
<td>8-64 bits</td>
<td>Specifies the address width for error logging. This value also affects the overall address width of the system, and should not exceed the maximum address width required in the system.</td>
</tr>
<tr>
<td>AXI data width</td>
<td>32, 64, or 128 bits</td>
<td>Specifies the data width for error logging.</td>
</tr>
<tr>
<td>Enable CSR Support (for error logging)</td>
<td>On / Off</td>
<td>When turned on, instantiates an Avalon CSR interface for error logging.</td>
</tr>
<tr>
<td>CSR Error Log Depth</td>
<td>1-16 bits</td>
<td>Depth of the transaction log, for example, the number of transactions the CSR logs for cycles with errors.</td>
</tr>
<tr>
<td>Register Avalon CSR inputs</td>
<td>On / Off</td>
<td>When turned on, controls debug access to the CSR interface.</td>
</tr>
</tbody>
</table>
```

### 5.2.2. Error Response Slave CSR Registers

The Error Response Slave with enabled CSR support provides a service to handle access violations. This service uses CSR registers for status and logging purposes.

The sequence of actions in the access violation service is equivalent for read and write access violations, but the CSR status bits and log registers are different.

#### 5.2.2.1. Error Response Slave Access Violation Service

When an access violation occurs, and the CSR port is enabled:

1. The Error Response Slave generates an interrupt:
For a read access violation, the Error Response Slave sets the **Read Access Violation Interrupt register bit** in the **Interrupt Status register**.

For a write access violation, the Error Response Slave sets the **Write Access Violation Interrupt register bit** in the **Interrupt Status register**.

2. The Error Response Slave transfers transaction information to the access violation log FIFO. The amount of information that the FIFO can handle is given by the **Error Log Depth** parameter.

   You define the **Error Log Depth** in the **Parameter Editor**, when you enable CSR Support.

3. Software reads entries of the access violation log FIFO until the corresponding **cycle log valid** bit is cleared, and then exits the service routine.

   - The **Read cycle log valid** bit is in the **Read Access Violation Log CSR Registers**.
   - The **Write cycle log valid** bit is in the **Write Access Violation Log CSR Registers**.

4. The Error Response Slave clears the interrupt bit when there are no access violations to report.

   Some special cases are:

   - If any error occurs when the FIFO is full, the Error Response Slave sets the corresponding **Access Violation Interrupt Overflow register bit** (bits 2 and 3 of the Status Register for write and read access violations, respectively). Setting this bit means that not all error entries were written to the access violation log.
   - After Software reads an entry in the Access Violation log, the Error Response Slave can write a new entry to the log.
   - Software can specify the number of entries to read before determining that the access violation service is taking too long to complete, and exit the routine.

### 5.2.2.2. CSR Interrupt Status Registers

**Table 121. CSR Interrupt Status Registers**

For CSR register maps: Address = Memory Address Base + Offset.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>31:4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RW1C</td>
<td>0</td>
<td>0</td>
<td>Read Access Violation Interrupt Overflow register Asserted when a read access causes the Interconnect to return a DECERR response, and the buffer log depth is full. Indicates that there is a logging error lost due to an exceeded buffer log depth. Cleared by setting the bit to 1.</td>
</tr>
<tr>
<td>2</td>
<td>RW1C</td>
<td>0</td>
<td>0</td>
<td>Write Access Violation Interrupt Overflow register Asserted when a write access causes the Interconnect to return a DECERR response, and the buffer log depth is full. Indicates that there is a logging error lost due to an exceeded buffer log depth. Cleared by setting the bit to 1.</td>
</tr>
<tr>
<td>1</td>
<td>RW1C</td>
<td>0</td>
<td>0</td>
<td>Read Access Violation Interrupt register</td>
</tr>
</tbody>
</table>
5.2.2.3. CSR Read Access Violation Log Registers

The CSR read access violation log settings are valid only when an associated read interrupt register is set. Read this set of registers until the validity bit is cleared.

Table 122. CSR Read Access Violation Log Registers

<table>
<thead>
<tr>
<th>Offset</th>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x100</td>
<td>31:13</td>
<td>Reserved</td>
<td>0</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0x104</td>
<td>31:0</td>
<td>RO</td>
<td>0</td>
<td>Offending read cycle burst type: Specifies the burst type of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>0x108</td>
<td>31:0</td>
<td>RO</td>
<td>0</td>
<td>Offending read cycle burst length: Specifies the burst length of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>0x10C</td>
<td>31:0</td>
<td>RO</td>
<td>0</td>
<td>Offending read cycle burst size: Specifies the burst size of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>0</td>
<td>Read cycle log valid: Specifies the validity of the read access violation log. This bit is cleared when the interrupt register is cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5.2.2.4. CSR Write Access Violation Log Registers

The CSR write access violation log settings are valid only when an associated write interrupt register is set. Read this set of registers until the validity bit is cleared.

Table 123. CSR Write Access Violation Log

<table>
<thead>
<tr>
<th>Offset</th>
<th>Bits</th>
<th>Attribute</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x190</td>
<td>31:13</td>
<td>Reserved</td>
<td>0</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0x194</td>
<td>12:11</td>
<td>RO</td>
<td>0</td>
<td>Offending write cycle burst type: Specifies the burst type of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>Offset</td>
<td>Bits</td>
<td>Attribute</td>
<td>Default</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
<td>-----------</td>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>10:7</td>
<td>R0</td>
<td>0</td>
<td></td>
<td>Offending write cycle burst length: Specifies the burst length of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>6:4</td>
<td>R0</td>
<td>0</td>
<td></td>
<td>Offending write cycle burst size: Specifies the burst size of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>3:1</td>
<td>R0</td>
<td>0</td>
<td></td>
<td>Offending write cycle PROT: Specifies the PROT of the initiating cycle that causes the access violation.</td>
</tr>
<tr>
<td>0</td>
<td>R0</td>
<td>0</td>
<td></td>
<td>Write cycle log valid: Specifies whether the log for the transaction is valid. This bit is cleared when the interrupt register is cleared.</td>
</tr>
<tr>
<td>0x194</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle ID: Master ID for the cycle that causes the access violation.</td>
</tr>
<tr>
<td>0x198</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle target address: Write target address for the cycle that causes the access violation (lower 32-bit).</td>
</tr>
<tr>
<td>0x19C</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle target address: Write target address for the cycle that causes the access violation (upper 32-bit). Valid only if widest address in system is larger than 32 bits.</td>
</tr>
<tr>
<td>0x1A0</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle first write data: First 32 bits of the write data for the write cycle that causes the access violation. Note: When this register is read, the current write access violation log is recovered from FIFO, when the data width is 32 bits.</td>
</tr>
<tr>
<td>0x1A4</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle first write data: Bits [63:32] of the write data for the write cycle that causes the access violation. Valid only if the data width is greater than 32 bits.</td>
</tr>
<tr>
<td>0x1A8</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle first write data: Bits [95:64] of the write data for the write cycle that causes the access violation. Valid only if the data width is greater than 64 bits.</td>
</tr>
<tr>
<td>0x1AC</td>
<td>31:0</td>
<td>R0</td>
<td>0</td>
<td>Offending write cycle first write data: The first bits [127:96] of the write data for the write cycle that causes the access violation. Valid only if the data width is greater than 64 bits. Note: When this register is read, the current write access violation log is recovered from FIFO.</td>
</tr>
</tbody>
</table>

### 5.2.3. Designating a Default Slave

You can designate any slave in your Platform Designer system as the error response default slave. The default slave you designate provides an error response service for masters that attempt access to an undefined memory region.

1. In your Platform Designer system, in the **System View** tab, right-click the header and turn on **Show Default Slave Column**.
2. Select the slave that you want to designate as the default slave, and then click the checkbox for the slave in the **Default Slave** column.
3. In the **System View** tab, in the **Connections** column, connect the designated default slave to one or more masters.

**Related Information**

- **Specifying a Default Slave** on page 57
5.3. Tri-State Components

The tri-state interface type allows you to design Platform Designer subsystems that connect to tri-state devices on your PCB. You can use tri-state components to implement pin sharing, convert between unidirectional and bidirectional signals, and create tri-state controllers for devices whose interfaces can be described using the tri-state signal types.

Example 28. Tri-State Conduit System to Control Off-Chip SRAM and Flash Devices

In this example, there are two generic Tri-State Conduit Controllers. The first is customized to control a flash memory. The second is customized to control an off-chip SSRAM. The Tri-State Conduit Pin Sharer multiplexes between these two controllers, and the Tri-State Conduit Bridge converts between an on-chip encoding of tri-state signals and true bidirectional signals. By default, the Tri-State Conduit Pin Sharer and Tri-State Conduit Bridge present byte addresses. Typically, each address location contains more than one byte of data.

Figure 191. Tri-State Conduit System to Control Off-Chip SRAM and Flash Devices

Address Connections from Platform Designer System to PCB

The flash device operates on 16-bit words and must ignore the least-significant bit of the Avalon memorymapped address. The figure shows $addr[0]$ as not connected. The SSRAM memory operates on 32-bit words and must ignore the two low-order memory bits. Because neither device requires a byte address, $addr[0]$ is not routed on the PCB.

The flash device responds to address range 0 MB to 8 MB-1. The SSRAM responds to address range 8 MB to 10 MB-1. The PCB schematic for the PCB connects $addr[21:0]$ to $addr[18:0]$ of the SSRAM device because the SSRAM responds to...
32-bit word address. The 8 MB flash device accesses 16-bit words; consequently, the schematic does not connect addr[0]. The chipselect signals select between the two devices.

**Figure 192. Address Connections from Platform Designer System to PCB**

![Address Connections from Platform Designer System to PCB](image)

**Note:** If you create a custom tri-state conduit master with word aligned addresses, the Tri-state Conduit Pin Sharer does not change or align the address signals.

**Figure 193. Tri-State Conduit System in Platform Designer**

![Tri-State Conduit System in Platform Designer](image)
5. Platform Designer System Design Components

5.3.1. Generic Tri-State Controller Intel FPGA IP

The Generic Tri-State Controller Intel FPGA IP provides a template for a controller. You can customize the Generic Tri-State Controller with various parameters to reflect the behavior of an off-chip device. The following types of parameters are available for the Generic Tri-State Controller:

- Width of the address and data signals
- Read and write wait times
- Bus turnaround time
- Data hold time

*Note:* In calculating delays, the Generic Tri-State Controller chooses the larger of the bus turnaround time and read latency. Turnaround time is measured from the time that a command is accepted, not from the time that the previous read returned data.

The Generic Tri-State Controller includes the following interfaces:

- **Memory-mapped slave interface**—This interface connects to a memory-mapped master, such as a processor.
- **Tristate Conduit Master interface**—The tri-state master interface usually connects to the tri-state conduit slave interface of the tri-state conduit pin sharer.
- **Clock sink**—The component’s clock reference. You must connect this interface to a clock source.
- **Reset sink**—This interface connects to a reset source interface.

5.3.2. Tri-State Conduit Pin Sharer Intel FPGA IP

The Tri-State Conduit Pin Sharer Intel FPGA IP multiplexes between the signals of the connected tri-state controllers. You connect all signals from the tri-state controllers to the Tri-State Conduit Pin Sharer IP, and then use the parameter editor to specify the signals that are shared.

The parameter editor includes a **Shared Signal Name** column. If the widths of shared signals differ, the signals are aligned on their 0th bit and the higher-order pins are driven to 0 whenever the smaller signal has control of the bus. Unshared signals always propagate through the pin sharer. The tri-state conduit pin sharer uses the round-robin arbiter to select between tri-state conduit controllers.
Figure 194. Tri-State Conduit Pin Sharer Parameter Editor

Note: All tri-state conduit components connected to a pin sharer must be in the same clock domain.

Related Information
Avalon Streaming Round Robin Scheduler Intel FPGA IP on page 358

5.3.3. Tri-State Conduit Bridge Intel FPGA IP

The Tri-State Conduit Bridge Intel FPGA IP instantiates bidirectional signals for each tri-state signal while passing all other signals straight through the component. The Tri-State Conduit Bridge registers all outgoing and incoming signals, which adds two cycles of latency for a read request. You must account for this additional pipelining when designing a custom controller. During reset, all outputs are placed in a high-impedance state. Outputs are enabled in the first clock cycle after reset is deasserted, and the output signals are then bidirectional.

5.4. Avalon Data Pattern Generator and Checker Intel FPGA IP

You can use the Avalon Data Pattern Generator IP to insert different error conditions, and then use the Avalon Data Pattern Checker IP to report these error conditions to the control interface, via an Avalon Memory-Mapped slave.

Similarly, for Avalon streaming interfaces, Avalon Data Pattern Generator IP generates data, and sends the data out on an Avalon streaming data interface. The Avalon Data Pattern Checker IP verifies the data. Optionally, you can format the data as packets, with accompanying start_of_packet and end_of_packet signals.
The **Throttle Seed** is the starting value for the throttle control random number generator. Intel recommends a unique value for each instance of the data pattern generator and checker IP cores in a system.

### 5.4.1. Avalon Data Pattern Generator Intel FPGA IP

The Avalon Data Pattern Generator IP accepts commands to generate data via an Avalon memory mapped command interface, and drives the generated data to an Avalon streaming data interface. You can parameterize most aspects of the Avalon streaming data interface, such as the number of error bits and data signal width, thus allowing you to test components with different interfaces.

#### Figure 195. Avalon Data Pattern Generator Intel FPGA IP

![Avalon Data Pattern Generator Intel FPGA IP Diagram]

The data pattern is calculated as: $\text{Symbol Value} = \text{Symbol Position in Packet} \oplus \text{Data Error Mask}$. Data that is not organized in packets is a single stream with no beginning or end. The Avalon Data Pattern Generator IP has a throttle register that is set via the Avalon memory mapped control interface. The Avalon Data Pattern Generator IP uses the value of the throttle register in conjunction with a pseudo-random number generator to throttle the data generation rate.

#### 5.4.1.1. Avalon Data Pattern Generator IP Command Interface

The command interface for the Avalon Data Pattern Generator is a 32-bit Avalon memory mapped write slave that accepts data generation commands. It is connected to a 16-element deep FIFO, thus allowing a master peripheral to drive commands into the Avalon Data Pattern Generator IP.

The command interface maps to the following registers: `cmd_lo` and `cmd_hi`. The command is pushed into the FIFO when the register `cmd_lo` (address 0) is addressed. When the FIFO is full, the command interface asserts the `waitrequest` signal. You can create errors by writing to the register `cmd_hi` (address 1). The errors are cleared when 0 is written to this register, or its respective fields.
5.4.1.2. Avalon Data Pattern Generator IP Control and Status Interface

The control and status interface of the Avalon Data Pattern Generator IP is a 32-bit Avalon memory mapped slave that allows you to enable or disable the data generation, as well as set the throttle. This interface also provides generation-time information, such as the number of channels and whether data packets are supported.

5.4.1.3. Avalon Data Pattern Generator IP Output Interface

The output interface of the Avalon Data Pattern Generator IP is an Avalon streaming interface that optionally supports data packets. You can configure the output interface to align with your system requirements. Depending on the incoming stream of commands, the output data may contain interleaved packet fragments for different channels. To keep track of the current symbol’s position within each packet, the Avalon Data Pattern Generator IP maintains an internal state for each channel.

You can configure the output interface of the Avalon Data Pattern Generator IP with the following parameters:

- **Number of Channels**—Number of channels that the Avalon Data Pattern Generator IP supports. Valid values are 1 to 256.
- **Data Bits Per Symbol**—Bits per symbol is related to the width of readdata and writedata signals, which must be a multiple of the bits per symbol.
- **Data Symbols Per Beat**—Number of symbols (words) that are transferred per beat. Valid values are 1 to 256.
- **Include Packet Support**—Indicates whether packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.
- **Error Signal Width (bits)**—Width of the error signal on the output interface. Valid values are 0 to 31. A value of 0 indicates that the error signal is not in use.

*Note:* If you change only bits per symbol, and do not change the data width, errors are generated.

5.4.1.4. Avalon Data Pattern Generator IP Functional Parameter

The Avalon Data Pattern Generator IP functional parameter allows you to configure the Avalon Data Pattern Generator as an entire system.

5.4.2. Avalon Data Pattern Checker Intel FPGA IP

The Avalon Data Pattern Checker Intel FPGA IP accepts data via an Avalon streaming interface and verifies it against a predetermined pattern that the Avalon Data Pattern Generator Intel FPGA IP produces. The Avalon Data Pattern Checker IP reports any exceptions to the control interface. You can parameterize most aspects of the Avalon Data Pattern Checker's Avalon streaming interface, such as the number of error bits, and the data signal width. This IP allows you to test components with different interfaces. The Avalon Data Pattern Checker IP has a throttle register that is set via the Avalon memory mapped control interface. The value of the throttle register controls the rate at which data is accepted.
The Avalon Data Pattern Checker IP detects exceptions and reports them to the control interface via a 32-element deep internal FIFO. Possible exceptions are data error, missing start-of-packet (SOP), missing end-of-packet (EOP), and signaled error.

As each exception occurs, an exception descriptor is pushed into the FIFO. If the same exception occurs more than once consecutively, only one exception descriptor is pushed into the FIFO. All exceptions are ignored when the FIFO is full. Exception descriptors are deleted from the FIFO after they are read by the control and status interface.

5.4.2.1. Avalon Data Pattern Checker IP Input Interface

The Avalon Data Pattern Checker IP input interface is an Avalon streaming interface that optionally supports data packets. You can configure the input interface to align with your system requirements. Incoming data may contain interleaved packet fragments. To keep track of the current symbol's position, the test pattern checker maintains an internal state for each channel.

5.4.2.2. Avalon Data Pattern Checker IP Control and Status Interface

The Avalon Data Pattern Checker IP control and status interface is a 32-bit Avalon memory mapped slave that allows you to enable or disable data acceptance, as well as set the throttle. This interface provides generation-time information, such as the number of channels and whether the Avalon Data Pattern Checker supports data packets. The control and status interface also provides information on the exceptions detected by the Avalon Data Pattern Checker IP. The interface obtains this information by reading from the exception FIFO.

5.4.2.3. Avalon Data Pattern Checker IP Functional Parameter

The Avalon Data Pattern Checker IP functional parameter allows you to configure the Avalon Data Pattern Checker IP as a whole system.
5.4.2.4. Avalon Data Pattern Checker Input Parameters

You can configure the input interface of the Avalon Data Pattern Checker IP using the following parameters:

- **Data Bits Per Symbol**—Bits per symbol is related to the width of `readdata` and `writedata` signals, which must be a multiple of the bits per symbol.
- **Data Symbols Per Beat**—Number of symbols (words) that are transferred per beat. Valid values are 1 to 32.
- **Include Packet Support**—Indicates whether data packet transfers are supported. Packet support includes the `startofpacket`, `endofpacket`, and `empty` signals.
- **Number of Channels**—Number of channels that the test pattern checker supports. Valid values are 1 to 256.
- **Error Signal Width (bits)**—Width of the `error` signal on the input interface. Valid values are 0 to 31. A value of 0 indicates that the `error` signal is not in use.

*Note:* If you change only bits per symbol, and do not change the data width, errors are generated.

5.4.3. Avalon Data Pattern Generator and Checker IP Software Programming Model

The HAL system library support, software files, and register maps describe the software programming model for the test pattern generator and checker cores.

5.4.3.1. HAL System Library Support

For Nios II processor users, Intel provides HAL system library drivers that allow you to initialize and access the Avalon Data Pattern Generator and Checker IPs. Intel recommends you use the provided drivers to access the IPs instead of accessing the registers directly.

For Nios II IDE users, copy the provided drivers from the following installation folders to your software application directory:

- `<IP installation directory>/ip/sopc_builder_ip/altera_Avalon_data_source/HAL`
- `<IP installation directory>/ip/sopc_builder_ip/altera_Avalon_data_sink/HAL`

*Note:* This instruction does not apply if you use the Nios II command-line tools.

5.4.3.2. Avalon Data Pattern Generator and Checker IP Files

The following files define the low-level access to the hardware, and provide the routines for the HAL device drivers.
• Avalon Data Pattern Generator IP files in <installation directory>/ip/sopc_builder_ip/altera_Avalon_data_source/HAL:
  — data_source_regs.h—header file that defines the test pattern generator’s register maps.
  — data_source_util.h, data_source_util.c—header and source code for the functions and variables required to integrate the driver into the HAL system library.

• Avalon Data Pattern Checker IP files in <installation directory>/ip/sopc_builder_ip/altera_Avalon_data_sink/HAL
  — data_sink_regs.h—header file that defines the IP register maps.
  — data_sink_util.h, data_sink_util.c—header and source code for the functions and variables required to integrate the driver into the HAL system library.

Note: Do not modify the Avalon Data Pattern Generator or Avalon Data Pattern Checker IP files.

5.4.3.3. Avalon Data Pattern Generator and Checker IP Register Maps

5.4.3.3.1. Avalon Data Pattern Generator IP Control and Status Registers

Table 124. Avalon Data Pattern Generator IP Control and Status Register Map
Each register is 32-bits wide.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>base + 0</td>
<td>status</td>
</tr>
<tr>
<td>base + 1</td>
<td>control</td>
</tr>
<tr>
<td>base + 2</td>
<td>fill</td>
</tr>
</tbody>
</table>

Table 125. Avalon Data Pattern Generator IP Status Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>ID</td>
<td>RO</td>
<td>A constant value of 0x64.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>NUMCHANNELS</td>
<td>RO</td>
<td>The configured number of channels.</td>
</tr>
<tr>
<td>[30:24]</td>
<td>NUMSYMBOLS</td>
<td>RO</td>
<td>The configured number of symbols per beat.</td>
</tr>
<tr>
<td>[31]</td>
<td>SUPPORTPACKETS</td>
<td>RO</td>
<td>A value of 1 indicates data packet support.</td>
</tr>
</tbody>
</table>

Table 126. Avalon Data Pattern Generator IP Control Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]</td>
<td>ENABLE</td>
<td>RW</td>
<td>Setting this bit to 1 enables the data pattern generator IP.</td>
</tr>
<tr>
<td>[7:1]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

continued...
### Table 127. Avalon Data Pattern Generator IP Fill Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16:8]</td>
<td>THROTTLE</td>
<td>RW</td>
<td>Specifies the throttle value which can be between 0–256, inclusively. The Data Pattern Generator IP uses this value in conjunction with a pseudo-random number generator to throttle the data generation rate.</td>
</tr>
<tr>
<td>[17]</td>
<td>SOFT RESET</td>
<td>RW</td>
<td>When this bit is set to 1, all internal counters and statistics are reset. Write 0 to this bit to exit reset.</td>
</tr>
<tr>
<td>[31:18]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 5.4.3.3.2. Avalon Data Pattern Generator IP Command Registers

#### Table 128. Avalon Data Pattern Generator IP Command Register Map

Shows the offset for the command registers. Each register is 32-bits wide.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>base + 0</td>
<td>cmd_lo</td>
</tr>
<tr>
<td>base + 1</td>
<td>cmd_hi</td>
</tr>
</tbody>
</table>

The cmd_lo is pushed into the FIFO only when the cmd_lo register is addressed.

#### Table 129. cmd_lo Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>SIZE</td>
<td>RW</td>
<td>The segment size in symbols. Except for the last segment in a packet, the size of all segments must be a multiple of the configured number of symbols per beat. If this condition is not met, the Data Pattern Generator IP inserts additional symbols to the segment to ensure the condition is fulfilled.</td>
</tr>
<tr>
<td>[29:16]</td>
<td>CHANNEL</td>
<td>RW</td>
<td>The channel to send the segment on. If the channel signal is less than 14 bits wide, the Data Pattern Generator IP uses the low order bits of this register to drive the signal.</td>
</tr>
<tr>
<td>[30]</td>
<td>SOP</td>
<td>RW</td>
<td>Set this bit to 1 when sending the first segment in a packet. This bit is ignored when data packets are not supported.</td>
</tr>
<tr>
<td>[31]</td>
<td>EOP</td>
<td>RW</td>
<td>Set this bit to 1 when sending the last segment in a packet. This bit is ignored when data packets are not supported.</td>
</tr>
</tbody>
</table>
Table 130. `cmd_hi` Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>SIGNALED ERROR</td>
<td>RW</td>
<td>Specifies the value to drive the error signal. A non-zero value creates a signaled error.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>DATA ERROR</td>
<td>RW</td>
<td>The output data is XORed with the contents of this register to create data errors. To stop creating data errors, set this register to 0.</td>
</tr>
<tr>
<td>[24]</td>
<td>SUPPRESS SOP</td>
<td>RW</td>
<td>Set this bit to 1 to suppress the assertion of the startofpacket signal when the first segment in a packet is sent.</td>
</tr>
<tr>
<td>[25]</td>
<td>SUPPRESS EOP</td>
<td>RW</td>
<td>Set this bit to 1 to suppress the assertion of the endofpacket signal when the last segment in a packet is sent.</td>
</tr>
</tbody>
</table>

5.4.3.3.3. Avalon Data Pattern Checker IP Control and Status Registers

Table 131. Avalon Data Pattern Generator and Checker IP Control and Status Register Map

Shows the offset for the control and status registers. Each register is 32 bits wide.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Register Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>base + 0</td>
<td>status</td>
</tr>
<tr>
<td>base + 1</td>
<td>control</td>
</tr>
<tr>
<td>base + 2</td>
<td>Reserved</td>
</tr>
<tr>
<td>base + 3</td>
<td></td>
</tr>
<tr>
<td>base + 4</td>
<td></td>
</tr>
<tr>
<td>base + 5</td>
<td>exception_descriptor</td>
</tr>
<tr>
<td>base + 6</td>
<td>indirect_select</td>
</tr>
<tr>
<td>base + 7</td>
<td>indirect_count</td>
</tr>
</tbody>
</table>

Table 132. Avalon Data Pattern Checker IP Status Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>ID</td>
<td>RO</td>
<td>Contains a constant value of 0x65.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>NUMCHANNELS</td>
<td>RO</td>
<td>The configured number of channels.</td>
</tr>
<tr>
<td>[30:24]</td>
<td>NUMSYMBOLS</td>
<td>RO</td>
<td>The configured number of symbols per beat.</td>
</tr>
<tr>
<td>[31]</td>
<td>SUPPORTPACKETS</td>
<td>RO</td>
<td>A value of 1 indicates packet support.</td>
</tr>
</tbody>
</table>

Table 133. Avalon Data Pattern Checker IP Control Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]</td>
<td>ENABLE</td>
<td>RW</td>
<td>Setting this bit to 1 enables the Data Pattern Checker IP.</td>
</tr>
<tr>
<td>[7:1]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[16:8]</td>
<td>THROTTLE</td>
<td>RW</td>
<td>Specifies the throttle value which can be between 0–256, inclusively.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Platform Designer uses this value in conjunction with a pseudo-random number generator to throttle the data generation rate.</td>
</tr>
</tbody>
</table>

continued...
Setting THROTTLE to 0 stops the Avalon Data Pattern Checker IP. Setting it to 256 causes the Avalon Data Pattern Checker IP to run at full throttle. Values between 0–256 result in a data rate proportional to the throttle value.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[17]</td>
<td>SOFT_RESET</td>
<td>RW</td>
<td>When this bit is set to 1, all internal counters and statistics are reset. Write 0 to this bit to exit reset.</td>
</tr>
<tr>
<td>[31:18]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If there is no exception, reading the exception_descriptor register bit register returns 0.

Table 134. exception_descriptor Register Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]</td>
<td>DATA ERROR</td>
<td>RO</td>
<td>A value of 1 indicates that an error is detected in the incoming data.</td>
</tr>
<tr>
<td>[7:3]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[15:8]</td>
<td>SIGNALLED ERROR</td>
<td>RO</td>
<td>The value of the error signal.</td>
</tr>
<tr>
<td>[23:16]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[31:24]</td>
<td>CHANNEL</td>
<td>RO</td>
<td>The channel on which the exception was detected.</td>
</tr>
</tbody>
</table>

Table 135. indirect_select Register Bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>INDIRECT CHANNEL</td>
<td>RW</td>
<td>Specifies the channel number that applies to the INDIRECT PACKET COUNT, INDIRECT SYMBOL COUNT, and INDIRECT ERROR COUNT registers.</td>
</tr>
<tr>
<td>[15:8]</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[31:16]</td>
<td>INDIRECT ERROR</td>
<td>RO</td>
<td>The number of data errors that occurred on the channel specified by INDIRECT CHANNEL.</td>
</tr>
</tbody>
</table>

Table 136. indirect_count Register Bits

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[15:0]</td>
<td>INDIRECT PACKET COUNT</td>
<td>RO</td>
<td>The number of data packets received on the channel specified by INDIRECT CHANNEL.</td>
</tr>
<tr>
<td>[31:16]</td>
<td>INDIRECT SYMBOL COUNT</td>
<td>RO</td>
<td>The number of symbols received on the channel specified by INDIRECT CHANNEL.</td>
</tr>
</tbody>
</table>

5.4.4. Avalon Data Pattern Generator IP API

The following subsections describe application programming interface (API) for the Avalon Data Pattern Generator IP.

Note: API functions are currently not available from the interrupt service routine (ISR).
5. Platform Designer System Design Components

5.4.4.1. data_source_reset()

Table 137. data_source_reset()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>void data_source_reset(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>void</td>
</tr>
<tr>
<td>Description</td>
<td>Resets the Avalon Data Pattern Generator IP, including all internal counters and FIFOs. The control and status registers are not reset by this function.</td>
</tr>
</tbody>
</table>

5.4.4.2. data_source_init()

Table 138. data_source_init()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_source_init(alt_u32 base, alt_u32 command_base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave. command_base—Base address of the command slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>1—Initialization is successful. 0—Initialization is unsuccessful.</td>
</tr>
</tbody>
</table>
| Description      | Performs the following operations to initialize the Avalon Data Pattern Generator IP:  
  - Resets and disables the Avalon Data Pattern Generator IP.  
  - Sets the maximum throttle.  
  - Clears all inserted errors. |
5.4.4.3. data_source_get_id()

Table 139. data_source_get_id()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_get_id(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>base</code>—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Avalon Data Pattern Generator IP identifier.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the Avalon Data Pattern Generator IP identifier.</td>
</tr>
</tbody>
</table>

5.4.4.4. data_source_get_supports_packets()

Table 140. data_source_get_supports_packets()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_init(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>base</code>—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>1—Data packets are supported. 0—Data packets are not supported.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if the Avalon Data Pattern Generator IP supports data packets.</td>
</tr>
</tbody>
</table>

5.4.4.5. data_source_get_num_channels()

Table 141. data_source_get_num_channels()

<table>
<thead>
<tr>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_get_num_channels(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>base</code>—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of channels supported.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of channels supported by the Avalon Data Pattern Generator IP.</td>
</tr>
</tbody>
</table>

5.4.4.6. data_source_get_symbols_per_cycle()

Table 142. data_source_get_symbols_per_cycle()

<table>
<thead>
<tr>
<th>Description</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_get_symbols(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
</tbody>
</table>

continued...
5.4.4.7. `data_source_get_enable()`

Table 143. `data_source_get_enable()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_get_enable(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>base—Base address of the control and status slave.</code></td>
</tr>
<tr>
<td>Returns</td>
<td>Value of the <code>ENABLE</code> bit.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the value of the <code>ENABLE</code> bit.</td>
</tr>
</tbody>
</table>

5.4.4.8. `data_source_set_enable()`

Table 144. `data_source_set_enable()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>void data_source_set_enable(alt_u32 base, alt_u32 value);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>base—Base address of the control and status slave. value—ENABLE bit set to the value of this parameter.</code></td>
</tr>
<tr>
<td>Returns</td>
<td><code>void</code></td>
</tr>
<tr>
<td>Description</td>
<td>Enables or disables the Avalon Data Pattern Generator IP. When disabled, the Avalon Data Pattern Generator IP stops data transmission but continues to accept commands and stores them in the FIFO.</td>
</tr>
</tbody>
</table>

5.4.4.9. `data_source_get_throttle()`

Table 145. `data_source_get_throttle()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_source_get_throttle(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_source_util.h&gt;</code></td>
</tr>
</tbody>
</table>
### 5.4.4.10. data_source_set_throttle()

**Table 146. data_source_set_throttle()**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>void data_source_set_throttle(alt_u32 base, alt_u32 value);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
<tr>
<td>Parameters base</td>
<td>Base address of the control and status slave.</td>
</tr>
<tr>
<td>Parameters value</td>
<td>Throttle value.</td>
</tr>
<tr>
<td>Returns</td>
<td>void</td>
</tr>
<tr>
<td>Description</td>
<td>Sets the throttle value, which can be between 0–256 inclusively. The throttle value, when divided by 256 yields the rate at which the Avalon Data Pattern Generator IP sends data.</td>
</tr>
</tbody>
</table>

### 5.4.4.11. data_source_is_busy()

**Table 147. data_source_is_busy()**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_source_is_busy(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
<tr>
<td>Parameters base</td>
<td>Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns 1</td>
<td>Avalon Data Pattern Generator IP is busy.</td>
</tr>
<tr>
<td>Returns 0</td>
<td>Avalon Data Pattern Generator IP is not busy.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if the Avalon Data Pattern Generator IP is busy. The Avalon Data Pattern Generator IP is busy when it is sending data or has data in the command FIFO to be sent.</td>
</tr>
</tbody>
</table>

### 5.4.4.12. data_source_fill_level()

**Table 148. data_source_fill_level()**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_source_fill_level(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
</tbody>
</table>

*continued...*
5.4.4.13. data_source_send_data()

**Table 149.  data_source_send_data()**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_source_send_data(alt_u32 cmd_base, alt_u16 channel, alt_u16 size, alt_u32 flags, alt_u16 error, alt_u8 data_error_mask);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_source_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>cmd_base—Base address of the command slave. channel—Channel to send the data. size—Data size. flags—Specifies whether to send or suppress SOP and EOP signals. Valid values are DATA_SOURCE_SEND_SOP, DATA_SOURCE_SEND_EOP, DATA_SOURCE_SEND_SUPPRESS_SOP and DATA_SOURCE_SEND_SUPPRESS_EOP. error—Value asserted on the error signal on the output interface. data_error_mask—Parameter and the data are XORed together to produce erroneous data.</td>
</tr>
<tr>
<td>Returns</td>
<td>Returns 1.</td>
</tr>
<tr>
<td>Description</td>
<td>Sends a data fragment to the specified channel. If data packets are supported, applications must ensure consistent usage of SOP and EOP in each channel. Except for the last segment in a packet, the length of each segment is a multiple of the data width. If data packets are not supported, applications must ensure that there are no SOP and EOP indicators in the data. The length of each segment in a packet is a multiple of the data width.</td>
</tr>
</tbody>
</table>

5.4.5. Avalon Data Pattern Checker IP API

The following subsections describe API for the Avalon Data Pattern Checker IP. The API functions are currently not available from the ISR.

data_sink_reset() on page 348
data_sink_init() on page 348
data_sink_get_id() on page 349
data_sink_get_supports_packets() on page 349
data_sink_get_num_channels() on page 349
data_sink_get_symbols_per_cycle() on page 349
data_sink_get_enable() on page 350
data_sink_set_enable() on page 350
data_sink_get_throttle() on page 350
data_sink_set_throttle() on page 351
data_sink_get_packet_count() on page 351  
data_sink_get_error_count() on page 351  
data_sink_get_symbol_count() on page 352  
data_sink_get_exception() on page 352  
data_sink_exception_is_exception() on page 352  
data_sink_exception_has_data_error() on page 353  
data_sink_exception_has_missing_sop() on page 353  
data_sink_exception_has_missing_eop() on page 353  
data_sink_exception_signalled_error() on page 354  
data_sink_exception_channel() on page 354

5.4.5.1. data_sink_reset()

Table 150. data_sink_reset()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>void data_sink_reset(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>void</td>
</tr>
<tr>
<td>Description</td>
<td>Resets the Avalon Data Pattern Checker IP, including all internal counters.</td>
</tr>
</tbody>
</table>

5.4.5.2. data_sink_init()

Table 151. data_sink_init()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_source_init(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
</tbody>
</table>
| Returns          | 1—Initialization is successful.  
                   0—Initialization is unsuccessful. |
| Description      | Performs the following operations to initialize the Avalon Data Pattern Checker IP:  
                   • Resets and disables the Avalon Data Pattern Checker IP.  
                   • Sets the throttle to the maximum value. |
### 5.4.5.3. `data_sink_get_id()`

**Table 152. `data_sink_get_id()`**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_get_id(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Avalon Data Pattern Checker IP identifier.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the Avalon Data Pattern Checker IP identifier.</td>
</tr>
</tbody>
</table>

### 5.4.5.4. `data_sink_get_supports_packets()`

**Table 153. `data_sink_get_supports_packets()`**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_init(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>Base address of the control and status slave.</td>
</tr>
</tbody>
</table>
| Returns          | `1`—Data packets are supported.  
  `0`—Data packets are not supported. |
| Description      | Checks if the Avalon Data Pattern Checker IP supports data packets. |

### 5.4.5.5. `data_sink_get_num_channels()`

**Table 154. `data_sink_get_num_channels()`**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_get_num_channels(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of channels supported.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of channels supported by the Avalon Data Pattern Checker IP.</td>
</tr>
</tbody>
</table>

### 5.4.5.6. `data_sink_get_symbols_per_cycle()`

**Table 155. `data_sink_get_symbols_per_cycle()`**

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_get_symbols(alt_u32 base);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
</tbody>
</table>

---

*continued*...
5.4.5.7. `data_sink_get_enable()`

Table 156. `data_sink_get_enable()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of symbols received in a beat.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of symbols received by the Avalon Data Pattern Checker IP in each beat.</td>
</tr>
</tbody>
</table>

5.4.5.8. `data_sink_set_enable()`

Table 157. `data_sink_set_enable()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Value of the ENABLE bit.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the value of the ENABLE bit.</td>
</tr>
</tbody>
</table>

5.4.5.9. `data_sink_get_throttle()`

Table 158. `data_sink_get_throttle()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>Throttle value.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the throttle value.</td>
</tr>
</tbody>
</table>
5.4.5.10. data_sink_set_throttle()

Table 159. data_sink_set_throttle()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>void data_sink_set_throttle(alt_u32 base, alt_u32 value);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include:</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave. value—Throttle value.</td>
</tr>
<tr>
<td>Returns</td>
<td>void</td>
</tr>
<tr>
<td>Description</td>
<td>Sets the throttle value, which can be between 0–256 inclusively. The throttle value, when divided by 256 yields the rate at which the Avalon Data Pattern Checker IP receives data.</td>
</tr>
</tbody>
</table>

5.4.5.11. data_sink_get_packet_count()

Table 160. data_sink_get_packet_count()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_get_packet_count(alt_u32 base, alt_u32 channel);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave. channel—Channel number.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of data packets received on the channel.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of data packets received on a channel.</td>
</tr>
</tbody>
</table>

5.4.5.12. data_sink_get_error_count()

Table 161. data_sink_get_error_count()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_get_error_count(alt_u32 base, alt_u32 channel);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave. channel—Channel number.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of errors received on the channel.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of errors received on a channel.</td>
</tr>
</tbody>
</table>
5.4.5.13. data_sink_get_symbol_count()

Table 162. data_sink_get_symbol_count()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_sink_get_symbol_count(alt_u32 base, alt_u32 channel);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>No</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave. channel—Channel number.</td>
</tr>
<tr>
<td>Returns</td>
<td>Number of symbols received on the channel.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the number of symbols received on a channel.</td>
</tr>
</tbody>
</table>

5.4.5.14. data_sink_get_exception()

Table 163. data_sink_get_exception()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_sink_get_exception(alt_u32 base);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>base—Base address of the control and status slave.</td>
</tr>
<tr>
<td>Returns</td>
<td>First exception descriptor in the exception FIFO. 0—No exception descriptor found in the exception FIFO.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the first exception descriptor in the exception FIFO and pops it off the FIFO.</td>
</tr>
</tbody>
</table>

5.4.5.15. data_sink_exception_is_exception()

Table 164. data_sink_exception_is_exception()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_sink_exception_is_exception(int exception);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>exception—Exception descriptor</td>
</tr>
<tr>
<td>Returns</td>
<td>1—Indicates an exception. 0—No exception.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if an exception descriptor describes a valid exception.</td>
</tr>
</tbody>
</table>
5.4.5.16. `data_sink_exception_has_data_error()`

Table 165. `data_sink_exception_has_data_error()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_exception_has_data_error(int exception);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>exception—Exception descriptor.</code></td>
</tr>
<tr>
<td>Returns</td>
<td>1—Data has errors. 0—No errors.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if an exception indicates erroneous data.</td>
</tr>
</tbody>
</table>

5.4.5.17. `data_sink_exception_has_missing_sop()`

Table 166. `data_sink_exception_has_missing_sop()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_exception_has_missing_sop(int exception);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>exception—Exception descriptor.</code></td>
</tr>
<tr>
<td>Returns</td>
<td>1—Missing SOP. 0—Other exception types.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if an exception descriptor indicates missing SOP.</td>
</tr>
</tbody>
</table>

5.4.5.18. `data_sink_exception_has_missing_eop()`

Table 167. `data_sink_exception_has_missing_eop()`

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td><code>int data_sink_exception_has_missing_eop(int exception);</code></td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td><code>&lt;data_sink_util.h&gt;</code></td>
</tr>
<tr>
<td>Parameters</td>
<td><code>exception—Exception descriptor.</code></td>
</tr>
<tr>
<td>Returns</td>
<td>1—Missing EOP. 0—Other exception types.</td>
</tr>
<tr>
<td>Description</td>
<td>Checks if an exception descriptor indicates missing EOP.</td>
</tr>
</tbody>
</table>
5.4.5.19. data_sink_exception_signalled_error()

Table 168. data_sink_exception_signalled_error()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_sink_exception_signalled_error(int exception);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>exception—Exception descriptor.</td>
</tr>
<tr>
<td>Returns</td>
<td>Signal error value.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the value of the signaled error from the exception.</td>
</tr>
</tbody>
</table>

5.4.5.20. data_sink_exception_channel()

Table 169. data_sink_exception_channel()

<table>
<thead>
<tr>
<th>Information Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype</td>
<td>int data_sink_exception_channel(int exception);</td>
</tr>
<tr>
<td>Thread-safe</td>
<td>Yes</td>
</tr>
<tr>
<td>Include</td>
<td>&lt;data_sink_util.h&gt;</td>
</tr>
<tr>
<td>Parameters</td>
<td>exception—Exception descriptor.</td>
</tr>
<tr>
<td>Returns</td>
<td>Channel number on which an exception occurred.</td>
</tr>
<tr>
<td>Description</td>
<td>Retrieves the channel number on which an exception occurred.</td>
</tr>
</tbody>
</table>

5.5. Avalon Streaming Splitter Intel FPGA IP

The Avalon Streaming Splitter Intel FPGA IP allows you to replicate transactions from an Avalon streaming sink interface to multiple Avalon streaming source interfaces. This IP supports from 1 to 16 outputs.

Figure 197. Avalon Streaming Splitter Intel FPGA IP
The Avalon Streaming Splitter IP copies input signals from the input interface to the corresponding output signals of each output interface without altering the size or functionality. This includes all signals except for the ready signal. The IP includes a clock signal to determine the Avalon streaming interface and clock domain where the IP resides. Because the Avalon Streaming Splitter IP does not use the clock signal internally, latency is not introduced when using this IP.

5.5.1. Avalon Streaming Splitter Intel FPGA IP Backpressure

The Avalon Streaming Splitter Intel FPGA IP integrates with backpressure by AND-ing the ready signals from the output interfaces and sending the result to the input interface. As a result, if an output interface deasserts the ready signal, the input interface receives the deasserted ready signal, as well. This functionality ensures that backpressure on the output interfaces is propagated to the input interface.

When the **Qualify Valid Out** option is enabled, the out_valid signals on all other output interfaces are gated when backpressure is applied from one output interface. In this case, when any output interface deasserts its ready signal, the out_valid signals on the other output interfaces are also deasserted.

When the **Qualify Valid Out** option is disabled, the output interfaces have a non-gated out_valid signal when backpressure is applied. In this case, when an output interface deasserts its ready signal, the out_valid signals on the other output interfaces are not affected.

Because the logic is combinational, the Intel FPGA IP introduces no latency.

5.5.2. Avalon Streaming Splitter Intel FPGA IP Interfaces

The Avalon Streaming Splitter Intel FPGA IP supports streaming data, with optional packet, channel, and error signals. The Intel FPGA IP propagates backpressure from any output interface to the input interface.

**Table 170. Avalon Streaming Splitter Intel FPGA IP Support**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backpressure</td>
<td>Ready latency = 0.</td>
</tr>
<tr>
<td>Data Width</td>
<td>Configurable.</td>
</tr>
<tr>
<td>Channel</td>
<td>Supported (optional).</td>
</tr>
<tr>
<td>Error</td>
<td>Supported (optional).</td>
</tr>
<tr>
<td>Packet</td>
<td>Supported (optional).</td>
</tr>
</tbody>
</table>
### 5.5.3. Avalon Streaming Splitter Intel FPGA IP Parameters

#### Table 171. Avalon Streaming Splitter Intel FPGA IP Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Legal Values</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number Of Outputs</td>
<td>1 to 16</td>
<td>2</td>
<td>The number of output interfaces. Platform Designer supports 1 for some systems where no duplicated output is required.</td>
</tr>
<tr>
<td>Qualify Valid Out</td>
<td>Enabled, Disabled</td>
<td>Enabled</td>
<td>If enabled, the out_valid signal of all output interfaces is gated when back pressure is applied.</td>
</tr>
<tr>
<td>Data Width</td>
<td>1–512</td>
<td>8</td>
<td>The width of the data on the Avalon streaming data interfaces.</td>
</tr>
<tr>
<td>Bits Per Symbol</td>
<td>1–512</td>
<td>8</td>
<td>The number of bits per symbol for the input and output interfaces. For example, byte-oriented interfaces have 8-bit symbols.</td>
</tr>
<tr>
<td>Use Packets</td>
<td>Enabled, Disabled</td>
<td>Disabled</td>
<td>Enable support of data packet transfers. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
</tr>
<tr>
<td>Use Channel</td>
<td>Enabled, Disabled</td>
<td>Disabled</td>
<td>Enable the channel signal.</td>
</tr>
<tr>
<td>Channel Width</td>
<td>0–8</td>
<td>1</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is set to 0.</td>
</tr>
<tr>
<td>Max Channels</td>
<td>0–255</td>
<td>1</td>
<td>The maximum number of channels that a data interface can support. This parameter is disabled when Use Channel is set to 0.</td>
</tr>
<tr>
<td>Use Error</td>
<td>Enabled, Disabled</td>
<td>Disabled</td>
<td>Enable the error signal.</td>
</tr>
<tr>
<td>Error Width</td>
<td>0–31</td>
<td>1</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the IP is not using the error signal. This parameter is disabled when Use Error is set to 0.</td>
</tr>
</tbody>
</table>

### 5.6. Avalon Streaming Delay Intel FPGA IP

The Avalon Streaming Delay Intel FPGA IP provides a solution to delay Avalon streaming transactions by a constant number of clock cycles. This IP supports up to 16 clock cycle delays.
The Avalon Streaming Delay Intel FPGA IP adds a delay between the input and output interfaces. The IP accepts transactions presented on the input interface and reproduces them on the output interface $N$ cycles later without changing the transaction.

The input interface delays the input signals by a constant $N$ number of clock cycles to the corresponding output signals of the output interface. The **Number Of Delay Clocks** parameter defines the constant $N$, which must be from 0 to 16. The change of the `in_valid` signal is reflected on the `out_valid` signal exactly $N$ cycles later.

### 5.6.1. Avalon Streaming Delay Intel FPGA IP Reset Signal

The Avalon Streaming Delay Intel FPGA IP has a `reset` signal that is synchronous to the `clk` signal. When the IP asserts the `reset` signal, the output signals are held at 0. After the `reset` signal is deasserted, the output signals are held at 0 for $N$ clock cycles. The delayed values of the input signals are then reflected at the output signals after $N$ clock cycles.

### 5.6.2. Avalon Streaming Delay Intel FPGA IP Interfaces

The Avalon Streaming Delay Intel FPGA IP supports streaming data, with optional packet, channel, and error signals. The Avalon Streaming Delay Intel FPGA IP does not support backpressure.

### Table 172. Avalon Streaming Delay Intel FPGA IP Support

<table>
<thead>
<tr>
<th>Feature</th>
<th>Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backpressure</td>
<td>Not supported.</td>
</tr>
<tr>
<td>Data Width</td>
<td>Configurable.</td>
</tr>
<tr>
<td>Channel</td>
<td>Supported (optional).</td>
</tr>
<tr>
<td>Error</td>
<td>Supported (optional).</td>
</tr>
<tr>
<td>Packet</td>
<td>Supported (optional).</td>
</tr>
</tbody>
</table>
5.6.3. Avalon Streaming Delay Intel FPGA IP Parameters

Table 173. Avalon Streaming Delay Intel FPGA IP Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Legal Values</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number Of Delay Clocks</td>
<td>0 to 16</td>
<td>1</td>
<td>Specifies the delay the IP introduces, in clock cycles. Platform Designer supports 0 for some systems where no delay is required.</td>
</tr>
<tr>
<td>Data Width</td>
<td>1–512</td>
<td>8</td>
<td>The width of the data on the Avalon streaming data interfaces.</td>
</tr>
<tr>
<td>Bits Per Symbol</td>
<td>1–512</td>
<td>8</td>
<td>The number of bits per symbol for the input and output interfaces. For example, byte-oriented interfaces have 8-bit symbols.</td>
</tr>
<tr>
<td>Use Packets</td>
<td>0 or 1</td>
<td>0</td>
<td>Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.</td>
</tr>
<tr>
<td>Use Channel</td>
<td>0 or 1</td>
<td>0</td>
<td>The option to enable or disable the channel signal.</td>
</tr>
<tr>
<td>Channel Width</td>
<td>0–8</td>
<td>1</td>
<td>The width of the channel signal on the data interfaces. This parameter is disabled when Use Channel is set to 0.</td>
</tr>
<tr>
<td>Max Channels</td>
<td>0–255</td>
<td>1</td>
<td>The maximum number of channels that a data interface can support. This parameter is disabled when Use Channel is set to 0.</td>
</tr>
<tr>
<td>Use Error</td>
<td>0 or 1</td>
<td>0</td>
<td>The option to enable or disable the error signal.</td>
</tr>
<tr>
<td>Error Width</td>
<td>0–31</td>
<td>1</td>
<td>The width of the error signal on the output interfaces. A value of 0 indicates that the error signal is not in use. This parameter is disabled when Use Error is set to 0.</td>
</tr>
</tbody>
</table>

5.7. Avalon Streaming Round Robin Scheduler Intel FPGA IP

The Avalon Streaming Round Robin Scheduler Intel FPGA IP controls the read operations from a multi-channel Avalon streaming component that buffers data by channels. The IP reads the almost-full threshold values from the multiple channels in the multi-channel component, and then issues the read request to the Avalon streaming source according to a round-robin scheduling algorithm.

Figure 199. Avalon Streaming Round Robin Scheduler Intel FPGA IP

![Avalon Streaming Round Robin Scheduler Intel FPGA IP diagram](image-url)
In a multi-channel component, the IP can store data either in the sequence that it comes in (FIFO), or in segments according to the channel. When data is stored in segments according to channels, a scheduler is needed to schedule the read operations.

### 5.7.1. Avalon Streaming Round Robin Scheduler IP Almost-Full Status Interface

The Almost-Full Status interface is an Avalon streaming sink interface that collects the almost-full status from the sink components for the channels in the sequence provided.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Property</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backpressure</td>
<td>Not supported</td>
</tr>
<tr>
<td>Data Width</td>
<td>Data width = 1; Bits per symbol = 1</td>
</tr>
<tr>
<td>Channel</td>
<td>Maximum channel = 32; Channel width = 5</td>
</tr>
<tr>
<td>Error</td>
<td>Not supported</td>
</tr>
<tr>
<td>Packet</td>
<td>Not supported</td>
</tr>
</tbody>
</table>

### 5.7.2. Avalon Streaming Round Robin Scheduler IP Request Interface

The Request Interface is an Avalon memory mapped write master interface that requests data from a specific channel. The Avalon Streaming Round Robin Scheduler cycles through the channels it supports and schedules data to be read.

### 5.7.3. Avalon Streaming Round Robin Scheduler IP Operation

If a particular channel is almost full, the Avalon Streaming Round Robin Scheduler does not schedule data to be read from that channel in the source component.

The scheduler only requests 1 bit of data from a channel at each transaction. To request 1 bit of data from channel \( n \), the scheduler writes the value 1 to address \( 4 \times n \). For example, if the scheduler is requesting data from channel 3, the scheduler writes 1 to address 0xC. At every clock cycle, the scheduler requests data from the next channel. Therefore, if the scheduler starts requesting from channel 1, at the next clock cycle, it requests from channel 2. The scheduler does not request data from a particular channel if the almost-full status for the channel is asserted. In this case, the scheduler uses one clock cycle without a request transaction.

The Avalon Streaming Round Robin Scheduler cannot determine if the requested component is able to service the request transaction. The component asserts \( \text{waitrequest} \) when it cannot accept new requests.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td>In</td>
<td>Clock reference.</td>
</tr>
</tbody>
</table>

Table 175. Avalon Streaming Round Robin Scheduler Ports
### Signal Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>reset_n</td>
<td>In</td>
<td>Asynchronous active low reset.</td>
</tr>
</tbody>
</table>

#### Avalon Memory Mapped Request Interface

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>request_address</td>
<td>Out</td>
<td>The write address that indicates which channel has the request.</td>
</tr>
<tr>
<td>request_write</td>
<td>Out</td>
<td>Write enable signal.</td>
</tr>
<tr>
<td>request_writedata</td>
<td>Out</td>
<td>The amount of data requested from the particular channel.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This value is always fixed at 1.</td>
</tr>
<tr>
<td>request_waitrequest</td>
<td>In</td>
<td>Wait request signal that pauses the scheduler when the slave cannot accept a new request.</td>
</tr>
</tbody>
</table>

#### Avalon Streaming Almost-Full Status Interface

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>almost_full_valid</td>
<td>In</td>
<td>Indicates that almost_full_channel and almost_full_data are valid.</td>
</tr>
<tr>
<td>almost_full_channel</td>
<td>In</td>
<td>Indicates the channel for the current status indication.</td>
</tr>
<tr>
<td>almost_full_data</td>
<td>In</td>
<td>A 1-bit signal that is asserted high to indicate that the channel indicated by almost_full_channel is almost full.</td>
</tr>
</tbody>
</table>

#### 5.7.4. Avalon Streaming Round Robin Scheduler IP Parameters

**Table 176. Avalon Streaming Round Robin Scheduler IP Parameters**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Legal Values</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of channels</td>
<td>2–32</td>
<td>2</td>
<td>Specifies the number of channels the Avalon Streaming Round Robin Scheduler supports.</td>
</tr>
<tr>
<td>Use almost-full status</td>
<td>Enabled, Disabled</td>
<td>Disabled</td>
<td>If enabled, the scheduler uses the almost-full interface. If not, the IP requests data from the next channel at the next clock cycle.</td>
</tr>
</tbody>
</table>

#### 5.8. Avalon Packets to Transactions Converter Intel FPGA IP

The Avalon Packets to Transactions Converter Intel FPGA IP receives streaming data from upstream components and initiates Avalon memory mapped transactions. The IP then returns Avalon memory mapped transaction responses to the requesting components.
Figure 200. Avalon Packets to Transactions Converter Intel FPGA IP

Note: The SPI Slave to Avalon Master Bridge, and the JTAG to Avalon Master Bridge, are examples of the Packets to Transactions Converter IP. For more information, refer to the Avalon Interface Specifications.

Related Information
Avalon Interface Specifications

5.8.1. Avalon Packets to Transactions Converter IP Interfaces

Table 177. Properties of Avalon Streaming Interfaces

<table>
<thead>
<tr>
<th>Feature</th>
<th>Property</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backpressure</td>
<td>Ready latency = 0.</td>
</tr>
<tr>
<td>Data Width</td>
<td>Data width = 8 bits; Bits per symbol = 8.</td>
</tr>
<tr>
<td>Channel</td>
<td>Not supported.</td>
</tr>
<tr>
<td>Error</td>
<td>Not used.</td>
</tr>
<tr>
<td>Packet</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

The Avalon memory mapped master interface supports read and write transactions. The data width is set to 32 bits, and burst transactions are not supported.

5.8.2. Avalon Packets to Transactions Converter IP Operation

The Avalon Packets to Transactions Converter IP receives streams of packets on its Avalon streaming sink interface and initiates Avalon memory mapped transactions. Upon receiving transaction responses from Avalon memory mapped slaves, the IP transforms the responses to packets and returns them to the requesting components via its Avalon streaming source interface. The IP does not report Avalon streaming errors.
5.8.2.1. Avalon Packets to Transactions Converter IP Data Packet Formats

A response packet is returned for every write transaction. The IP also returns a response packet if a no transaction (0x7f) is received. An invalid transaction code is regarded as a no transaction. For read transactions, the IP returns the data read.

The Avalon Packets to Transactions Converter IP expects incoming data streams to be in the formats shown in the table below.

Table 178. Data Packet Formats

<table>
<thead>
<tr>
<th>Byte</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Transaction code</td>
<td>Type of transaction.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>[3:2]</td>
<td>Size</td>
<td>Transaction size in bytes. For write transactions, the size indicates the size of the data field. For read transactions, the size indicates the total number of bytes to read.</td>
</tr>
<tr>
<td>[n:8]</td>
<td>Data</td>
<td>Transaction data; data to be written for write transactions.</td>
</tr>
</tbody>
</table>

Response Packet Format

<table>
<thead>
<tr>
<th>Byte</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Transaction code</td>
<td>The transaction code with the most significant bit inverted.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>[4:2]</td>
<td>Size</td>
<td>Total number of bytes read/written successfully.</td>
</tr>
</tbody>
</table>

Related Information
Avalon Packets to Transactions Converter IP Interfaces on page 361

5.8.2.2. Avalon Packets to Transactions Converter IP Supported Transactions

The Avalon Packets to Transactions Converter IP supports the following Avalon memory mapped transactions:

Table 179. Avalon Packets to Transactions Converter IP Supported Transactions

<table>
<thead>
<tr>
<th>Transaction Code</th>
<th>Avalon Memory Mapped Transaction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Write, non-incrementing address.</td>
<td>Writes data to the address until the total number of bytes written to the same word address equals to the value specified in the size field.</td>
</tr>
<tr>
<td>0x04</td>
<td>Write, incrementing address.</td>
<td>Writes transaction data starting at the current address.</td>
</tr>
<tr>
<td>0x10</td>
<td>Read, non-incrementing address.</td>
<td>Reads 32 bits of data from the address until the total number of bytes read from the same address equals to the value specified in the size field.</td>
</tr>
<tr>
<td>0x14</td>
<td>Read, incrementing address.</td>
<td>Reads the number of bytes specified in the size parameter starting from the current address.</td>
</tr>
<tr>
<td>0x7f</td>
<td>No transaction.</td>
<td>No transaction is initiated. You can use this transaction type for testing purposes. Although no transaction is initiated on the Avalon memory mapped interface, the IP still returns a response packet for this transaction code.</td>
</tr>
</tbody>
</table>
The Avalon Packets to Transactions Converter IP can process only a single transaction at a time. The ready signal on the IP Avalon streaming sink interface is asserted only when the current transaction is completely processed.

No internal buffer is implemented on the datapaths. Data received on the Avalon streaming interface is forwarded directly to the Avalon memory mapped interface and vice-versa. Asserting the waitrequest signal on the Avalon memory mapped interface backpressures the Avalon streaming sink interface. In the opposite direction, if the Avalon streaming source interface is back pressured, the read signal on the Avalon memory mapped interface is not asserted until the backpressure is alleviated. Backpressuring the Avalon streaming source in the middle of a read can result in data loss. In this cases, the IP returns the data that is successfully received.

A transaction is considered complete when the IP receives an EOP. For write transactions, the actual data size is expected to be the same as the value of the size property. Whether or not both values agree, the IP always uses the end of packet (EOP) to determine the end of data.

### 5.8.2.3. Avalon Packets to Transactions IP Converter Malformed Packets

The following are examples of malformed packets:

- **Consecutive start of packet (SOP)**—An SOP marks the beginning of a transaction. If an SOP is received in the middle of a transaction, the IP drops the current transaction without returning a response packet for the transaction, and initiates a new transaction. This effectively processes packets without an end of packet (EOP).

- **Unsupported transaction codes**—The IP processes unsupported transactions as a no transaction.

### 5.9. Avalon Streaming Pipeline Stage Intel FPGA IP

The Avalon Streaming Pipeline Stage Intel FPGA IP receives data from an Avalon streaming source interface, and outputs the data to an Avalon streaming sink interface. In the absence of back pressure, the Avalon Streaming Pipeline Stage Intel FPGA IP source interface outputs data one cycle after receiving the data on its sink interface.

If the pipeline stage receives back pressure on its source interface, the pipeline stage continues to assert its source interface's current data output. While the pipeline stage is receiving back pressure on its source interface, and then receives new data on its sink interface, the pipeline stage internally buffers the new data. It then asserts back pressure on its sink interface.

After the backpressure is deasserted, the pipeline stage's source interface is deasserted and the pipeline stage asserts internally buffered data (if present). Additionally, the pipeline stage deasserts back pressure on its sink interface.
**Figure 201. Pipeline Stage Simple Register**
If the ready signal is not pipelined, the pipeline stage becomes a simple register.

![Simple Register Diagram](image)

**Figure 202. Pipeline Stage Holding Register**
If the ready signal is pipelined, the pipeline stage must also include a second “holding” register.

![Holding Register Diagram](image)

### 5.10. Avalon Streaming Multiplexer and Demultiplexer Intel FPGA IP

The Avalon Streaming Multiplexer Intel FPGA IP receives data from various input interfaces and multiplexes the data into a single output interface, using the optional channel signal to indicate the origin of the data. The Avalon Streaming Multiplexer Intel FPGA IP receives data from a channelized input interface and drives that data to multiple output interfaces, where the output interface is selected by the input channel signal.

The Multiplexer and Demultiplexer IPs can transfer data between interfaces on that supports a unidirectional flow of data. The Multiplexer and Demultiplexer IP allow you to create multiplexed or demultiplexed datapaths without having to write custom HDL code. The Multiplexer IP includes an Avalon Streaming Round Robin Scheduler.

**Related Information**
Avalon Streaming Round Robin Scheduler Intel FPGA IP on page 358
5.10.1. Avalon Streaming Multiplexer and Demultiplexer Software Programming Model

The Multiplexer and Demultiplexer IP components do not have any user-visible control or status registers. Therefore, Platform Designer cannot control or configure any aspect of the Multiplexer or Demultiplexer at run-time. These IP components cannot generate interrupts.

5.10.2. Avalon Streaming Multiplexer Intel FPGA IP

The Avalon Streaming Multiplexer Intel FPGA IP takes data from a variety of input data interfaces, and multiplexes the data onto a single output interface. The multiplexer includes a round-robin scheduler that selects from the next input interface that has data. Each input interface has the same width as the output interface, so that the other input interfaces are backpressured when the multiplexer is carrying data from a different input interface.

Figure 203. Avalon Streaming Multiplexer Intel FPGA IP

The multiplexer includes an optional channel signal that enables each input interface to carry channelized data. The output interface channel width is equal to:

\[(\log_2 (n-1)) + 1 + w\]

where \(n\) is the number of input interfaces, and \(w\) is the channel width of each input interface. All input interfaces must have the same channel width. These bits are appended to either the most or least significant bits of the output channel signal.

The scheduler processes one input interface at a time, selecting it for transfer. Once an input interface has been selected, data from that input interface is sent until one of the following scenarios occurs:

- The specified number of cycles have elapsed.
- The input interface has no more data to send and the valid signal is deasserted on a ready cycle.
- When packets are supported, endofpacket is asserted.
5.10.2.1. Avalon Streaming Multiplexer IP Input Interfaces

Each input interface is an Avalon streaming data interface that optionally supports packets. The input interfaces are identical; they have the same symbol and data widths, error widths, and channel widths.

5.10.2.2. Avalon Multiplexer IP Output Interface

The output interface carries the multiplexed data stream with data from the inputs. The symbol, data, and error widths are the same as the input interfaces.

The width of the channel signal is the same as the input interfaces, with the addition of the bits needed to indicate the origin of the data.

You can configure the following parameters for the output interface:

- **Data Bits Per Symbol**—the bits per symbol is related to the width of `readdata` and `writedata` signals, which must be a multiple of the bits per symbol.
- **Data Symbols Per Beat**—the number of symbols (words) that are transferred per beat (transfer). Valid values are 1 to 32.
- **Include Packet Support**—indicates whether packet transfers are supported. Packet support includes the `startofpacket`, `endofpacket`, and `empty` signals.
- **Channel Signal Width (bits)**—the number of bits Platform Designer uses for the channel signal for output interfaces. For example, set this parameter to 1 if you have two input interfaces with no channel, or set this parameter to 2 if you have two input interfaces with a channel width of 1 bit. The input channel can have a width between 0-31 bits.
- **Error Signal Width (bits)**—the width of the error signal for input and output interfaces. A value of 0 means the error signal is not in use.

*Note:* If you change only bits per symbol, and do not change the data width, errors are generated.

5.10.2.3. Avalon Multiplexer IP Parameters

You can configure the following parameters for the multiplexer:

- **Number of Input Ports**—the number of input interfaces that the multiplexer supports. Valid values are 2 to 16.
- **Scheduling Size (Cycles)**—the number of cycles that are sent from a single channel before changing to the next channel.
- **Use Packet Scheduling**—when this parameter is turned on, the multiplexer only switches the selected input interface on packet boundaries. Therefore, packets on the output interface are not interleaved.
- **Use high bits to indicate source port**—when this parameter is turned on, the multiplexer uses the high bits of the output channel signal to indicate the origin of the input interface of the data. For example, if the input interfaces have 4-bit channel signals, and the multiplexer has 4 input interfaces, the output interface has a 6-bit channel signal. If this parameter is turned on, bits [5:4] of the output channel signal indicate origin of the input interface of the data, and bits [3:0] are the channel bits that were presented at the input interface.
5.10.3. Avalon Streaming Demultiplexer Intel FPGA IP

The Avalon Streaming Demultiplexer Intel FPGA IP takes data from a channelized input data interface and provides that data to multiple output interfaces, where the output interface selected for a particular transfer is specified by the input channel signal.

**Figure 204. Avalon Streaming Demultiplexer**

The data is delivered to the output interfaces in the same order it is received at the input interface, regardless of the value of channel, packet, frame, or any other signal. Each of the output interfaces has the same width as the input interface; each output interface is idle when the demultiplexer is driving data to a different output interface. The demultiplexer uses \( \log_2(\text{num_output_interfaces}) \) bits of the channel signal to select the output for the data; the remainder of the channel bits are forwarded to the appropriate output interface unchanged.

5.10.3.1. Avalon Streaming Demultiplexer IP Input Interface

Each input interface is an Avalon streaming data interface that optionally supports packets. You can configure the following parameters for the input interface:

- **Data Bits Per Symbol**—The bits per symbol is related to the width of readdata and writedata signals, which must be a multiple of the bits per symbol.
- **Data Symbols Per Beat**—The number of symbols (words) that are transferred per beat (transfer). Valid values are 1 to 32.
- **Include Packet Support**—Indicates whether data packet transfers are supported. Packet support includes the startofpacket, endofpacket, and empty signals.
- **Channel Signal Width (bits)**—The number of bits for the channel signal for output interfaces. A value of 0 means that output interfaces do not use the optional channel signal.
- **Error Signal Width (bits)**—The width of the error signal for input and output interfaces. A value of 0 means the error signal is in use.

*Note:* If you change only bits per symbol, and do not change the data width, errors are generated.
5.10.3.2. Avalon Streaming Demultiplexer IP Output Interface

Each output interface carries data from a subset of channels from the input interface. Each output interface is identical; all have the same symbol and data widths, error widths, and channel widths. The symbol, data, and error widths are the same as the input interface. The width of the channel signal is the same as the input interface, without the bits that the demultiplexer uses to select the output interface.

5.10.3.3. Avalon Streaming Demultiplexer IP Parameters

You can configure the following parameters for the demultiplexer:

- **Number of Output Ports**—The number of output interfaces that the multiplexer supports. Valid values are 2 to 16.
- **High channel bits select output**—When this option is turned on, the demultiplexing function uses the high bits of the input channel signal, and the low order bits are passed to the output. When this option is turned off, the demultiplexing function uses the low order bits, and the high order bits are passed to the output.

Where you place the signals in your design affects the functionality; for example, there is one input interface and two output interfaces. If the low-order bits of the channel signal select the output interfaces, the even channels go to channel 0, and the odd channels go to channel 1. If the high-order bits of the channel signal select the output interface, channels 0 to 7 go to channel 0 and channels 8 to 15 go to channel 1.

Figure 205. Select Bits for the Demultiplexer

5.11. Avalon Streaming Single-Clock and Dual-Clock FIFO Intel FPGA IP

The Avalon Streaming Single-Clock and Avalon Streaming Dual-Clock FIFO Intel FPGA IP are FIFO buffers which operate with a common clock and independent clocks for input and output ports respectively.
5.11.1. Interfaces Implemented in FIFO Cores

The following interfaces are implemented in FIFO Intel FPGA IP:

Avalon Streaming Data Interface on page 370
Avalon Memory Mapped Control and Status Register Interface on page 370
Avalon Streaming Status Interface on page 370

5.11.1.1. Avalon Streaming Data Interface

Each FIFO IP has an Avalon Streaming data sink and source interface. The data sink and source interfaces in the dual-clock FIFO IP are driven by different clocks.

Table 180. Avalon Streaming Interfaces Properties

<table>
<thead>
<tr>
<th>Feature</th>
<th>Property</th>
</tr>
</thead>
<tbody>
<tr>
<td>Backpressure</td>
<td>Ready latency = 0.</td>
</tr>
<tr>
<td>Data Width</td>
<td>Configurable.</td>
</tr>
<tr>
<td>Channel</td>
<td>Supported, up to 255 channels.</td>
</tr>
<tr>
<td>Error</td>
<td>Configurable.</td>
</tr>
<tr>
<td>Packet</td>
<td>Configurable.</td>
</tr>
</tbody>
</table>

5.11.1.2. Avalon Memory Mapped Control and Status Register Interface

You can configure the single-clock FIFO IP to include an optional Avalon memory mapped interface, and the dual-clock FIFO IP to include an Avalon memory mapped interface in each clock domain. The Avalon memory mapped interface provides access to 32-bit registers, which allows you to retrieve the FIFO buffer fill level and configure the almost-empty and almost-full thresholds. In the single-clock FIFO IP, you can also configure the packet and error handling modes.

5.11.1.3. Avalon Streaming Status Interface

The single-clock FIFO IP has two optional Avalon streaming status source interfaces from which you can obtain the FIFO buffer almost-full and almost empty statuses.

5.11.2. Avalon Streaming FIFO IP Operating Modes

- **Default mode**—The IP accepts incoming data on the `in` interface (Avalon streaming data sink) and forwards it to the `out` interface (Avalon streaming data source). The IP asserts the `valid` signal on the Avalon streaming source interface to indicate that data is available at the interface.

- **Store and forward mode**—this mode applies only to the single-clock FIFO IP. The IP asserts the `valid` signal on the `out` interface only when a full packet of data is available at the interface. In this mode, you can also enable the drop-on-error feature by setting the `drop_on_error` register to 1. When this feature is enabled, the IP drops all packets received with the `in_error` signal asserted.

- **Cut-through mode**—this mode applies only to the single-clock FIFO IP. The IP asserts the `valid` signal on the `out` interface to indicate that data is available for consumption when the number of entries specified in the `cut_through_threshold` register are available in the FIFO buffer.

**Note:** To turn on **Cut-through mode**, the **Use store and forward** parameter must be set to 0. Turning on **Use store and forward mode** prompts the user to turn on **Use fill level**, and then the CSR appears.
5.11.3. Avalon Streaming FIFO IP Buffer Fill Level

You can obtain the fill level of the Avalon Streaming FIFO IP buffer via the optional Avalon memory mapped control and status interface. Turn on the Use fill level parameter (Use sink fill level and Use source fill level in the Avalon Streaming Dual-Clock FIFO IP) and read the fill_level register.

The Avalon Streaming Dual-Clock FIFO IP has two fill levels, one in each clock domain. Due to the latency of the clock crossing logic, the fill levels reported in the input and output clock domains may be different for any instance. In both cases, the fill level may report badly for the clock domain; that is, the fill level is reported high in the input clock domain, and low in the output clock domain.

The Avalon Streaming Dual-Clock FIFO IP has an output pipeline stage to improve fMAX. This output stage is accounted for when calculating the output fill level, but not when calculating the input fill level. Therefore, the best measure of the amount of data in the FIFO is by the fill level in the output clock domain. The fill level in the input clock domain represents the amount of space available in the FIFO (available space = FIFO depth - input fill level).

5.11.4. Almost-Full and Almost-Empty Thresholds to Prevent Overflow and Underflow

You can use almost-full and almost-empty thresholds as a mechanism to prevent FIFO IP overflow and underflow. This feature is available only in the Avalon Streaming Single-Clock FIFO IP. To use the thresholds, turn on the Use fill level, Use almost-full status, and Use almost-empty status parameters. You can access the almost_full_threshold and almost_empty_threshold registers via the csr interface and set the registers to an optimal value for your application.

You can obtain the almost-full and almost-empty statuses from almost_full and almost_empty interfaces (Avalon streaming status source). The IP asserts the almost_full signal when the fill level is equal to or higher than the almost-full threshold. Likewise, the IP asserts the almost_empty signal when the fill level is equal to or lower than the almost-empty threshold.

5.11.5. Avalon Streaming Single-Clock and Dual-Clock FIFO IP Parameters

Table 181. Avalon Streaming Single-Clock and Dual-Clock FIFO IP Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Legal Values</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits per symbol</td>
<td>1–32</td>
<td>These parameters determine the width of the FIFO.</td>
</tr>
<tr>
<td>Symbols per beat</td>
<td>1–32</td>
<td>FIFO width = Bits per symbol * Symbols per beat, where: Bits per symbol is the number of bits in a symbol, and Symbols per beat is the number of symbols transferred in a beat.</td>
</tr>
<tr>
<td>Error width</td>
<td>0–32</td>
<td>The width of the error signal.</td>
</tr>
<tr>
<td>FIFO depth</td>
<td>2^n</td>
<td>The FIFO depth. An output pipeline stage is added to the FIFO to increase performance, which increases the FIFO depth by one. (&lt;n&gt; = n=1,2,3,4 and so on.)</td>
</tr>
<tr>
<td>Use packets</td>
<td>—</td>
<td>Turn on this parameter to enable data packet support on the Avalon streaming data interfaces.</td>
</tr>
</tbody>
</table>

continued...
### Parameter Legal Values Description

**Channel width**

1–32

The width of the channel signal.

**Avalon Streaming Single Clock FIFO Only**

**Use fill level**

—

Turn on this parameter to include the Avalon memory mapped control and status register interface (CSR). The CSR is enabled when **Use fill level** is set to 1.

**Use Store and Forward**

To turn on **Cut-through mode, Use store and forward** must be set to 0. Turning on **Use store and forward** prompts the user to turn on **Use fill level**, and then the CSR appears.

**Avalon Streaming Dual Clock FIFO Only**

**Use sink fill level**

—

Turn on this parameter to include the Avalon memory mapped control and status register interface in the input clock domain.

**Use source fill level**

—

Turn on this parameter to include the Avalon memory mapped control and status register interface in the output clock domain.

**Write pointer synchronizer length**

2–8

The length of the write pointer synchronizer chain. Setting this parameter to a higher value leads to better metastability while increasing the latency of the IP.

**Read pointer synchronizer length**

2–8

The length of the read pointer synchronizer chain. Setting this parameter to a higher value leads to better metastability.

**Use Max Channel**

—

Turn on this parameter to specify the maximum channel number.

**Max Channel**

1–255

Maximum channel number.

**Note:** For more information about metastability in Intel devices, refer to *Understanding Metastability in FPGAs*. For more information about metastability analysis and synchronization register chains, refer to the *Managing Metastability*.

**Related Information**

- Managing Metastability with the Software
- Understanding Metastability in FPGAs

### 5.11.6. Avalon Streaming Single-Clock FIFO IP Registers

**Table 182. Avalon Streaming Single-Clock FIFO IP Registers**

The CSR interface in the Avalon Streaming Single Clock FIFO IP provides access to registers.

<table>
<thead>
<tr>
<th>32-Bit Word Offset</th>
<th>Name</th>
<th>Access</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>fill_level</td>
<td>R</td>
<td>0</td>
<td>24-bit FIFO fill level. Bits 24 to 31 are not used.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
<td>Reserved for future use.</td>
</tr>
<tr>
<td>2</td>
<td>almost_full_threshold</td>
<td>RW</td>
<td>FIFO depth – 1</td>
<td>Set this register to a value that indicates the FIFO buffer is getting full.</td>
</tr>
</tbody>
</table>

*continued...*
### Table 183. Register Description for Avalon Streaming Dual-Clock FIFO

The in_csr and out_csr interfaces in the Avalon Streaming Dual Clock FIFO IP reports the FIFO fill level.

<table>
<thead>
<tr>
<th>32-Bit Word Offset</th>
<th>Name</th>
<th>Access</th>
<th>Reset Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>fill_level</td>
<td>R</td>
<td>0</td>
<td>24-bit FIFO fill level. Bits 24 to 31 are not used.</td>
</tr>
</tbody>
</table>

#### Related Information
- Avalon Memory-Mapped Design Optimizations
- Avalon Interface Specifications

### 5.12. Platform Designer System Design Components Revision History

The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019.11.11</td>
<td>19.1.0</td>
<td>Updated the names of Intel FPGA IP components throughout.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated name of Test Pattern Checker IP to Avalon Data Pattern Checker IP throughout.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Address Span Extender figure bit order.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Provided directory path in Test Pattern Generator</td>
</tr>
<tr>
<td>2018.12.15</td>
<td>18.1.0</td>
<td>Replaced references to System Contents tab with new System View tab.</td>
</tr>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>Changed instances of Qsys Pro to Platform Designer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Changed instances of AXI Default Slave to Error Response Slave.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated topics: Error Response Slave.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Figure: Error Response Slave Parameter Editor.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>• Added Figure: Error Response Slave Parameter Editor with Enabled CSR Support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated topics: CSR Registers and renamed to Error Response Slave CSR Registers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added topic: Error Response Slave Access Violation Service.</td>
</tr>
<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Implemented Intel rebranding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Implemented Qsys rebranding.</td>
</tr>
<tr>
<td>2016.05.03</td>
<td>16.0.0</td>
<td>Updated Address Span Extender</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Address Span Extender register mapping better explained</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Address Span Extender Parameters table added</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Address Span Extender example added</td>
</tr>
<tr>
<td>2015.11.02</td>
<td>15.1.0</td>
<td>Changed instances of Quartus II to Quartus Prime.</td>
</tr>
<tr>
<td>2015.05.04</td>
<td>15.0.0</td>
<td>Avalon Memory Mapped Unaligned Burst Expansion Bridge and Avalon Memory Mapped Pipeline Bridge, <strong>Maximum pending read transactions</strong> parameter. Extended description.</td>
</tr>
<tr>
<td>December 2014</td>
<td>14.1.0</td>
<td>• AXI Timeout Bridge.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added notes to Avalon Memory Mapped Clock Crossing Bridge pertaining to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— SDC constraints for its internal asynchronous FIFOs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— FIFO-based clock crossing.</td>
</tr>
<tr>
<td>June 2014</td>
<td>14.0.0</td>
<td>• AXI Bridge support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Address Span Extender updates.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Avalon Memory Mapped Unaligned Burst Expansion Bridge support.</td>
</tr>
<tr>
<td>November 2013</td>
<td>13.1.0</td>
<td>• Address Span Extender</td>
</tr>
<tr>
<td>May 2013</td>
<td>13.0.0</td>
<td>• Added Streaming Pipeline Stage support.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added AMBA APB support.</td>
</tr>
<tr>
<td>November 2012</td>
<td>12.1.0</td>
<td>• Moved relevant content from the <em>Embedded Peripherals IP User Guide</em>.</td>
</tr>
</tbody>
</table>
6. Platform Designer Command-Line Utilities

You can perform many of the functions available in the Platform Designer GUI at the command-line, with Platform Designer command-line utilities.

You run Platform Designer command-line executables from the Intel Quartus Prime installation directory:

```
<Intel Quartus Prime installation directory>\quartus\sopc_builder \bin
```

For command-line help listing of all the options for any executable, type the following command:

```
<Intel Quartus Prime installation directory>\quartus\sopc_builder \bin\<executable name> --help
```

Note: You must add `$QUARTUS_ROOTDIR/sopc_builder/bin/` to the PATH variable to access command-line utilities. Once you add this PATH variable, you can launch the utility from any directory location.

6.1. Run the Platform Designer Editor with qsys-edit

The `qsys-edit` utility allows you to run the Platform Designer editor from command-line.

You can use the following options with the `qsys-edit` utility:

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>1st arg file</code></td>
<td>Optional</td>
<td>Specifies the name of the .qsys system or .qvar variation file to edit.</td>
</tr>
<tr>
<td><code>--search-path=&lt;value&gt;</code></td>
<td>Optional</td>
<td>If you omit this command, Platform Designer uses a standard default path. If you provide a search path, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$&quot;, for example:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>/extra/dir,$ .</td>
</tr>
<tr>
<td><code>--quartus-project=&lt;value&gt;</code></td>
<td>Required</td>
<td>This option is mandatory if you are associating your Platform Designer system with an existing Intel Quartus Prime project. Specifies the name of the Intel Quartus Prime project file. If you do not provide the revision via <code>--rev</code>, Platform Designer uses the default revision as the Intel Quartus Prime project name.</td>
</tr>
<tr>
<td>Option</td>
<td>Usage</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------</td>
<td>-----------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>--new-quartus-project</td>
<td>Required</td>
<td>This option is mandatory if you are associating your Platform Designer system with a new Intel Quartus Prime project. Specifies the name and path of the new Intel Quartus Prime project. Creates a new Intel Quartus Prime project at the specified path. You can also provide the revision name.</td>
</tr>
<tr>
<td>--rev</td>
<td>Optional</td>
<td>Specifies the name of the Intel Quartus Prime project revision.</td>
</tr>
<tr>
<td>--family</td>
<td>Optional</td>
<td>Sets the device family.</td>
</tr>
<tr>
<td>--part</td>
<td>Optional</td>
<td>Sets the device part number. If set, this option overrides the --family option.</td>
</tr>
<tr>
<td>--new-component-type</td>
<td>Optional</td>
<td>Specifies the instance type for parameterization in a variation.</td>
</tr>
<tr>
<td>--require-generation</td>
<td>Optional</td>
<td>Marks the loading system as requiring generation.</td>
</tr>
<tr>
<td>--debug</td>
<td>Optional</td>
<td>Enables debugging features and output.</td>
</tr>
<tr>
<td>--jvm-max-heap-size</td>
<td>Optional</td>
<td>The maximum memory size that Platform Designer uses when running qsys-edit. You specify this value as &lt;size&gt;&lt;unit&gt;, where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes. The default value is 512m.</td>
</tr>
<tr>
<td>--help</td>
<td>Optional</td>
<td>Displays help for qsys-edit.</td>
</tr>
</tbody>
</table>

**Important:** The options --quartus-project and --new-quartus-project are mutually exclusive. If you use --quartus-project you cannot use --new-quartus-project and vice versa.

**Extended Features with the --debug Options**

The --debug option provides powerful tools for debugging. When you launch Platform Designer with the --debug option enabled, you can:

- View debug messages when opening a system or generating HDL for that system.
- Add the --verbose argument when generating IP or a system using command-line utilities.
- Access internal library components in the IP Catalog, for example, modules used to create interconnect fabric.
- Access to debug tools and files from the **Internal** menu.
**Figure 208. Internal Menu Options**

<table>
<thead>
<tr>
<th>Menu Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Show hw.tcl Debugger</td>
<td>Displays a Tcl debugger.</td>
</tr>
<tr>
<td>Show System File</td>
<td>Displays the current system XML in a text dialog box.</td>
</tr>
<tr>
<td>Show SOPCINFO File</td>
<td>Shows the SOPCINFO report XML in a text dialog box.</td>
</tr>
<tr>
<td>Show UI Properties</td>
<td>Displays the UI properties in a text dialog box.</td>
</tr>
<tr>
<td>Show Command Line Arguments</td>
<td>Displays all command-line arguments and environment variables in a text</td>
</tr>
<tr>
<td></td>
<td>dialog box.</td>
</tr>
<tr>
<td>Show System Changes</td>
<td>Displays dynamic system changes in a text dialog box.</td>
</tr>
<tr>
<td>Make Model Read-only</td>
<td>Makes the system you are working in read-only.</td>
</tr>
<tr>
<td>Take Screenshots</td>
<td>Creates a .png file in the &lt;project_directory&gt; by default. You can navigate</td>
</tr>
<tr>
<td></td>
<td>and save to a directory of your choice.</td>
</tr>
<tr>
<td>Show Plug-In Catalog</td>
<td>Displays library details such as type, version, tags, etc. for all IPs in the</td>
</tr>
<tr>
<td></td>
<td>IP Catalog.</td>
</tr>
<tr>
<td>Show Adapter Reports</td>
<td>Displays adapter reports for any adapters added when transforming the system.</td>
</tr>
</tbody>
</table>

- You can view detailed debugging messages in the **Component Editor** while building a custom IP component.
- You can view the generated Tcl script while editing in the **Component Editor** with the **Advanced ➤ Show Tcl for Component** command.
- You can launch the System Console with debug logging.

**6.2. Scripting IP Core Generation**

Use the `qsys-script` and `qsys-generate` utilities to define and generate an IP core variation outside of the Intel Quartus Prime GUI.

To parameterize and generate an IP core at command-line, follow these steps:
1. Run `qsys-script` to start a Tcl script that instantiates the IP and sets parameters:

```
qsys-script --script=<script_file>.tcl
```

2. Run `qsys-generate` to generate the IP core variation:

```
qsys-generate <IP variation file>.qsys
```

### Related Information

Generate a Platform Designer System with `qsys-script` on page 382

#### 6.2.1. `qsys-generate` Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;lst arg file&gt;</code></td>
<td>Required</td>
<td>Specifies the name of the .qsys system file to generate.</td>
</tr>
<tr>
<td><code>--block-symbol-file</code></td>
<td>Optional</td>
<td>Creates a Block Symbol File (.bsf) for the Platform Designer system.</td>
</tr>
<tr>
<td><code>--clear-output-directory</code></td>
<td>Optional</td>
<td>Clears the output directory corresponding to the selected target, that is, simulation or synthesis.</td>
</tr>
<tr>
<td><code>--example-design=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Creates example design files. For example, <code>--example-design</code> or <code>--example-design=all</code>. The default is <code>All</code>, which generates example designs for all instances. Alternatively, choose specific filesets based on instance name and fileset name. For example <code>--example-design=instance0.example_design1,instance1.example_design2</code>. Specify an output directory for the example design files creation.</td>
</tr>
<tr>
<td><code>--family=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Sets the device family name.</td>
</tr>
<tr>
<td><code>--help</code></td>
<td>Optional</td>
<td>Displays help for <code>--qsys-generate</code>.</td>
</tr>
<tr>
<td><code>--greybox</code></td>
<td>Optional</td>
<td>If you are synthesizing your design with a third-party EDA synthesis tool, generate a netlist for the synthesis tool to estimate timing and resource usage for this design. <em>Note:</em> Generation of a timing and area estimation (gray box) netlist is available only for individual Intel FPGA IP, and not for Platform Designer systems.</td>
</tr>
<tr>
<td><code>--ipxact</code></td>
<td>Optional</td>
<td>If you specify this option, Platform Designer generates the post-generation system as an IPXACT-compatible component description. <em>Note:</em> Platform Designer supports importing and exporting files in IP-XACT 2009 format and exporting IP-XACT files in 2014 format.</td>
</tr>
<tr>
<td><code>--jvm-max-heap-size=&lt;value&gt;</code></td>
<td>Optional</td>
<td>The maximum memory size that Platform Designer uses when running <code>qsys-generate</code>. You specify the value as <code>&lt;size&gt;&lt;unit&gt;</code>, where unit is m (or M) for multiples of megabytes or g (or G) for multiples of gigabytes. The default value is 512m.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--parallel=[&lt;level&gt;]</td>
<td>Optional</td>
<td>Directs Platform Designer to generate in parallel mode, with the level of parallelism that you specify. If you omit the level, Platform Designer determines a number based on processor availability and number of files to be generated.</td>
</tr>
<tr>
<td>--part=&lt;value&gt;</td>
<td>Optional</td>
<td>Sets the device part number. If set, this option overrides the --family option.</td>
</tr>
<tr>
<td>--search-path=&lt;value&gt;</td>
<td>Optional</td>
<td>If you omit this command, Platform Designer uses a standard default path. If you provide this command, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$$&quot;, for example, &quot;/extra/dir,$&quot;.</td>
</tr>
<tr>
<td>--simulation=&lt;VERILOG</td>
<td>VHDL&gt;</td>
<td>Optional</td>
</tr>
<tr>
<td>--synthesis=&lt;VERILOG</td>
<td>VHDL&gt;</td>
<td>Optional</td>
</tr>
<tr>
<td>--testbench=&lt;SIMPLE</td>
<td>STANDARD&gt;</td>
<td>Optional</td>
</tr>
<tr>
<td>--testbench-simulation=&lt;VERILOG</td>
<td>VHDL&gt;</td>
<td>Optional</td>
</tr>
<tr>
<td>--upgrade-ip-cores</td>
<td>Optional</td>
<td>Enables upgrading all the IP cores that support upgrade in the Platform Designer system you specify. This command has no impact on IP cores in any subsystem.</td>
</tr>
<tr>
<td>--upgrade-variation-file</td>
<td>Optional</td>
<td>If you set this option to true, the file argument for this command accepts a .v file, which contains a IP variant. This file parameterizes a corresponding instance in a Platform Designer system of the same name.</td>
</tr>
</tbody>
</table>

6.3. Display Available IP Components with ip-catalog

The `ip-catalog` command displays a list of available IP components relative to the current Intel Quartus Prime project directory, as either text or XML.

You can use the following options with the `ip-catalog` utility:

Table 187. `ip-catalog` Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--project-dir= &lt;directory&gt;</td>
<td>Optional</td>
<td>Finds IP components relative to the Intel Quartus Prime project directory. By default, Platform Designer uses &quot;.&quot; as the current directory. To exclude a project directory, leave the value empty.</td>
</tr>
<tr>
<td>--type</td>
<td>Optional</td>
<td>Provides a pattern to filter the type of available plug-ins. By default, Platform Designer shows only IP components. To look for a partial type string, surround with *, for instance, &quot;<em>connection</em>&quot;.</td>
</tr>
</tbody>
</table>

continued...
## 6.4. Create an .ipx File with ip-make-ipx

The `ip-make-ipx` command creates an .ipx index file. This file provides a convenient way to include a collection of IP components from an arbitrary directory. You can edit the .ipx file to disable visibility of one or more IP components in the IP Catalog.

You can use the following options with the `ip-make-ipx` utility:

### Table 188. ip-make-ipx Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>--source-directory=&lt;directory&gt;</code></td>
<td>Optional</td>
<td>Specifies the directory containing your IP components. The default directory is &quot;.&quot;. You can provide a comma-separated list of directories.</td>
</tr>
<tr>
<td><code>--output=&lt;file&gt;</code></td>
<td>Optional</td>
<td>Specifies the name of the index file to generate. The default name is <code>/component.ipx</code>. Set as <code>--output=&quot;&quot;</code> to print the output to the console.</td>
</tr>
<tr>
<td><code>--relative-vars=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Causes the output file to include references relative to the specified variable or variables wherever possible. You can specify multiple variables as a comma-separated list.</td>
</tr>
<tr>
<td><code>--thorough-descent</code></td>
<td>Optional</td>
<td>If you set this option, Platform Designer searches all the component files, without skipping the sub-directories.</td>
</tr>
<tr>
<td><code>--message-before=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Prints a log message at the start of reading an index file.</td>
</tr>
</tbody>
</table>

*continued...*
### 6.5. Generate Simulation Scripts

You can use the `ip-make-simscript` utility to generate simulation scripts for one or more simulators, given one or more Simulation Package Descriptor (.spd) files, .qsys files, and .ip files.

In Platform Designer, `ip-make-simscript` generates simulation scripts in a hierarchical structure instead of a flat view of the entire system. The `ip-make-simscript` utility uses .spd and system files according to the options you select:

- When targeting only .spd files (`ip-make-simscript --spd=<file>.spd`) the utility combines the contents of all input .spd files, and generates a common directory which contains a set of `<simulator>_files.tcl` files under the specified output directory.

- When targeting only system files (`ip-make-simscript --system-file=<file>`) such as .qsys and .ip files, the utility searches for instances of `<simulator>_files.tcl` files for each input system, and generates a combined simulation script which contains a list of references of `<simulator>_files.tcl`.

- When the utility uses both --spd and --system-file options, `ip-make-simscript` combines all input .spd files and generates a common/ `<simulator>_files.tcl` in the specified output directory. The generated simulation script refers to the generated common/ `<simulator>_files.tcl` first, followed by a list of Tcl files from each input system.

**Table 189. ip-make-simscript Command-Line Options**

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>--spd=&lt;file&gt;</code></td>
<td>Optional/Repeatable</td>
<td>The .spd files describe the list of HDL files for simulation, and memory models hierarchy. This argument can either be a single path to an .spd file or a comma-separated list of paths of .spd files. For instance, <code>--spd=ipcore_1.spd,ipcore_2.spd</code> The generated list is processed in the order of the input .spd files. Note: When this argument is used in combination with --system-file, the .spd files are parsed before the system files.</td>
</tr>
<tr>
<td><code>--system-file=&lt;file&gt;</code></td>
<td>Optional/Repeatable</td>
<td>Specifies the system files (.qsys or .ip files) used to generate the simulation scripts. This argument can contain either a single path to a Platform Designer system file or a comma-separated list of paths to Platform Designer system files.</td>
</tr>
</tbody>
</table>

---

**Option** | **Usage** | **Description**  
---|---|---  
`--message-after=<value>` | Optional | Prints a log message at the end of reading an index file.  
`--jvm-max-heap-size=<value>` | Optional | The maximum memory size Platform Designer uses when running `ip-make-ipx`. You specify this value as `<size><unit>`, where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes. The default value is 512m.  
`--help` | Optional | Displays help for the `ip-make-ipx` command.
Option | Usage | Description
--- | --- | ---
The simulation script is generated in the order the system files are listed. 
Note: When this argument is used in combination with --ssp, the .ssp files are parsed before the system files.

--output-directory[=directory] | Optional | Specifies the directory path for the location of output files. If you do not specify a directory, the output directory defaults to the directory from which --ip-make-simscript runs.

--compile-to-work | Optional | Compiles all design files to the default library - work.

--use-relative-paths | Optional | Uses relative paths whenever possible.


--quiet | Optional | Quiet reporting mode. Does not report generated files.

--jvm-max-heap-size=value | Optional | The maximum memory size Platform Designer uses when running ip-make-simscript. You specify this value as

\[size] [unit]

where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes. The default value is 512m.

--search-path=value | Optional | Comma-separated list of search paths. 
If omitted, a default path including the current working directory is used.
To include the standard path in your replacement, append the $ symbol, for example:

"/extra/dir,$"

--device-family=value | Optional | Overrides the existing device family when used.

--top-name=value | Optional | Specify a top-level entity name used in generated simulation scripts.

--help | Optional | Displays help for --ip-make-simscript.

### 6.6. Generate a Platform Designer System with qsys-script

You can use the qsys-script utility to create and manipulate a Platform Designer system with Tcl scripting commands. If you specify a system, Platform Designer loads that system before executing any of the scripting commands.

*Note:* You must provide a package version for the qsys-script. If you do not specify the --package-version=value command, you must then provide a Tcl script and request the system scripting API directly with the package require -exact qsys<version> command.

**Example 29. Platform Designer Command-Line Scripting**

```bash
qsys-script --script=my_script.tcl \
--system-file=fancy.qsys
```
my_script.tcl contains:

```tcl
package require -exact qsys 16.0
# get all instance names in the system and print one by one
set instances [ get_instances ]
foreach instance $instances {
    send_message Info "$instance"
}
```

You can use the following options with the `qsys-script` utility:

**Table 190. qsys-script Command-Line Options**

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>--system-file=&lt;file&gt;</code></td>
<td>Optional</td>
<td>Specifies the path to a <code>.qsys</code> file. Platform Designer loads the system before running scripting commands.</td>
</tr>
<tr>
<td><code>--script=&lt;file&gt;</code></td>
<td>Optional</td>
<td>A file that contains Tcl scripting commands that you can use to create or manipulate a Platform Designer system. If you specify both <code>--cmd</code> and <code>--script</code>, Platform Designer runs the <code>--cmd</code> commands before the script specified by <code>--script</code>.</td>
</tr>
<tr>
<td><code>--cmd=&lt;value&gt;</code></td>
<td>Optional</td>
<td>A string that contains Tcl scripting commands that you can use to create or manipulate a Platform Designer system. If you specify both <code>--cmd</code> and <code>--script</code>, Platform Designer runs the <code>--cmd</code> commands before the script specified by <code>--script</code>.</td>
</tr>
<tr>
<td><code>--package-version=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Specifies which Tcl API scripting version to use and determines the functionality and behavior of the Tcl commands. The Intel Quartus Prime software supports Tcl API scripting commands. The minimum supported version is 12.0. If you do not specify the version on the command-line, your script must request the scripting API directly with the <code>package require -exact qsys &lt;version&gt;</code> command.</td>
</tr>
<tr>
<td><code>--search-path=&lt;value&gt;</code></td>
<td>Optional</td>
<td>If you omit this command, a Platform Designer uses a standard default path. If you provide this command, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$&quot;, for example, /&lt;directory path&gt;/dir,$. Separate multiple directory references with a comma.</td>
</tr>
<tr>
<td><code>--quartus-project=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Specifies the path to a <code>.qpf</code> Intel Quartus Prime project file. Utilizes the specified Intel Quartus Prime project to add the file saved using <code>save_system</code> command. If you omit this command, Platform Designer uses the default revision as the project name.</td>
</tr>
<tr>
<td><code>--new-quartus-project=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Specifies the name of the new Intel Quartus Prime project. Creates a new Intel Quartus Prime project at the specified path and adds the file saved using <code>save_system</code> command to the project. If you omit this command, Platform Designer uses the Intel Quartus Prime project revision as the new Intel Quartus Prime project name.</td>
</tr>
<tr>
<td><code>--rev=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Allows you to specify the name of the Intel Quartus Prime project revision.</td>
</tr>
<tr>
<td><code>--jvm-max-heap-size=&lt;value&gt;</code></td>
<td>Optional</td>
<td>The maximum memory size that the <code>qsys-script</code> tool uses. You specify this value as <code>&lt;size&gt;&lt;unit&gt;</code>, where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes.</td>
</tr>
<tr>
<td><code>--help</code></td>
<td>Optional</td>
<td>Displays help for the <code>qsys-script</code> utility.</td>
</tr>
</tbody>
</table>
6.7. Parameterizing an Instantiated IP Core after save_system Command

When you call the save_system command in your Tcl script, Platform Designer converts all the instantiated IP cores in your system to generic components.

To modify these IP cores after saving your system, you must first load the actual component within the instantiated generic component. Re-parameterize an instantiated IP core using one of the following methods:

1. Load the component in the Platform Designer system, modify the component's parameter value, and save the component:

   ```tcl
   ... save_system kernel_system.qsys
   ... load_component cra_root
   set_component_parameter_value DATA_W 64
   save_component
   ...
   ```

2. Load the .ip file specific to the component, modify the instance's parameter value, and save the .ip file:

   ```tcl
   ... save_system kernel_system.qsys
   ... load_system cra_root.ip
   set_instance_parameter_value cra_root DATA_W 64
   save_system
   ...
   ```

   Note: To directly modify an instance parameter value after the save_system command, you must load the .ip file corresponding to the IP component.

Related Information

- set_component_parameter_value on page 513
- load_component on page 510
- save_component on page 512
- save_system on page 400
6.8. Validate the Generic Components in a System with qsys-validate

Use the qsys-validate utility to run IP component footprint validation on the .qsys file for the system.

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st arg file</td>
<td>Optional</td>
<td>The name of the .qsys system file to validate.</td>
</tr>
<tr>
<td>--search-path[=&lt;value&gt;]</td>
<td>Optional</td>
<td>If omitted, Platform Designer uses a standard default path. If provided, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$&quot;, for example: /extra/dir.$</td>
</tr>
<tr>
<td>--strict</td>
<td>Optional</td>
<td>Enables strict validation. All warnings are reported as errors</td>
</tr>
<tr>
<td>--jvm-max-heap-size=&lt;value&gt;</td>
<td>Optional</td>
<td>The maximum memory size Platform Designer uses for allocations when running qsys-edit. You specify this value as &lt;size&gt;&lt;unit&gt;, where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes. The default value is 512m.</td>
</tr>
<tr>
<td>--help</td>
<td>Optional</td>
<td>Display help for qsys-validate.</td>
</tr>
</tbody>
</table>

6.9. Generate an IP Component or Platform Designer System with quartus_ipgenerate

The quartus_ipgenerate command allows you to generate IP components or a Platform Designer system in your Intel Quartus Prime project. Ensure that you include the IP component or the Platform Designer system you wish to generate in your Intel Quartus Prime project.

To run the quartus_ipgenerate command from the Intel Quartus Prime shell, type:

```
quartus_ipgenerate <project name> [<options>]
```

Use any of the following options with the quartus_ipgenerate utility:

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;1st arg file&gt;</td>
<td>Required</td>
<td>Specifies the name of the Intel Quartus Prime project file (.qpf). This option generates all the .qsys and .ip files in the specified Intel Quartus Prime project (&lt;project name&gt;).</td>
</tr>
<tr>
<td>-f [&lt;argument file&gt;]</td>
<td>Optional</td>
<td>Specifies a file containing additional command-line arguments. Arguments that you specify after this option can conflict or override the options you specify in the argument file.</td>
</tr>
<tr>
<td>--rev[=&lt;revision name&gt;] or -c[=&lt;revision name&gt;]</td>
<td>Optional</td>
<td>Specifies the Intel Quartus Prime project revision and the associated .qsf file to use. If you omit this option, Platform Designer uses the same revision name as your Intel Quartus Prime project.</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>--clear_ip_generation_dirs</code> or <code>--clean</code></td>
<td>Optional</td>
<td>Clears the generation directories of all the <code>.qsys</code> or the <code>.ip</code> files in the specified Intel Quartus Prime project. For example, to clear the generation directories in the project <code>test</code>, run the following command:</td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>quartus_ipgenerate --clear_ip_generation_dirs test</code> or <code>quartus_ipgenerate --clean test</code></td>
</tr>
<tr>
<td><code>--generate_ip_file --ip_file[=&lt;ip file name&gt;]</code></td>
<td>Optional</td>
<td>Generates the files for <code>&lt;file name&gt;</code>.ip file in the specified Intel Quartus Prime project. Use the following optional flags with <code>--generate_ip_file</code>:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--synthesis[=&lt;value&gt;]</code>—optional argument that specifies the synthesis target type. Specify the value as either <code>verilog</code> or <code>vhdl</code>. The default value is <code>verilog</code>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--simulation[=&lt;value&gt;]</code>—optional argument that specifies the simulation target type. Specify the value as either <code>verilog</code> or <code>vhdl</code>. If you omit this flag, Platform Designer does not generate any simulation files.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--clear_ip_generation_dirs</code>—clears the preexisting generation directories before generation. If you omit this command, Platform Designer does not clear the generation directories.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For example, to generate the files for a <code>test.qsys</code> file within the project, <code>test</code>:</td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>quartus_ipgenerate --generate_ip_file --synthesis=vhdl --simulation=verilog --clear_ip_generation_dirs --ip_file=test.qsys test</code></td>
</tr>
<tr>
<td><code>--generate_project_ip_files [&lt;project name&gt;]</code></td>
<td>Optional</td>
<td>Generates the files for all the <code>.qsys</code> and <code>.ip</code> files in the specified Intel Quartus Prime project. Use any of the following optional flags with <code>--generate_project_ip_files</code>:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--synthesis[=&lt;value&gt;]</code>—optional argument that specifies the synthesis target type. Specify the value as either <code>verilog</code> or <code>vhdl</code>. The default value is <code>verilog</code>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--simulation[=&lt;value&gt;]</code>—optional argument that specifies the simulation target type. Specify the value as either <code>verilog</code> or <code>vhdl</code>. If you omit this flag, Platform Designer does not generate any simulation files.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--clear_ip_generation_dirs</code>—clears the preexisting generation directories before generation. If you omit this command, Platform Designer does not clear the generation directories.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For example, to generate all the <code>.qsys</code> and <code>.ip</code> files within the project, <code>test</code>:</td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>quartus_ipgenerate --generate_project_ip_files --synthesis=vhdl --simulation=verilog --clear_ip_generation_dirs test</code></td>
</tr>
</tbody>
</table>
### 6.10. Generate an IP Variation File with ip-deploy

Use the `ip-deploy` utility to generate an IP variation file (.ip file) in the specified location.

**Table 193. ip-deploy Command-Line Options**

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--component-name=&lt;{value}&gt;</td>
<td>Required</td>
<td>The name of a component you instantiate.</td>
</tr>
<tr>
<td>--output-name=&lt;{value}&gt;</td>
<td>Optional</td>
<td>Name for the resulting component; defaults to the component’s type name.</td>
</tr>
<tr>
<td>--component-parameter=&lt;{value}&gt;</td>
<td>Optional</td>
<td>Repeatable. A single value assignment, like <code>--component-param=WIDTH=11</code>. To assign multiple parameters, use this option several times.</td>
</tr>
<tr>
<td>--preset=&lt;{value}&gt;</td>
<td>Optional</td>
<td>Repeatable. The name of a saved preset to use in creating a variation of the IP component. Presets are additive and repeatable.</td>
</tr>
<tr>
<td>--family=&lt;{value}&gt;</td>
<td>Optional</td>
<td>Sets the device family</td>
</tr>
<tr>
<td>--part=&lt;{value}&gt;</td>
<td>Optional</td>
<td>Sets the device part number. You can also use this command to set the base device, device speed-grade, device family, and device feature's system information.</td>
</tr>
<tr>
<td>--output-directory=&lt;{value}&gt;</td>
<td>Optional</td>
<td>This directory contains the output IP variation file.</td>
</tr>
<tr>
<td>--search-path=&lt;{value}&gt;</td>
<td>Optional</td>
<td>If you do not specify the search path, the command uses a standard default path. If you provide a search path, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$&quot;, like <code>/extra/dir,$</code>.</td>
</tr>
<tr>
<td>--jvm-max-heap-size=&lt;{value}&gt;</td>
<td>Optional</td>
<td>The maximum memory size Platform Designer uses for allocations when running qsys-edit. You specify this value as <code>&lt;size&gt;&lt;unit&gt;</code>, where unit is m (megabytes) or g (gigabytes). The default value is 512m.</td>
</tr>
<tr>
<td>--help</td>
<td>Optional</td>
<td>Displays help for ip-deploy</td>
</tr>
</tbody>
</table>
6.11. Archive a Platform Designer System with qsys-archive

The `qsys-archive` command allows you to archive a system, extract an archived system, and retrieve information about the system’s dependencies.

### Table 194. qsys-archive Command-Line Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Usage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>&lt;1st arg file&gt;</code></td>
<td>Required</td>
<td>The filename of the root Platform Designer system, Platform Designer file archive, or the Intel Quartus Prime project file.</td>
</tr>
<tr>
<td><code>--search-path[=&lt;value&gt;]</code></td>
<td>Optional</td>
<td>If you omit this option, Platform Designer uses a standard default path. If you specify this option, Platform Designer searches a comma-separated list of paths. To include the standard path in your replacement, use &quot;$&quot;, for example: <code>/extra/dir,\$</code>.</td>
</tr>
<tr>
<td><code>--archive</code></td>
<td>Optional</td>
<td>Creates a zip archive of the specified Platform Designer system or the Intel Quartus Prime project.</td>
</tr>
<tr>
<td><code>--report-file[=&lt;value&gt;]</code></td>
<td>Optional</td>
<td>Lists the files that the Platform Designer system or the Intel Quartus Prime project references, and writes the files list to the specified name in .txt format.</td>
</tr>
<tr>
<td><code>--output-directory[=&lt;file&gt;]</code></td>
<td>Optional</td>
<td>Specifies the output directory to save the archive.</td>
</tr>
<tr>
<td><code>--extract</code></td>
<td>Optional</td>
<td>Extracts all the files in the given archive.</td>
</tr>
<tr>
<td><code>--output-name[=&lt;value&gt;]</code></td>
<td>Optional</td>
<td>Specifies the output name to save the archive or report.</td>
</tr>
<tr>
<td>`collect-to-common-directory[=&lt;true</td>
<td>false&gt;]`</td>
<td>Optional</td>
</tr>
<tr>
<td><code>new-quartus-project[=&lt;value&gt;]</code></td>
<td>Optional</td>
<td>Creates a new Intel Quartus Prime project which contains all the .ip and system files referenced by the Platform Designer system or the Intel Quartus Prime project.</td>
</tr>
<tr>
<td><code>quartus-project[=&lt;value&gt;]</code></td>
<td>Optional</td>
<td>When you use this command in combination with:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--report-file</code>—adds all the referenced files to the Intel Quartus Prime project.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--extract</code>—adds all extracted files to the specified project.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• <code>--archive</code>—archives all the system and .ip files referenced in the Intel Quartus Prime project.</td>
</tr>
<tr>
<td><code>--rev</code></td>
<td>Optional</td>
<td>Specifies the name of the Intel Quartus Prime project revision.</td>
</tr>
<tr>
<td><code>--include-generated-files</code></td>
<td>Optional</td>
<td>Includes all the generated files of the Platform Designer system.</td>
</tr>
<tr>
<td><code>--force</code></td>
<td>Optional</td>
<td>Forcefully creates the specified archive or report, overwriting any existing archives or reports.</td>
</tr>
<tr>
<td><code>--jvm-max-heap-size=&lt;value&gt;</code></td>
<td>Optional</td>
<td>Specifies the maximum memory size Platform Designer uses for allocations when running <code>qsys-edit</code>. Specify this value as <code>&lt;size&gt;&lt;unit&gt;</code>, where unit is m (or M) for multiples of megabytes, or g (or G) for multiples of gigabytes. The default value is 512m.</td>
</tr>
<tr>
<td><code>--help</code></td>
<td>Optional</td>
<td>Displays help for <code>qsys-archive</code>.</td>
</tr>
</tbody>
</table>

Alternatively, you can archive and restore your system using the Platform Designer GUI. For more information, refer to Archive your System section.
6.12. Platform Designer Scripting Command Reference

Platform Designer system scripting provides Tcl commands to manipulate your system. The `qsys-script` provides a command-line alternative to the Platform Designer tool. Use the `qsys-script` commands to create and modify your system, as well as to create reports about the system.

To use the current version of the Tcl commands, include the following line at the top of your script:

```tcl
package require -exact qsys <version>
```

For example, for the current release of the Intel Quartus Prime software, include:

```tcl
package require -exact qsys 18.0
```

The Platform Designer scripting commands fall under the following categories:

- **System** on page 390
- **Subsystems** on page 404
- **Domains and Interfaces** on page 412
- **Instances** on page 417
- **Instantiations** on page 450
- **Components** on page 489
- **Connections** on page 515
- **Top-level Exports** on page 527
- **Validation** on page 541
- **Miscellaneous** on page 552
- **Wire-Level Connection Commands** on page 562
6.12.1. System

This section lists the commands that allow you to manipulate a Platform Designer system.

- `create_system` on page 391
- `export_hw_tcl` on page 392
- `get_device_families` on page 393
- `get_devices` on page 394
- `get_module_properties` on page 395
- `get_module_property` on page 396
- `get_project_properties` on page 397
- `get_project_property` on page 398
- `load_system` on page 399
- `save_system` on page 400
- `set_design_id` on page 400
- `set_module_property` on page 402
- `set_project_property` on page 403
6.12.1.1. create_system

Description
Replaces the current system with a new system of the specified name.

Usage
create_system [<name>]

Returns
No return value.

Arguments

name (optional)  The new system name.

Example
create_system my_new_system_name

Related Information
- load_system on page 399
- save_system on page 400
6.12.1.2. export_hw_tcl

**Description**
Allows you to save the currently open system as an `.hw.tcl` file in the project directory. The saved systems appears under the **System** category in the IP Catalog.

**Usage**
export_hw_tcl

**Returns**
No return value.

**Arguments**
No arguments

**Example**

```
export_hw_tcl
```

**Related Information**
- `load_system` on page 399
- `save_system` on page 400
6.12.1.3. `get_device_families`

**Description**
Returns the list of installed device families.

**Usage**
```
get_device_families
```

**Returns**

`String[]` The list of device families.

**Arguments**
No arguments

**Example**
```
get_device_families
```

**Related Information**
`get_devices` on page 394
6.12.1.4. get_devices

Description
Returns the list of installed devices for the specified family.

Usage
get_devices <family>

Returns

String[] The list of devices.

Arguments

family Specifies the family name to get the devices for.

Example

get_devices exampleFamily

Related Information
get_device_families on page 393
6.12.1.5. `get_module_properties`

**Description**
Returns the properties that you can manage for a top-level module of the Platform Designer system.

**Usage**
get_module_properties

**Returns**
The list of property names.

**Arguments**
No arguments.

**Example**
get_module_properties

**Related Information**
- `get_module_property` on page 396
- `set_module_property` on page 402
6.12.1.6. get_module_property

Description
Returns the value of a top-level system property.

Usage
get_module_property <property>

Returns
The property value.

Arguments

property  The property name to query. Refer to Module Properties.

Example
get_module_property NAME

Related Information
- get_module_properties on page 395
- set_module_property on page 402
6.12.1.7. get_project_properties

**Description**
Returns the list of properties that you can query for properties pertaining to the Intel Quartus Prime project.

**Usage**
get_project_properties

**Returns**
The list of project properties.

**Arguments**
No arguments

**Example**
get_project_properties

**Related Information**
- get_project_property on page 398
- set_project_property on page 403
6.12.1.8. get_project_property

**Description**
Returns the value of an Intel Quartus Prime project property.

**Usage**
get_project_property <property>

**Returns**
The property value.

**Arguments**

*property*  The project property name. Refer to *Project properties*.

**Example**

```
get_project_property DEVICE_FAMILY
```

**Related Information**
- get_module_properties on page 395
- get_module_property on page 396
- set_module_property on page 402
- Project Properties on page 580
6.12.1.9. load_system

**Description**
Loads the Platform Designer system from a file, and uses the system as the current system for scripting commands.

**Usage**
load_system <file>

**Returns**
No return value.

**Arguments**

*file* The path to the .qsys file.

**Example**
load_system example.qsys

**Related Information**
- create_system on page 391
- save_system on page 400
6.12.1.10. save_system

Description
Saves the current system to the specified file. If you do not specify the file, Platform Designer saves the system to the same file opened with the load_system command.

Usage
save_system <file>

Returns
No return value.

Arguments

file  If available, the path of the .qsys file to save.

Example
save_system
save_system file.qsys

Related Information
- load_system on page 399
- create_system on page 391

6.12.1.11. set_design_id

Description
Specifies an alphanumeric string that identifies the system.

If you specify set_design_id when creating a system, the generated system includes a SOPCINFO file with a new design_id attribute in the EnsembleReport element:

<EnsembleReport
name="my_system"
kind="my_system"
design_id="my_design_id"
version="1.0"
fabric="QSYS">

Usage
set_design_id <design-id>

Returns
No return value.
Arguments

design-id (optional)  An alphanumeric string that identifies the system.

Example

set_design_id foo121
6.12.1.12. set_module_property

**Description**
Specifies the Tcl procedure to evaluate changes in Platform Designer system instance parameters.

**Usage**
set_module_property <property> <value>

**Returns**
No return value.

**Arguments**

*property* The property name. Refer to Module Properties.

*value* The new value of the property.

**Example**
set_module_property COMPOSITION_CALLBACK "my_composition_callback"

**Related Information**
- get_module_properties on page 395
- get_module_property on page 396
- Module Properties on page 574
6.12.1.13. set_project_property

**Description**
Sets the project property value, such as the device family.

**Usage**
set_project_property <property> <value>

**Returns**
No return value.

**Arguments**

property  The property name. Refer to Project Properties.

value  The new property value.

**Example**
set_project_property DEVICE_FAMILY "Cyclone IV GX"

**Related Information**
- get_project_properties on page 397
- get_project_property on page 398
- Project Properties on page 580
6.12.2. Subsystems

This section lists the commands that allow you to obtain the connection and parameter information of instances in your Platform Designer subsystem.

get_composed_connections on page 405
get_composed_connection_parameter_value on page 406
get_composed_connection_parameters on page 407
get_composed_instance_assignment on page 408
get_composed_instance_assignments on page 409
get_composed_instance_parameter_value on page 410
get_composed_instance_parameters on page 411
get_composed_instances on page 412
6.12.2.1. get_composed_connections

Description
Returns the list of all connections in the subsystem for an instance that contains the subsystem of the Platform Designer system.

Usage
get_composed_connections <instance>

Returns
The list of connection names in the subsystem.

Arguments

instance  The child instance containing the subsystem.

Example
get_composed_connections subsystem_0

Related Information

•  get_composed_connection_parameter_value on page 406
•  get_composed_connection_parameters on page 407
6.12.2.2. get_composed_connection_parameter_value

Description
Returns the parameter value of a connection in a child instance containing the subsystem.

Usage
get_composed_connection_parameter_value <instance> <child_connection> <parameter>

Returns
The parameter value.

Arguments

instance  The child instance that contains the subsystem.

child_connection  The connection name in the subsystem.

parameter  The parameter name to query for the connection.

Example
get_composed_connection_parameter_value subsystem_0 cpu.data_master/memory.s0 baseAddress

Related Information
•  get_composed_connection_parameters on page 407
•  get_composed_connections on page 405
6.12.2.3. get_composed_connection_parameters

**Description**
Returns the list of parameters of a connection in the subsystem, for an instance that contains the subsystem.

**Usage**
get_composed_connection_parameters <instance> <child_connection>

**Returns**
The list of parameter names.

**Arguments**

*instance*   The child instance containing the subsystem.

*child_connection*   The name of the connection in the subsystem.

**Example**
get_composed_connection_parameters subsystem_0 cpu.data_master/memory.s0

**Related Information**
- get_composed_connection_parameter_value on page 406
- get_composed_connections on page 405
6.12.2.4. `get_composed_instance_assignment`

**Description**
Returns the assignment value of the child instance in the subsystem.

**Usage**
```
get_composed_instance_assignment <instance> <child_instance> <assignment>
```

**Returns**
The assignment value.

**Arguments**
- `instance`  The subsystem containing the child instance.
- `child_instance`  The child instance name in the subsystem.
- `assignment`  The assignment key.

**Example**
```
get_composed_instance_assignment subsystem_0 video_0
"embeddedsw.CMacro.colorSpace"
```

**Related Information**
- `get_composed_instance_assignments` on page 409
- `get_composed_instances` on page 412
6.12.2.5. get_composed_instance_assignments

**Description**
Returns the list of assignments of the child instance in the subsystem.

**Usage**
get_composed_instance_assignments <instance> <child_instance>

**Returns**
The list of assignment names.

**Arguments**

*instance*  The subsystem containing the child instance.

*child_instance*  The child instance name in the subsystem.

**Example**
get_composed_instance_assignments subsystem_0 cpu

**Related Information**
- get_composed_instance_assignment on page 408
- get_composed_instances on page 412
6.12.2.6. get_composed_instance_parameter_value

**Description**
Returns the parameter value of the child instance in the subsystem.

**Usage**
get_composed_instance_parameter_value <instance> <child_instance> <parameter>

**Returns**
The parameter value of the instance in the subsystem.

**Arguments**

- **instance**  The subsystem containing the child instance.
- **child_instance**  The child instance name in the subsystem.
- **parameter**  The parameter name to query on the child instance in the subsystem.

**Example**

```
get_composed_instance_parameter_value subsystem_0 cpu DATA_WIDTH
```

**Related Information**
- get_composed_instance_parameters on page 411
- get_composed_instances on page 412
6.12.2.7. **get_composed_instance_parameters**

**Description**

Returns the list of parameters of the child instance in the subsystem.

**Usage**

```
get_composed_instance_parameters <instance> <child_instance>
```

**Returns**

The list of parameter names.

**Arguments**

- `instance`  The subsystem containing the child instance.
- `child_instance`  The child instance name in the subsystem.

**Example**

```
get_composed_instance_parameters subsystem_0 cpu
```

**Related Information**

- [get_composed_instance_parameter_value](#) on page 410
- [get_composed_instances](#) on page 412
6.12.2.8. get_composed_instances

**Description**
Returns the list of child instances in the subsystem.

**Usage**
get_composed_instances <instance>

**Returns**
The list of instance names in the subsystem.

**Arguments**

*instance*  The subsystem containing the child instance.

**Example**
get_composed_instances subsystem_0

**Related Information**
- get_composed_instance_assignment on page 408
- get_composed_instance_assignments on page 409
- get_composed_instance_parameter_value on page 410
- get_composed_instance_parameters on page 411

6.12.3. Domains and Interfaces

This section lists the commands that allow you to specify parameters for domains and interfaces in your system.

**Related Information**
Specifying Interconnect Parameters on page 50

6.12.3.1. set_domain_assignment

**Description**
Sets the assignment value to all connections on the given domain.

**Usage**
set_domain_assignment <element> <assignment> <value>

**Arguments**

*element*  Connection or interface in the domain to set with assignment. If element name is $system, assigns to all the domains in the system.

*assignment*  The name of the assignment.
value  The value of the assignment.

6.12.3.2. `get_domain_assignment`

**Description**
Obtains the value for specified assignment in the given domain.

**Usage**
`get_domain_assignment <element> <assignment>`

**Arguments**
- **element**  Connection or interface in the domain for which you want the assignment value.
- **assignment**  The name of the assignment.

6.12.3.3. `get_domain_assignments`

**Description**
Obtains all domain assignments for the given domain as a list of strings. Each "group" of three elements in the list contains the element name, assignment name, and value (in that order). Element name in the output is the input element name. If the input element is $system, then the output element name is the connection point in the domain. For example, typical list contents appear like this:

```
[element0 name0 value0 element1 name1 value1 ... ]
```

In TCL, you'd loop over the list by writing a foreach loop:

```
foreach {element name value } $requirement_list {
    puts "$element $name $value"
}
```

**Usage**
`get_domain_assignments <element>`

**Arguments**
- **element**  Connection or interface in the domain for which you want to get assignments. If element is specified as $system, gives values of all the domains in the system.

6.12.3.4. `set_interface_assignment`

**Description**
Adds interconnect assignment to the interface.

**Usage**
`set_interface_assignment <interface> <assignment> <value>`
Arguments

interface Interface name.

assignment The name of the assignment.

value The value of the assignment.

6.12.3.5. get_interface_assignment

Description
Obtains the value of the named interface interconnect assignment on the specified interface.

Usage
get_interface_assignment <interface> <assignment>

Arguments

interface Interface name.

assignment The name of the assignment.

6.12.3.6. get_interface_assignments

Description
Obtains all interface interconnect assignments for the given domain as a list of strings. Each "group" of three elements in the list contains the interface name, assignment name, and value (in that order). For example, typical list contents might look like this:

[interface0 name0 value0 interface1 name1 value1 ...]

In TCL, you'd loop over the list by writing a foreach loop:

foreach {interface name value} $requirement_list {
    puts "$interface $name $value"
}

Usage
get_interface_assignments <interface>

Arguments

interface Interface name that you want to get assignments for. If interface is specified as $system, it gives assignments of all the interfaces in the system.

assignment The name of the assignment.
6.12.3.7. set_postadaptation_assignment

Description
Adds a post adaptation interconnect assignment.

Usage
set_postadaptation_assignment <element> <assignment> <value>

Arguments

element  Element name.

assignment  The name of the assignment.

value  The value of the assignment.

6.12.3.8. get_postadaptation_assignment

Description
Obtains the value of the named post adaptation interconnect assignment on the specified element.

Usage
get_postadaptation_assignment <element> <assignment>

Arguments

element  Element name.

assignment  The name of the assignment.

6.12.3.9. get_postadaptation_assignments

Description
Obtains all post adaptation interconnect assignments for the given domain as a list of strings. Each "group" of three elements in the list contains the element name, assignment name, and value (in that order). For example, typical list contents might look like this:

[element0 name0 value0 element1 name1 value1 ... ]

In TCL, you'd loop over the list by writing a foreach loop:

foreach {element name value } $requirement_list \
   { puts "$element $name $value" }

Usage
get_postadaptation_assignments <interface>
Arguments

interface  Interface name that you want to get assignments for. If interface is specified as $system, it gives assignments of all the interfaces in the system.
6.12.4. Instances

This section lists the commands that allow you to manipulate the instances of IP components in your Platform Designer system.

- **add_instance** on page 418
- **apply_instance_preset** on page 419
- **create_ip** on page 420
- **add_component** on page 421
- **duplicate_instance** on page 422
- **enable_instance_parameter_update_callback** on page 423
- **get_instance_assignment** on page 424
- **get_instance_assignments** on page 425
- **get_instance_documentation_links** on page 426
- **get_instance_interface_assignment** on page 427
- **get_instance_interface_assignments** on page 428
- **get_instance_interface_parameter_property** on page 429
- **get_instance_interface_parameter_value** on page 430
- **get_instance_interface_parameters** on page 431
- **get_instance_interface_port_property** on page 432
- **get_instance_interface_ports** on page 433
- **get_instance_interface_properties** on page 434
- **get_instance_interfaces** on page 435
- **get_instance_parameter_property** on page 436
- **get_instance_parameter_value** on page 437
- **get_instance_parameter_values** on page 438
- **get_instance_parameters** on page 439
- **get_instance_port_property** on page 440
- **get_instance_properties** on page 441
- **get_instance_property** on page 442
- **get_instances** on page 443
- **is_instance_parameter_update_callback_enabled** on page 445
- **remove_instance** on page 446
- **set_instance_parameter_value** on page 447
- **set_instance_parameter_values** on page 448
- **set_instance_property** on page 449
6.12.4.1. add_instance

**Description**
Adds an instance of a component, referred to as a *child* or *child instance*, to the system.

**Usage**
```
add_instance <name> <type> [<version>]
```

**Returns**
No return value.

**Arguments**
- **name**: Specifies a unique local name that you can use to manipulate the instance. Platform Designer uses this name in the generated HDL to identify the instance.
- **type**: Refers to a kind of instance available in the IP Catalog, for example `altera_avalon_uart`.
- **version (optional)**: The required version of the specified instance type. If you do not specify any instance, Platform Designer uses the latest version.

**Example**
```
add_instance uart_0 altera_avalon_uart 16.1
```

**Related Information**
- `get_instance_property` on page 443
- `get_instances` on page 444
- `remove_instance` on page 446
- `set_instance_parameter_value` on page 447
- `get_instance_parameter_value` on page 438
6.12.4.2. apply_instance_preset

**Description**
Applies the settings in a preset to the specified instance.

**Usage**
apply_instance_preset *<preset_name>*

**Returns**
No return value.

**Arguments**

*<preset_name>*  The preset name.

**Example**
apply_preset "Custom Debug Settings"

**Related Information**
set_instance_parameter_value on page 447
6.12.4.3. create_ip

Description
Creates a new IP Variation system with the given instance.

Usage
create_ip <type> [ <instance_name> <version>]

Returns
No return value.

Arguments

  type  Kind of instance available in the IP catalog, for example, altera_avalon_uart.

  instance_name   (optional)  A unique local name that you can use to manipulate the instance. If not specified, Platform Designer uses a default name.

  version (optional)  The required version of the specified instance type. If not specified, Platform Designer uses the latest version.

Example
create_ip altera_avalon_uart altera_avalon_uart_inst 17.0

Related Information
  - add_component on page 421
  - load_system on page 399
  - save_system on page 400
  - set_instance_parameter_value on page 447
6.12.4.4. add_component

Description
Adds a new IP Variation component to the system.

Usage
add_component <instance_name> <file_name> [ <component_type> <component_instance_name> <component_version> ]

Returns
No return value.

Arguments

instance_name  A unique local name that you can use to manipulate the instance.

file_name  The IP variation file name. If a path is not specified, Platform Designer saves the file in the ./ip/system/ sub-folder of your system.

component_type  (optional)
The kind of instance available in the IP catalog, for example altera_avalon_uart.

component_instance_name  (optional)
The instance name of the component in the IP variation file. If not specified, Platform Designer uses a default name.

component_version  (optional)
The required version of the specified instance type. If not specified, Platform Designer uses the latest version.

Example
add_component myuart_0 myuart.ip altera_avalon_uart altera_avalon_uart_inst 17.0

Related Information
• load_component on page 510
• load_instantiation on page 477
• save_system on page 400
### 6.12.4.5. duplicate_instance

**Description**
Creates a duplicate instance of the specified instance.

**Usage**
duplicate_instance <instance> [ <name>]  

**Returns**

String  The new instance name.

**Arguments**

*instance*  Specifies the instance name to duplicate.

*name (optional)*  Specifies the name of the duplicate instance.

**Example**

duplicate_instance cpu cpu_0

**Related Information**
- add_instance on page 418
- remove_instance on page 446
6.12.4.6. enable_instance_parameter_update_callback

**Description**
Enables the update callback for instance parameters.

**Usage**
enable_instance_parameter_update_callback [<value>]

**Returns**
No return value.

**Arguments**

value (optional)  Specifies whether to enable/disable the instance parameters callback. Default option is "1".

**Example**
enabled_instance_parameter_update_callback

**Related Information**
- is_instance_parameter_update_callback_enabled on page 445
- set_instance_parameter_value on page 447
6.12.4.7. get_instance_assignment

Description
Returns the assignment value of a child instance. Platform Designer uses assignments
to transfer information about hardware to embedded software tools and applications.

Usage
get_instance_assignment <instance> <assignment>

Returns

String  The value of the specified assignment.

Arguments

instance  The instance name.

assignment  The assignment key to query.

Example

get_instance_assignment video_0 embeddedsw.CMacro.colorSpace

Related Information
get_instance_assignments on page 425
6.12.4.8. get_instance_assignments

**Description**
Returns the list of assignment keys for any defined assignments for the instance.

**Usage**
get_instance_assignments <instance>

**Returns**

`String[]` The list of assignment keys.

**Arguments**

*instance* The instance name.

**Example**

```
get_instance_assignments sdram
```

**Related Information**

*get_instance_assignment* on page 424
6.12.4.9. get_instance_documentation_links

**Description**
Returns the list of all documentation links provided by an instance.

**Usage**
get_instance_documentation_links <instance>

**Returns**

*String[]* The list of documentation links.

**Arguments**

*instance* The instance name.

**Example**

get_instance_documentation_links cpu_0

**Notes**
The list of documentation links includes titles and URLs for the links. For instance, a component with a single data sheet link may return:

{Data Sheet} {http://url/to/data/sheet}
6.12.4.10. get_instance_interface_assignment

**Description**
Returns the assignment value for an interface of a child instance. Platform Designer uses assignments to transfer information about hardware to embedded software tools and applications.

**Usage**
geret_instance_interface_assignment <instance> <interface> <assignment>

**Returns**
String  The value of the specified assignment.

**Arguments**

*instance*  The child instance name.

*interface*  The interface name.

*assignment*  The assignment key to query.

**Example**
get_instance_interface_assignment sdram s1 embeddedsw.configuration.isFlash

**Related Information**
get_instance_interface_assignments on page 428
6.12.4.11. get_instance_interface_assignments

**Description**
Returns the list of assignment keys for any assignments defined for an interface of a child instance.

**Usage**
```
get_instance_interface_assignments <instance> <interface>
```

**Returns**
`String[]` The list of assignment keys.

**Arguments**

*instance* The child instance name.

*interface* The interface name.

**Example**
```
get_instance_interface_assignments sdram s1
```

**Related Information**
`get_instance_interface_assignment` on page 427
6.12.4.12. get_instance_interface_parameter_property

Description
Returns the property value for a parameter in an interface of an instance. Parameter properties are metadata about how Platform Designer uses the parameter.

Usage
get_instance_interface_parameter_property <instance> <interface> <parameter> <property>

Returns
various The parameter property value.

Arguments
instance The child instance name.
interface The interface name.
parameter The parameter name for the interface.
property The property name for the parameter. Refer to Parameter Properties.

Example
get_instance_interface_parameter_property uart_0 s0 setupTime ENABLED

Related Information
- get_instance_interface_parameters on page 431
- get_instance_interfaces on page 436
- get_parameter_properties on page 556
- Parameter Properties on page 575
6.12.4.13. get_instance_interface_parameter_value

**Description**
Returns the parameter value of an interface in an instance.

**Usage**

```
get_instance_interface_parameter_value <instance> <interface> <parameter>
```

**Returns**

*various*  The parameter value.

**Arguments**

*instance*  The child instance name.

*interface*  The interface name.

*parameter*  The parameter name for the interface.

**Example**

```
get_instance_interface_parameter_value uart_0 s0 setupTime
```

**Related Information**

- *get_instance_interface_parameters* on page 431
- *get_instance_interfaces* on page 436
6.12.4.14. get_instance_interface_parameters

**Description**
Returns the list of parameters for an interface in an instance.

**Usage**
get_instance_interface_parameters <instance> <interface>

**Returns**

*String[]* The list of parameter names for parameters in the interface.

**Arguments**

- **instance** The child instance name.
- **interface** The interface name.

**Example**

```
get_instance_interface_parameters uart_0 s0
```

**Related Information**
- [get_instance_interface_parameter_value](#) on page 430
- [get_instance_interfaces](#) on page 436
6.12.4.15. get_instance_interface_port_property

**Description**
Returns the property value of a port in the interface of a child instance.

**Usage**
get_instance_interface_port_property <instance> <interface> <port> <property>

**Returns**

`various` The port property value.

**Arguments**

`instance` The child instance name.

`interface` The interface name.

`port` The port name.

`property` The property name of the port. Refer to Port Properties.

**Example**

get_instance_interface_port_property uart_0 exports tx WIDTH

**Related Information**

- get_instance_interface_ports on page 433
- get_port_properties on page 536
- Port Properties on page 579
6.12.4.16. get_instance_interface_ports

Description
Returns the list of ports in an interface of an instance.

Usage
get_instance_interface_ports <instance> <interface>

Returns
String[] The list of port names in the interface.

Arguments

instance  The instance name.

interface  The interface name.

Example
get_instance_interface_ports uart_0 s0

Related Information
- get_instance_interface_port_property on page 432
- get_instance_interfaces on page 436
6.12.4.17. get_instance_interface_properties

**Description**
Returns the list of properties that you can query for an interface in an instance.

**Usage**
get_instance_interface_properties

**Returns**

*String[]* The list of property names.

**Arguments**
No arguments.

**Example**

```
get_instance_interface_properties
```

**Related Information**
- `get_instance_interface_property` on page 435
- `get_instance_interfaces` on page 436
6.12.4.18. get_instance_interface_property

Description
Returns the property value for an interface in a child instance.

Usage
get_instance_interface_property <instance> <interface> <property>

Returns
String  The property value.

Arguments
instance  The child instance name.

interface  The interface name.

property  The property name. Refer to Element Properties.

Example
get_instance_interface_property uart_0 s0 DESCRIPTION

Related Information
- get_instance_interface_properties on page 434
- get_instance_interfaces on page 436
- Element Properties on page 570
6.12.4.19. get_instance_interfaces

**Description**
Returns the list of interfaces in an instance.

**Usage**
get_instance_interfaces <instance>

**Returns**

```
String[]   The list of interface names.
```

**Arguments**

`instance`   The instance name.

**Example**

```
get_instance_interfaces uart_0
```

**Related Information**

- `get_instance_interface_ports` on page 433
- `get_instance_interface_properties` on page 434
- `get_instance_interface_property` on page 435
6.12.4.20. **get_instance_parameter_property**

**Description**
Returns the property value of a parameter in an instance. Parameter properties are metadata about how Platform Designer uses the parameter.

**Usage**
get_instance_parameter_property <instance> <parameter> <property>

**Returns**

various  The parameter property value.

**Arguments**

instance  The instance name.

parameter  The parameter name.

property  The property name of the parameter. Refer to Parameter Properties.

**Example**
get_instance_parameter_property uart_0 baudRate ENABLED

**Related Information**
- get_instance_parameters on page 440
- get_parameter_properties on page 556
- Parameter Properties on page 575
6.12.4.21. get_instance_parameter_value

Description
Returns the parameter value in a child instance.

Usage
get_instance_parameter_value <instance> <parameter>

Returns
various  The parameter value.

Arguments
instance  The instance name.

parameter  The parameter name.

Example
get_instance_parameter_value pixel_converter input_DPI

Related Information
• get_instance_parameters on page 440
• set_instance_parameter_value on page 447
6.12.4.22. get_instance_parameter_values

**Description**
Returns a list of the parameters' values in a child instance.

**Usage**
get_instance_parameter_values <instance> <parameters>

**Returns**
[String[]]  A list of the parameters' value.

**Arguments**

*instance*  The child instance name.

*parameter*  A list of parameter names in the instance.

**Example**
get_instance_parameter_value uart_0 [list param1 param2]

**Related Information**
- get_instance_parameters on page 440
- set_instance_parameter_value on page 447
- set_instance_parameter_values on page 448
6.12.4.23. get_instance_parameters

Description
Returns the names of all parameters for a child instance that the parent can manipulate. This command omits derived parameters and parameters that have the SYSTEM_INFO parameter property set.

Usage
get_instance_parameters <instance>

Returns
instance The list of parameters in the instance.

Arguments
instance The instance name.

Example
get_instance_parameters uart_0

Related Information
• get_instance_parameter_property on page 437
• get_instance_parameter_value on page 438
• set_instance_parameter_value on page 447
6.12.4.24. get_instance_port_property

**Description**
Returns the property value of a port contained by an interface in a child instance.

**Usage**
get_instance_port_property <instance> <port> <property>

**Returns**

*various*  The property value for the port.

**Arguments**

*instance*  The child instance name.

*port*  The port name.

*property*  The property name. Refer to Port Properties.

**Example**

get_instance_port_property uart_0 tx WIDTH

**Related Information**

- get_instance_interface_ports on page 433
- get_port_properties on page 536
- Port Properties on page 579
6.12.4.25. get_instance_properties

**Description**
Returns the list of properties for a child instance.

**Usage**
get_instance_properties

**Returns**

*String[]*  The list of property names for the child instance.

**Arguments**
No arguments.

**Example**

```sh
get_instance_properties
```

**Related Information**

*get_instance_property* on page 443
6.12.4.26. get_instance_property

**Description**

Returns the property value for a child instance.

**Usage**

get_instance_property <instance> <property>

**Returns**

*String*  The property value.

**Arguments**

*instance*  The child instance name.

*property*  The property name. Refer to *Element Properties*.

**Example**

```
get_instance_property uart_0 ENABLED
```

**Related Information**

-  `get_instance_properties` on page 442
-  *Element Properties* on page 570
6.12.4.27. get_instances

Description
Returns the list of the instance names for all the instances in the system.

Usage
get_instances

Returns

String[] The list of child instance names.

Arguments
No arguments.

Example

get_instances

Related Information
- add_instance on page 418
- remove_instance on page 446
6.12.4.28. is_instance_parameter_update_callback_enabled

Description
Returns true if you enable the update callback for instance parameters.

Usage
is_instance_parameter_update_callback_enabled

Returns
boolean  1 if you enable the callback; 0 if you disable the callback.

Arguments
No arguments

Example
is_instance_parameter_update_callback_enabled

Related Information
enable_instance_parameter_update_callback on page 423
6.12.4.29. remove_instance

Description
Removes an instance from the system.

Usage
remove_instance <instance>

Returns
No return value.

Arguments

instance  The child instance name to remove.

Example

remove_instance cpu

Related Information
- add_instance on page 418
- get_instances on page 444
6.12.4.30. set_instance_parameter_value

Description
Sets the parameter value for a child instance. You cannot set derived parameters and SYSTEM_INFO parameters for the child instance with this command.

Usage
set_instance_parameter_value <instance> <parameter> <value>

Returns
No return value.

Arguments

instance The child instance name.

parameter The parameter name.

value The parameter value.

Example

set_instance_parameter_value uart_0 baudRate 9600

Related Information

- get_instance_parameter_value on page 438
- get_instance_parameter_property on page 437
6.12.4.31. set_instance_parameter_values

Description
Sets a list of parameter values for a child instance. You cannot set derived parameters and SYSTEM_INFO parameters for the child instance with this command.

Usage
set_instance_parameter_value <instance> <parameter_value_pairs>

Returns
No return value.

Arguments

instance  The child instance name.

parameter_value_pairs  The pairs of parameter name and value to set.

Example
set_instance_parameter_value uart_0 [list baudRate 9600 parity odd]

Related Information
- get_instance_parameter_value on page 438
- get_instance_parameter_values on page 439
- get_instance_parameters on page 440
6.12.4.32. set_instance_property

**Description**
Sets the property value of a child instance. Most instance properties are read-only and can only be set by the instance itself. The primary use for this command is to update the ENABLED parameter, which includes or excludes a child instance when generating Platform Designer interconnect.

**Usage**
set_instance_property <instance> <property> <value>

**Returns**
No return value.

**Arguments**

*instance*  The child instance name.

*property*  The property name. Refer to Instance Properties.

*value*  The property value.

**Example**

```
set_instance_property cpu ENABLED false
```

**Related Information**
- get_instance_parameters on page 440
- get_instance_property on page 443
- Instance Properties on page 571
6.12.5. Instantiations

This section lists the commands that allow you to manipulate the loaded instantiations in a Platform Designer system.

add_instantiation_hdl_file on page 452
add_instantiation_interface on page 453
add_instantiation_interface_port on page 454
copy_instance_interface_to_instantiation on page 455
get_instantiation_assignment_value on page 456
get_instantiation_assignments on page 457
get_instantiation_hdl_file_properties on page 458
get_instantiation_hdl_file_property on page 459
get_instantiation_hdl_files on page 460
get_instantiation_interface_assignment_value on page 461
get_instantiation_interface_assignments on page 462
get_instantiation_interface_parameter_value on page 463
get_instantiation_interface_parameters on page 464
get_instantiation_interface_port_properties on page 465
get_instantiation_interface_port_property on page 466
get_instantiation_interface_ports on page 467
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get_instantiation_interface_properties on page 469
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load_instantiation on page 477
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set_instantiation_hdl_file_property on page 483
set_instantiation_interface_assignment_value on page 484
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set_instantiation_interface_port_property on page 486
set_instantiation_interface_sysinfo_parameter_value on page 487
set_instantiation_property on page 488
6.12.5.1. add_instantiation_hdl_file

**Description**
Adds an HDL file to the loaded instantiation.

**Usage**
add_instantiation_hdl_file <file> [kind]

**Returns**
No return value.

**Arguments**

*file*  Specifies the HDL file name.

*kind* (optional)  Indicates the file set kind to add the file to. If you do not specify this option, the command adds the file to all the file sets. Refer to File Set Kind.

**Example**
add_instantiation_hdl_file my_nios2_gen2.vhdl quartus_synth

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- File Set Kind on page 586
6.12.5.2. add_instantiation_interface

**Description**
Adds an interface to the loaded instantiation.

**Usage**
```
add_instantiation_interface <interface> <type> <direction>
```

**Returns**
No return value.

**Arguments**
- **interface**  Specifies the interface name.
- **type**  Specifies the interface type.
- **direction**  Specifies the interface direction. Refer to Interface Direction.

**Example**
```
add_instantiation_interface clk_0 clock OUTPUT
```

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- Interface Direction on page 585
6.12.5.3. add_instantiation_interface_port

**Description**
Adds a port to a loaded instantiation's interface.

**Usage**

```
add_instantiation_interface_port <interface> <port> <role> <width> <vhdl_type><direction>
```

**Returns**
No return value.

**Arguments**

- `interface`  Specifies the interface name.
- `port`  Specifies the port name.
- `role`  Specifies the port role.
- `width`  Specifies the port width.
- `vhdl_type`  Specifies the VHDL type of the port. Refer to VHDL Type.
- `direction`  Specifies the port direction. Refer to Direction Properties.

**Example**

```
add_instantiation_interface_port avs_s0 avs_s0_address address 8 {standard logic vector} input
```

**Related Information**

- load_instantiation on page 477
- save_instantiation on page 481
- VHDL Type on page 593
- Direction Properties on page 569
6.12.5.4. copy_instance_interface_to_instantiation

Description
Adds an interface to a loaded instantiation by copying the specified interface of another instance.

Usage
copy_instance_interface_to_instantiation <instance> <interface> <type>

Returns
String  The name of the newly added interface.

Arguments
instance  Specifies the name of the instance to copy the interface from.

interface  Specifies the name of the interface to copy.

type  Specifies the type of copy to make. Refer to Instantiation Interface Duplicate Type.

Example
copy_instance_interface_to_instantiation cpu_0 data_master CLONE

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
- Instantiation Interface Duplicate Type on page 589
6.12.5.5. get_instantiation_assignment_value

Description
Gets the assignment value on the loaded instantiation.

Usage
get_instantiation_assignment_value <name>

Returns

String  The assignment value.

Arguments

name  Specifies the name of the assignment to get the value of.

Example

get_instantiation_assignment_value embeddedsw.configuration.exceptionOffset

Related Information

• load_instantiation on page 477
• save_instantiation on page 481
6.12.5.6. get_instantiation_assignments

**Description**
Gets the assignment names in the loaded instantiation.

**Usage**
geq_get_instantiation_assignments\

**Returns**

`String[]` The list of assignment names.

**Arguments**
No arguments

**Example**

```
geq_get_instantiation_assignments
```

**Related Information**

- `load_instantiation` on page 477
- `save_instantiation` on page 481
6.12.5.7. get_instantiation_hdl_file_properties

**Description**
Returns the list of properties in an HDL file associated with an instantiation.

**Usage**
get_instantiation_hdl_file_properties

**Returns**
String[] The list of property names.

**Arguments**
No arguments

**Example**
get_instantiation_hdl_file_properties

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.8. get_instantiation_hdl_file_property

Description
Returns the property value of an HDL file associated with the loaded instantiation.

Usage
get_instantiation_hdl_file_property <file> <property>

Returns
various The property value.

Arguments
file Specifies the HDL file name.

property Specifies the property name. Refer to Instantiation Hdl File Properties.

Example
get_instantiation_hdl_file_property my_nios2_gen2.vhdl OUTPUT_PATH

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
- Instantiation HDL File Properties on page 588
6.12.5.9. get_instantiation_hdl_files

**Description**
Returns the list of HDL files of the loaded instantiation.

**Usage**
get_instantiation_hdl_files [<kind>]

**Returns**

String[]  The list of HDL file names.

**Arguments**

kind (optional)  Specifies the file set kind to get the files of. If you do not specify this option, the command gets the QUARTUS_SYNTH files. Refer to *File Set Kind*.

**Example**

get_instantiation_hdl_files quartus_synth

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- File Set Kind on page 586
6.12.5.10. get_instantiation_interface_assignment_value

Description
Gets the assignment value of the loaded instantiation's interface.

Usage
get_instantiation_interface_assignment_value <interface> <name>

Returns
String  The assignment value

Arguments
interface  Specifies the interface name.

name  Specifies the assignment name to get the value of.

Example
get_instantiation_interface_assignment_value avs_s0
embeddedsw.configuration.exceptionOffset

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.11. get_instantiation_interface_assignments

Description
Gets the assignment names of the loaded instantiation's interface.

Usage
get_instantiation_interface_assignments <interface>

Returns
String[]  The list of assignment names.

Arguments
interface  Specifies the interface name.

Example
get_instantiation_interface_assignments avs_s0

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.12. get_instantiation_interface_parameter_value

Description
Returns the parameter value of a loaded instantiation's interface.

Usage
get_instantiation_interface_parameter_value <interface> <parameter>

Returns
String  The parameter value.

Arguments
interface  Specifies the interface name.

parameter  Specifies the parameter name.

Example
get_instantiation_interface_parameter_value avs_s0 associatedClock

Related Information
- get_instantiation_interface_parameters on page 464
- set_instantiation_interface_parameter_value on page 485
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.13. get_instantiation_interface_parameters

**Description**
Returns the list of parameters of an instantiation's interface.

**Usage**
get_instantiation_interface_parameters <interface>

**Returns**

String[] The list of parameter names.

**Arguments**

interface Specifies the interface name.

**Example**

get_instantiation_interface_parameters avs_s0

**Related Information**

- load_instantiation on page 477
- save_instantiation on page 481
- get_instantiation_interface_parameter_value on page 463
- set_instantiation_interface_parameter_value on page 485
6.12.5.14. get_instantiation_interface_port_properties

**Description**
Returns the list of port properties of an instantiation's interface.

**Usage**
get_instantiation_interface_port_properties

**Returns**

*String[]*  The list of port properties.

**Arguments**
No arguments

**Example**

```
get_instantiation_interface_port_properties
```

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.15. **get_instantiation_interface_port_property**

**Description**
Returns the port property value of a loaded instantiation's interface.

**Usage**
get_instantiation_interface_port_property <interface> <port> <property>

**Returns**

*various*  The property value.

**Arguments**

*interface*  Specifies the interface name.

*port*  Specifies the port name.

*property*  Specifies the property name. Refer to *Port Properties*.

**Example**
get_instantiation_interface_port_property avs_s0 avs_s0_address WIDTH

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- Port Properties on page 592
6.12.5.16. get_instantiation_interface_ports

Description
Returns the list of ports of the loaded instantiation’s interface.

Usage
get_instantiation_interface_ports <interface>

Returns
String[] The list of port names.

Arguments
interface Specifies the interface name.

Example
get_instantiation_interface_ports avs_s0

Related Information
• load_instantiation on page 477
• save_instantiation on page 481
6.12.5.17. get_instantiation_interface_property

**Description**
Returns the value of a single interface property from the specified instantiation interface.

**Usage**
get_instantiation_interface_property <interface> <property>

**Returns**

*various*  The property value.

**Arguments**

*interface*  The interface name on the currently loaded interface.

*property*  The property name. Refer to *Instantiation Interface Properties*.

**Example**

```
get_instantiation_interface_property in_clk TYPE
```

**Related Information**

- *get_instantiation_interface_properties* on page 469
- *load_instantiation* on page 477
- *Instantiation Interface Properties* on page 590
6.12.5.18. get_instantiation_interface_properties

Description
Returns the names of all the available instantiation interface properties, common to all interface types.

Usage
get_instantiation_interface_properties

Returns
String[]  A list of instantiation interface properties.

Arguments
No arguments.

Example
get_instantiation_interface_properties

Related Information
get_instantiation_interface_property on page 468
6.12.5.19. get_instantiation_interface_sysinfo_parameter_value

Description
Gets the system info parameter value for a loaded instantiation's interface.

Usage
get_instantiation_interface_sysinfo_parameter_value <interface> <parameter>

Returns
various The system info property value.

Arguments
interface Specifies the interface name.

parameter Specifies the system info parameter name. Refer to System Info Type.

Example
get_instantiation_interface_sysinfo_parameter_value debug_mem_slave max_slave_data_width

Related Information
- get_instantiation_interface_sysinfo_parameters on page 471
- set_instantiation_interface_sysinfo_parameter_value on page 487
- System Info Type Properties on page 581
6.12.5.20. get_instantiation_interface_sysinfo_parameters

**Description**
Returns the list of system info parameters for the loaded instantiation's interface.

**Usage**
get_instantiation_interface_sysinfo_parameters <interface> [<type>]

**Returns**
String[] The list of system info parameter names.

**Arguments**

*interface* Specifies the interface name.

*type (optional)* Specifies the parameters type to return. If you do not specify this option, the command returns all the parameters. Refer to Access Type.

**Example**
get_instantiation_interface_sysinfo_parameters debug_mem_slave

**Related Information**
- get_instantiation_interface_sysinfo_parameter_value on page 470
- set_instantiation_interface_sysinfo_parameter_value on page 487
- Access Type on page 587
6.12.5.21. get_instantiation_interfaces

**Description**
Returns the list of interfaces for the loaded instantiation.

**Usage**
get_instantiation_interfaces

**Returns**

*String[]* The list of interface names.

**Arguments**
No arguments.

**Example**

get_instantiation_interfaces

**Related Information**
- [load_instantiation](#) on page 477
- [save_instantiation](#) on page 481
6.12.5.22. get_instantiation_properties

**Description**
Returns the list of properties for the loaded instantiation.

**Usage**
get_instantiation_properties

**Returns**

*String[]*  The list of property names.

**Arguments**
No arguments.

**Example**

<table>
<thead>
<tr>
<th>get_instantiation_properties</th>
</tr>
</thead>
</table>

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.23. get_instantiation_property

**Description**
Returns the value of the specified property for the loaded instantiation.

**Usage**
get_instantiation_property <property>

**Returns**

*various*  The value of an instantiation property.

**Arguments**

*property*  Specifies the property name to get the value of. Refer to *Instantiation Properties*.

**Example**

```
get_instantiation_property HDL_ENTITY_NAME
```

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- Instantiation Properties on page 591
6.12.5.24. get_loaded_instantiation

Description
Returns the instance name of the loaded instantiation.

Usage
get_loaded_instantiation

Returns

String  The instance name.

Arguments
No arguments

Example
get_loaded_instantiation

Related Information
•  load_instantiation on page 477
•  save_instantiation on page 481
6.12.5.25. import_instantiation_interfaces

Description
Sets the interfaces of a loaded instantiation by importing the interfaces from the specified file.

Usage
import_instantiation_interfaces <file>

Returns
No return value

Arguments

<file> Specifies the IP or IP-XACT file to import the interfaces from.

Example
import_instantiation_interfaces ip/my_system/my_system_nios2_gen2_0.ip

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.26. load_instantiation

**Description**
Loads the instantiation of an instance, so that you can modify the instantiation if necessary.

**Usage**
load_instantiation <instance>

**Returns**
boolean  1 if successful; 0 if unsuccessful.

**Arguments**

instancename  Specifies the instance name.

**Example**

load_instantiation cpu

**Related Information**
save_instantiation on page 481
6.12.5.27. `remove_instantiation_hdl_file`

**Description**
Removes an HDL file from the loaded instantiation.

**Usage**
```
remove_instantiation_hdl_file <file> [kind]
```

**Returns**
No return value.

**Arguments**
- `file` Specifies the HDL file name.

- `kind (optional)` Specifies the kind of file set to remove the file from. If you do not specify this option, the command removes the file from all the file sets. Refer to `File Set Kind`.

**Example**
```
remove_instantiation_hdl_file my_nios2_gen2.vhdl quartus_synth
```

**Related Information**
- `load_instantiation` on page 477
- `save_instantiation` on page 481
- `File Set Kind` on page 586
6.12.5.28. remove_instantiation_interface

**Description**
Removes an interface from a loaded instantiation.

**Usage**
remove_instantiation_interface <interface>

**Returns**
No return value

**Arguments**

*interface*  Specifies the interface name.

**Example**
remove_instantiation_interface avs_s0

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.5.29. remove_instantiation_interface_port

Description
Removes a port from a loaded instantiation's interface.

Usage
remove_instantiation_interface_port <interface> <port>

Returns
No return value

Arguments

interface  Specifies the interface name.

port      Specifies the port name.

Example
remove_instantiation_interface_port avs_s0 avs_s0_address

Related Information
• load_instantiation on page 477
• save_instantiation on page 481
6.12.5.30. **save_instantiation**

**Description**
Saves the loaded instantiation.

**Usage**
save_instantiation

**Returns**
No return value

**Arguments**
No arguments

**Example**

```bash
save_instantiation
```

**Related Information**
load_instantiation on page 477
6.12.5.31. set_instantiation_assignment_value

**Description**
Sets the assignment value for the loaded instantiation.

**Usage**
```
set_instantiation_assignment_value <name> [value]
```

**Returns**
No return value

**Arguments**

- **instance**  Specifies the assignment name to set value for.

- **value (optional)**  Specifies the assignment value. If you do not specify this option, the command removes the assignment.

**Example**
```
set_instantiation_assignment_value embeddedsw.configuration.exceptionOffset 32
```

**Related Information**
`get_instantiation_assignment_value` on page 456
6.12.5.32. set_instantiation_hdl_file_property

**Description**
Sets the property value for an HDL file associated with a loaded instantiation.

**Usage**
```
set_instantiation_hdl_file_property <file> <property> <value>
```

**Returns**
No return value

**Arguments**
- **file**  Specifies the HDL file name.
- **property**  Specifies the property name. Refer to *Instantiation Hdl File Properties*.
- **value**  Specifies the property value.

**Example**
```
set_instantiation_hdl_file_property my_nios2_gen2.vhdl OUTPUT_PATH
my_nios2_gen2.vhdl
```

**Related Information**
- [load_instantiation](#) on page 477
- [save_instantiation](#) on page 481
- [Instantiation HDL File Properties](#) on page 588
6.12.5.33. set_instantiation_interface_assignment_value

**Description**
Sets the assignment value for the loaded instantiation’s interface.

**Usage**
```
set_instantiation_interface_assignment_value <interface> <name> [<value>]
```

**Returns**
No return value

**Arguments**

- `interface` Specifies the interface name.
- `name` Specifies the assignment name to set the value of.
- `value (optional)` Specifies the new assignment value. If you do not specify this value, the command removes the assignment.

**Example**
```
set_instantiation_interface_assignment_value
embeddedsw.configuration.exceptionOffset 32
```

**Related Information**
get_instantiation_assignment_value on page 456
6.12.5.34. set_instantiation_interface_parameter_value

**Description**
Sets the parameter value for the loaded instantiation’s interface.

**Usage**
```sh
set_instantiation_interface_parameter_value <interface> <parameter> <value>
```

**Returns**
No return value

**Arguments**

- **instance**  Specifies the interface name.
- **parameter**  Specifies the parameter name.
- **value**  Specifies the parameter value.

**Example**
```sh
set_instantiation_interface_parameter avs_s0 associatedClock clk
```

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
- get_instantiation_interface_parameter_value on page 463
- get_instantiation_interface_parameters on page 464
6.12.5.35. set_instantiation_interface_port_property

Description
Sets the port property value on a loaded instantiation's interface.

Usage
set_instantiation_interface_port_property <interface> <port> <property> <value>

Returns
No return value

Arguments
interface  Specifies the interface name.
port  Specifies the port name.
property  Specifies the property name. Refer to Port Properties.
value  Specifies the property value.

Example
set_instantiation_interface_port_property avs_s0 avs_s0_address WIDTH 1

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
- Port Properties on page 592
6.12.5.36. set_instantiation_interface_sysinfo_parameter_value

Description
Sets the system info parameter value for the loaded instantiation's interface.

Usage
set_instantiation_interface_sysinfo_parameter_value <interface> <parameter> <value>

Returns
No return value

Arguments

interface  Specifies the interface name.

parameter  Specifies the system info parameter name. Refer to System Info Type.

value  Specifies the system info parameter value.

Example
set_instantiation_interface_sysinfo_parameter_value debug_mem_slave max_slave_data_width 64

Related Information
- get_instantiation_interface_sysinfo_parameter_value on page 470
- get_instantiation_interface_sysinfo_parameters on page 471
- System Info Type Properties on page 581
6.12.5.37. set_instantiation_property

**Description**
Sets the property value for the loaded instantiation.

**Usage**

```
set_instantiation_property <property> <value>
```

**Returns**
No return value

**Arguments**

- **property** Specifies the property name. Refer to [Instantiation Properties](#).
- **value** Specifies the value to set.

**Example**

```
set_instantiation_property HDL_ENTITY_NAME my_system_nios2_gen2_0
```

**Related Information**

- [load_instantiation](#) on page 477
- [save_instantiation](#) on page 481
- [Instantiation Properties](#) on page 591
6.12.6. Components

This section lists the commands that allow you to manipulate the IP components loaded in a Platform Designer system.

apply_component_preset on page 490
get_component_assignment on page 491
get_component_assignments on page 492
get_component_documentation_links on page 493
get_component_interface_assignment on page 494
get_component_interface_assignments on page 495
get_component_interface_parameter_property on page 496
get_component_interface_parameter_value on page 497
get_component_interface_parameters on page 498
get_component_interface_port_property on page 499
get_component_interface_ports on page 500
get_component_interface_property on page 501
get_component_interfaces on page 502
get_component_parameter_property on page 503
get_component_parameter_value on page 504
get_component_parameters on page 505
get_component_project_properties on page 506
get_component_project_property on page 507
get_component_property on page 508
get_loaded_component on page 509
load_component on page 510
reload_component_footprint on page 511
save_component on page 512
set_component_parameter_value on page 513
set_component_project_property on page 514
6.12.6.1. apply_component_preset

Description
Applies the settings in a preset to the loaded component.

Usage
apply_component_preset<preset_name>

Returns
No return value

Arguments

preset_name  Specifies the preset name.

Example
apply_component_preset "Custom Debug Settings"

Related Information
- load_component on page 510
- set_component_parameter_value on page 513
6.12.6.2. get_component_assignment

Description
Returns the assignment value for the loaded component.

Usage
get_component_assignment <assignment>

Returns

String  The specified assignment value.

Arguments

assignment  Specifies the assignment key value to query.

Example

get_component_assignment embeddedsw.CMacro.colorSpace

Related Information

•  load_component on page 510
•  get_component_assignments on page 492
6.12.6.3. get_component_assignments

**Description**
Returns the list of assignment keys for the loaded component.

**Usage**
get_component_assignments

**Returns**

`String[]` The list of assignment keys.

**Arguments**
No arguments

**Example**

```
get_component_assignments
```

**Related Information**
- `get_instance_assignment` on page 424
- `load_component` on page 510
6.12.6.4. get_component_documentation_links

**Description**
Returns the list of all documentation links that the loaded component provides.

**Usage**
get_component_documentation_links

**Returns**

*String[]*  The list of documentation links.

**Arguments**
No arguments

**Example**

get_component_documentation_links

**Related Information**
load_component on page 510
6.12.6.5. get_component_interface_assignment

**Description**
Returns the assignment value of an interface of the loaded component.

**Usage**
get_component_interface_assignment <interface> <assignment>

**Returns**

*String*  The specified assignment value.

**Arguments**

*interface*  Specifies the interface name.

*assignment*  Specifies the assignment key to the query.

**Example**

get_component_interface_assignment s1 embeddedsw.configuration.isFlash

**Related Information**

- get_component_interface_assignments on page 495
- load_component on page 510
6.12.6.6. get_component_interface_assignments

**Description**
Returns the list of assignment keys for any assignments that you define for an interface on the loaded component.

**Usage**
get_component_interface_assignments <interface>

**Returns**

`String[]` The list of assignment keys.

**Arguments**

`interface` Specifies the interface name.

**Example**

| get_component_interface_assignments s1 |

**Related Information**
- `get_component_interface_assignment` on page 494
- `load_component` on page 510
6.12.6.7. get_component_interface_parameter_property

**Description**

Returns the property value of a parameter in a loaded component's interface. Parameter properties are metadata about how the Intel Quartus Prime uses the parameters.

**Usage**

```
get_component_interface_parameter_property <interface> <parameter> <property>
```

**Returns**

*various*  The parameter property value.

**Arguments**

*interface*  Specifies the interface name.

*parameter*  Specifies the parameter name.

*property*  Specifies the parameter property. Refer to *Parameter Properties*.

**Example**

```
get_component_interface_parameter_property s0 setupTime ENABLED
```

**Related Information**

- *get_component_interface_parameters* on page 498
- *get_component_interfaces* on page 502
- *load_component* on page 510
- *Parameter Properties* on page 575
- *get_parameter_properties* on page 556
6.12.6.8. get_component_interface_parameter_value

Description
Returns the parameter value of an interface of the loaded component.

Usage
get_component_interface_parameter_value <interface> <parameter>

Returns
various  The parameter value.

Arguments
interface  Specifies the interface name.

parameter  Specifies the parameter name.

Example
get_component_interface_parameter_value s0 setupTime

Related Information
- get_component_interface_parameters on page 498
- get_component_interfaces on page 502
- load_component on page 510
6.12.6.9. get_component_interface_parameters

**Description**
Returns the list of parameters for an interface of the loaded component.

**Usage**
get_component_interface_parameters `<interface>`

**Returns**

`String[]` The list of parameter names.

**Arguments**

`interface` Specifies the interface name.

**Example**

```
get_component_interface_parameters s0
```

**Related Information**

- `get_component_interface_parameter_value` on page 497
- `get_component_interfaces` on page 502
- `load_component` on page 510
6.12.6.10. get_component_interface_port_property

**Description**
Returns the property value of a port in the interface of the loaded component.

**Usage**
get_component_interface_port_property <interface> <port> <property>

**Returns**

various  The port property value

**Arguments**

interface  Specifies the interface name.

port  Specifies the port name of the interface.

property  Specifies the property name of the port. Refer to Port Properties.

**Example**
get_component_interface_port_property exports tx WIDTH

**Related Information**

- get_component_interface_ports on page 500
- load_component on page 510
- Port Properties on page 592
- get_port_properties on page 536
6.12.6.11. get_component_interface_ports

**Description**

Returns the list of interface ports of the loaded component.

**Usage**

get_component_interface_ports <interface>

**Returns**

*String[]* The list of port names

**Arguments**

*interface* Specifies the interface name.

**Example**

```
get_component_interface_ports s0
```

**Related Information**

- `get_component_interface_port_property` on page 499
- `get_component_interfaces` on page 502
- `load_component` on page 510
6.12.6.12. get_component_interface_property

Description
Returns the value of a single property from the specified interface for the loaded component.

Usage
get_component_interface_property <interface> <property>

Returns
String  The property value.

Arguments

interface  Specifies the interface name.

property  Specifies the property name. Refer to Element Properties.

Example
get_interface_property clk_in DISPLAY_NAME

Related Information
- load_component on page 510
- Element Properties on page 570
- get_interface_properties on page 533
6.12.6.13. get_component_interfaces

**Description**
Returns the list of interfaces in the loaded component.

**Usage**
get_component_interfaces

**Returns**

*String[]* The list of interface names.

**Arguments**
No arguments

**Example**

get_component_interfaces

**Related Information**
- get_component_interface_ports on page 500
- get_component_interface_property on page 501
- load_component on page 510
6.12.6.14. get_component_parameter_property

**Description**
Returns the property value of a parameter in the loaded component.

**Usage**
get_component_parameter_property <parameter> <property>

**Returns**

*Various*  The parameter property value.

**Arguments**

*parameter*  Specifies the parameter name in the component.

*property*  Specifies the property name of the parameter. Refer to *Parameter Properties*.

**Example**

get_component_parameter_property baudRate ENABLED

**Related Information**

- `get_component_parameters` on page 505
- `get_parameter_properties` on page 556
- `load_component` on page 510
- *Parameter Properties* on page 575
6.12.6.15. `get_component_parameter_value`

**Description**
Returns the parameter value in the loaded component.

**Usage**
```
get_component_parameter_value <parameter>
```

**Returns**

*various*  The parameter value

**Arguments**

*parameter*  Specifies the parameter name in the component.

**Example**
```
get_component_parameter_value baudRate
```

**Related Information**
- `get_component_parameters` on page 505
- `load_component` on page 510
- `set_component_parameter_value` on page 513
6.12.6.16. get_component_parameters

Description
Returns the list of parameters in the loaded component.

Usage
get_component_parameters

Returns

String[] The list of parameters in the component.

Arguments
No arguments

Example
get_instance_parameters

Related Information
• get_component_parameter_property on page 503
• get_component_parameter_value on page 504
• load_component on page 510
• set_component_parameter_value on page 513
6.12.6.17. get_component_project_properties

**Description**
Returns the list of properties that you query about the loaded component’s Intel Quartus Prime project.

**Usage**
get_component_project_properties

**Returns**

String[]  The list of project properties.

**Arguments**
No arguments

**Example**

get_component_project_properties

**Related Information**
- get_component_project_property on page 507
- load_component on page 510
- set_component_project_property on page 514
6.12.6.18. get_component_project_property

**Description**
Returns the project property value of the loaded component. Only select project properties are available.

**Usage**
get_component_project_property <property>

**Returns**

*String* The property value.

**Arguments**

*property* Specifies the project property name. Refer to *Project Properties*.

**Example**

```
get_component_project_property HIDE_FROM_IP_CATALOG
```

**Related Information**
- `get_component_project_properties` on page 506
- `load_component` on page 510
- `set_component_project_property` on page 514
- *Project Properties* on page 580
6.12.6.19. get_component_property

**Description**
Returns the property value of the loaded component.

**Usage**
`get_component_property <property>`

**Returns**

*String* The property value.

**Arguments**

`property` The property name on the loaded component. Refer to *Element Properties*.

**Example**

```
get_component_property CLASS_NAME
```

**Related Information**

- `load_component` on page 510
- `get_instance_properties` on page 442
- *Element Properties* on page 570
6.12.6.20. get_loaded_component

Description
Returns the instance name associated with the loaded component.

Usage
get_loaded_component

Returns
String  The instance name.

Arguments
No arguments

Example
get_loaded_component

Related Information
- load_component on page 510
- save_component on page 512
6.12.6.21. load_component

**Description**
Loads the actual component inside of a generic component, so that you can modify the component parameters.

**Usage**
load_component <instance>

**Returns**
boolean  1 if successful; 0 if unsuccessful.

**Arguments**

instance Specifies the instance name.

**Example**
load_component cpu

**Related Information**
- get_loaded_component on page 509
- save_component on page 512
6.12.6.22. reload_component_footprint

Description
Validates the footprint of a specified child instance, and updates the footprint of the instance in case of issues.

Usage
reload_component_footprint [<instance>]

Returns
String[] A list of validation messages.

Arguments

instance (optional) Specifies the child instance name to validate. If you do not specify this option, the command validates all the generic components in the system.

Example
reload_component_footprint cpu_0

Related Information
- load_instantiation on page 477
- save_instantiation on page 481
- validate_component_footprint on page 550
6.12.6.23. `save_component`

**Description**
Saves the loaded component.

**Usage**
```
save_component
```

**Returns**
No return value

**Arguments**
No arguments

**Example**
```
save_component
```

**Related Information**
- `get_loaded_component` on page 509
- `load_component` on page 510
6.12.6.24. set_component_parameter_value

**Description**
Sets the parameter value for the loaded component.

**Usage**
set_component_parameter_value <parameter> <value>

**Returns**
No return value

**Arguments**

- `parameter` Specifies the parameter name.
- `parameter` Specifies the new parameter value.

**Example**
set_component_parameter_value baudRate 9600

**Related Information**
- `get_component_parameter_value` on page 504
- `get_component_parameters` on page 505
- `load_component` on page 510
6.12.6.25. set_component_project_property

**Description**
Sets the project property value of the loaded component, such as hiding from the IP catalog.

**Usage**

```
set_component_project_property <property> <value>
```

**Returns**
No return value

**Arguments**

- `property` Specifies the property name. Refer to *Project Properties*.
- `value` Specifies the new property value.

**Example**

```
set_component_project_property HIDE_FROM_IP_CATALOG false
```

**Related Information**
- `get_component_project_properties` on page 506
- `get_component_project_property` on page 507
- `load_component` on page 510
- *Project Properties* on page 580
6.12.7. Connections

This section lists the commands that allow you to manipulate the interface connections in your Platform Designer system.

add_connection on page 516
auto_connect on page 517
get_connection_parameter_property on page 518
get_connection_parameter_value on page 519
get_connection_parameters on page 520
get_connection_properties on page 521
get_connection_property on page 522
get_connections on page 523
remove_connection on page 524
remove_dangling_connections on page 525
set_connection_parameter_value on page 526
6.12.7.1. add_connection

**Description**
Connects the named interfaces using an appropriate connection type. Both interface names consist of an instance name, followed by the interface name that the module provides.

**Usage**
add_connection <start> [<end>]

**Returns**
No return value.

**Arguments**

- **start**  The start interface that you connect, in `<instance_name>.<interface_name>` format. If you do not specify the end argument, the connection must be of the form `<instance1>.<interface> / <instance2>.<interface>`.

- **end (optional)**  The end interface that you connect, in `<instance_name>.<interface_name>` format.

**Example**
add_connection dma.read_master sdram.s1

**Related Information**
- [get_connection_parameter_value on page 519](#)
- [get_connection_property on page 522](#)
- [get_connections on page 523](#)
- [remove_connection on page 524](#)
- [set_connection_parameter_value on page 526](#)
6.12.7.2. auto_connect

Description
Creates connections from an instance or instance interface to matching interfaces of other instances in the system. For example, Avalon memory mapped slaves connect to Avalon memory mapped masters.

Usage
auto_connect <element>

Returns
No return value.

Arguments

element  The instance interface name, or the instance name.

Example

auto_connect sdram
auto_connect uart_0.s1

Related Information
add_connection on page 516
6.12.7.3. `get_connection_parameter_property`

**Description**
Returns the property value of a parameter in a connection. Parameter properties are metadata about how Platform Designer uses the parameter.

**Usage**
`get_connection_parameter_property <connection> <parameter> <property>`

**Returns**
`various` The parameter property value.

**Arguments**
- `connection` The connection to query.
- `parameter` The parameter name.
- `property` The property of the connection. Refer to `Parameter Properties`.

**Example**
`get_connection_parameter_property cpu.data_master/dma0.csr baseAddress UNITS`

**Related Information**
- `get_connection_parameter_value` on page 519
- `get_connection_property` on page 522
- `get_connections` on page 523
- `get_parameter_properties` on page 556
- `Parameter Properties` on page 575
6.12.7.4. get_connection_parameter_value

Description
Returns the parameter value of the connection. Parameters represent aspects of the connection that you can modify, such as the base address for an Avalon memory mapped connection.

Usage
get_connection_parameter_value <connection> <parameter>

Returns

various  The parameter value.

Arguments

classification  The connection to query.

parameter  The parameter name.

Example

get_connection_parameter_value cpu.data_master/dma0.csr baseAddress

Related Information
- get_connection_parameters on page 520
- get_connections on page 523
- set_connection_parameter_value on page 526
6.12.7.5. get_connection_parameters

**Description**
Returns the list of parameters of a connection.

**Usage**
get_connection_parameters <connection>

**Returns**
String[]  The list of parameter names.

**Arguments**
connection  The connection to query.

**Example**
```
get_connection_parameters cpu.data_master/dma0.csr
```

**Related Information**
- get_connection_parameter_property on page 518
- get_connection_parameter_value on page 519
- get_connection_property on page 522
6.12.7.6. get_connection_properties

Description
Returns the properties list of a connection.

Usage
get_connection_properties

Returns

String[] The list of connection properties.

Arguments
No arguments.

Example

get_connection_properties

Related Information
• get_connection_property on page 522
• get_connections on page 523
6.12.7.7. get_connection_property

**Description**
Returns the property value of a connection. Properties represent aspects of the connection that you can modify, such as the connection type.

**Usage**
get_connection_property <connection> <property>

**Returns**

*String*  The connection property value.

**Arguments**

*connection*  The connection to query.

*property*  The connection property name. Refer to *Connection Properties*.

**Example**

get_connection_property cpu.data_master/dma0.csr TYPE

**Related Information**

- get_connection_properties on page 521
- Connection Properties on page 567
6.12.7.8. get_connections

Description
Returns the list of all connections in the system if you do not specify any element. If you specify a child instance, for example cpu, Platform Designer returns all connections to any interface on the instance. If you specify an interface of a child instance, for example cpu.instruction_master, Platform Designer returns all connections to that interface.

Usage
get_connections [ <element> ]

Returns
String[] The list of connections.

Arguments

element (optional) The child instance name, or the qualified interface name on a child instance.

Example

get_connections
get_connections cpu
get_connections cpu.instruction_master

Related Information

• add_connection on page 516
• remove_connection on page 524
6.12.7.9. remove_connection

**Description**
Removes a connection from the system.

**Usage**
remove_connection <connection>

**Returns**
No return value.

**Arguments**

*connection*  The connection name to remove.

**Example**
remove_connection cpu.data_master/sdram.s0

**Related Information**
- [add_connection](#) on page 516
- [get_connections](#) on page 523
6.12.7.10. remove_dangling_connections

Description
Removes connections where both end points of the connection no longer exist in the system.

Usage
remove_dangling_connections

Returns
No return value.

Arguments
No arguments.

Example
remove_dangling_connections

Related Information
- add_connection on page 516
- get_connections on page 523
- remove_connection on page 524
6.12.7.11. set_connection_parameter_value

**Description**
Sets the parameter value for a connection.

**Usage**
set_connection_parameter_value <connection> <parameter> <value>

**Returns**
No return value.

**Arguments**
- **connection**  The connection name.
- **parameter**   The parameter name.
- **value**       The new parameter value.

**Example**
```
set_connection_parameter_value cpu.data_master/dma0.csr baseAddress "0x000a0000"
```

**Related Information**
- [get_connection_parameter_value](#) on page 519
- [get_connection_parameters](#) on page 520
6.12.8. Top-level Exports

This section lists the commands that allow you to manipulate the exported interfaces in your Platform Designer system.

- `add_interface` on page 528
- `get_exported_interface_sysinfo_parameter_value` on page 529
- `get_exported_interface_sysinfo_parameters` on page 530
- `get_interface_port_property` on page 531
- `get_interface_ports` on page 532
- `get_interface_properties` on page 533
- `get_interface_property` on page 534
- `get_interfaces` on page 535
- `get_port_properties` on page 536
- `remove_interface` on page 537
- `set_exported_interface_sysinfo_parameter_value` on page 538
- `set_interface_port_property` on page 539
- `set_interface_property` on page 540
6.12.8.1. add_interface

**Description**
Adds an interface to your system, which Platform Designer uses to export an interface from within the system. You specify the exported internal interface with `set_interface_property <interface> EXPORT_OF instance.interface`.

**Usage**
`add_interface <name> <type> <direction>`. 

**Returns**
No return value.

**Arguments**
- **name** The name of the interface that Platform Designer exports from the system.
- **type** The type of interface.
- **direction** The interface direction.

**Example**
```
add_interface my_export conduit end
set_interface_property my_export EXPORT_OF uart_0.external_connection
```

**Related Information**
- `get_interface_ports` on page 532
- `get_interface_properties` on page 533
- `get_interface_property` on page 534
- `set_interface_property` on page 540
6.12.8.2. get_exported_interface_sysinfo_parameter_value

**Description**
Gets the value of a system info parameter for an exported interface.

**Usage**
get_exported_interface_sysinfo_parameter_value <interface> <parameter>

**Returns**

`various` The system info parameter value.

**Arguments**

`interface` Specifies the name of the exported interface.

`parameter` Specifies the name of the system info parameter. Refer to System Info Type.

**Example**

```bash
get_exported_interface_sysinfo_parameter_value clk clock_rate
```

**Related Information**

- `get_exported_interface_sysinfo_parameters` on page 530
- `set_exported_interface_sysinfo_parameter_value` on page 538
- `System Info Type Properties` on page 581
6.12.8.3. get_exported_interface_sysinfo_parameters

Description
Returns the list of system info parameters for an exported interface.

Usage
get_exported_interface_sysinfo_parameters <interface> [<<type>>]

Returns

String[]  The list of system info parameter names.

Arguments

interface  Specifies the name of the exported interface.

type (optional)  Specifies the parameters type to return. If you do not specify this option, the command returns all the parameters. Refer to Access Type.

Example

get_exported_interface_sysinfo_parameters clk

Related Information
- get_exported_interface_sysinfo_parameter_value on page 529
- set_exported_interface_sysinfo_parameter_value on page 538
- Access Type on page 587
6.12.8.4. get_interface_port_property

**Description**
Returns the value of a property of a port contained by one of the top-level exported interfaces.

**Usage**
get_interface_port_property <interface> <port> <property>

**Returns**

*various*  The property value.

**Arguments**

*interface*  The name of a top-level interface of the system.

*port*  The port name in the interface.

*property*  The property name on the port. Refer to *Port Properties*.

**Example**
get_interface_port_property uart_exports tx DIRECTION

**Related Information**
- get_interface_ports on page 532
- get_port_properties on page 536
- Port Properties on page 579
6.12.8.5. get_interface_ports

**Description**
Returns the names of all the added ports to a given interface.

**Usage**
get_interface_ports <interface>

**Returns**

String[] The list of port names.

**Arguments**

interface The top-level interface name of the system.

**Example**

get_interface_ports export_clk_out

**Related Information**

- [get_interface_port_property](#) on page 531
- [get_interfaces](#) on page 535
6.12.8.6. get_interface_properties

**Description**
Returns the names of all the available interface properties common to all interface types.

**Usage**
get_interface_properties

**Returns**

String[] The list of interface properties.

**Arguments**
No arguments.

**Example**

get_interface_properties

**Related Information**
- get_interface_property on page 534
- set_interface_property on page 540
6.12.8.7. get_interface_property

**Description**
Returns the value of a single interface property from the specified interface.

**Usage**
ge\_get_interface_property <\textit{interface}> <\textit{property}>

**Returns**

\textit{various}  The property value.

**Arguments**

\textit{interface}  The name of a top-level interface of the system.

\textit{property}  The name of the property. Refer to \textit{Interface Properties}.

**Example**

get\_interface\_property export\_clk\_out EXPORT\_OF

**Related Information**

- get\_interface\_properties on page 533
- set\_interface\_property on page 540
- Interface Properties on page 572
6.12.8.8. get_interfaces

**Description**
Returns the list of top-level interfaces in the system.

**Usage**
get_interfaces

**Returns**

`String[]` The list of the top-level interfaces exported from the system.

**Arguments**
No arguments.

**Example**

```java
get_interfaces
```

**Related Information**
- `add_interface` on page 528
- `get_interface_ports` on page 532
- `get_interface_property` on page 534
- `remove_interface` on page 537
- `set_interface_property` on page 540
6.12.8.9. get_port_properties

Description
Returns the list of properties that you can query for ports.

Usage
get_port_properties

Returns
String[] The list of port properties.

Arguments
No arguments.

Example
get_port_properties

Related Information
- get_instance_interface_port_property on page 432
- get_instance_interface_ports on page 433
- get_instance_port_property on page 441
- get_interface_port_property on page 531
- get_interface_ports on page 532
6.12.8.10. remove_interface

Description
Removes an exported top-level interface from the system.

Usage
remove_interface <interface>

Returns
No return value.

Arguments

interface  The name of the exported top-level interface.

Example

remove_interface clk_out

Related Information
• add_interface on page 528
• get_interfaces on page 535
6.12.8.11. set_exported_interface_sysinfo_parameter_value

**Description**
Sets the system info parameter value for an exported interface.

**Usage**
set_exported_interface_sysinfo_parameter_value <interface> <parameter> <value>

**Returns**
No return value

**Arguments**

*interface*  Specifies the name of the exported interface.

*parameter*  Specifies the name of the system info parameter. Refer to System Info Type.

*value*  Specifies the system info parameter value.

**Example**
set_exported_interface_sysinfo_parameter_value clk clock_rate 5000000

**Related Information**
- get_exported_interface_sysinfo_parameter_value on page 529
- get_exported_interface_sysinfo_parameters on page 530
- System Info Type Properties on page 581
6.12.8.12. set_interface_port_property

**Description**
Sets the port property in a top-level interface of the system.

**Usage**

```
set_interface_port_property <interface> <port> <property> <value>
```

**Returns**
No return value

**Arguments**

- `interface`  Specifies the top-level interface name of the system.
- `port`  Specifies the port name in a top-level interface of the system.
- `property`  Specifies the property name of the port. Refer to *Port Properties*.
- `value`  Specifies the property value.

**Example**

```
set_interface_port_property clk clk_clk NAME my_clk
```

**Related Information**

- *Port Properties* on page 592
- `get_interface_ports` on page 532
- `get_interfaces` on page 535
- `get_port_properties` on page 536
6.12.8.13. set_interface_property

**Description**
Sets the value of a property on an exported top-level interface. You use this command to set the EXPORT_OF property to specify which interface of a child instance is exported via this top-level interface.

**Usage**
set_interface_property <interface> <property> <value>

**Returns**
No return value.

**Arguments**

*interface*  The name of an exported top-level interface.

*property*  The name of the property. Refer to Interface Properties.

*value*  The property value.

**Example**
set_interface_property clk_out EXPORT_OF clk.clk_out

**Related Information**
- add_interface on page 528
- get_interface_properties on page 533
- get_interface_property on page 534
- Interface Properties on page 572
### 6.12.9. Validation

This section lists the commands that allow you to validate the components, instances, interfaces and connections in a Platform Designer system.

- `set_validation_property` on page 542
- `sync_sysinfo_parameters` on page 543
- `validate_component` on page 544
- `validate_component_interface` on page 545
- `validate_connection` on page 546
- `validate_instance` on page 547
- `validate_instance_interface` on page 548
- `validate_system` on page 549
- `validate_component_footprint` on page 550
- `reload_component_footprint` on page 511
6.12.9.1. set_validation_property

**Description**
Sets a property that affects how and when validation is run. To disable system validation after each scripting command, set AUTOMATIC_VALIDATION to False.

**Usage**
```plaintext
set_validation_property <property> <value>
```

**Returns**
No return value.

**Arguments**

*property*  The name of the property. Refer to Validation Properties.

*value*  The new property value.

**Example**
```plaintext
set_validation_property AUTOMATIC_VALIDATION false
```

**Related Information**
- validate_system on page 549
- Validation Properties on page 584
6.12.9.2. sync_sysinfo_parameters

**Description**
Updates the system info parameters of the specified generic component.

**Usage**
sync_sysinfo_parameters [{instance}]

**Returns**
String[]  A list of update messages.

**Arguments**

*instance* *(optional)*  Specifies the name of the instance to sync. If you do not specify this option, the command synchronizes all the generic components in the system.

**Example**
sync_sysinfo_parameters cpu_0

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.9.3. validate_component

**Description**
Validates the loaded component.

**Usage**
validate_component

**Returns**

`String[]`  A list of validation messages.

**Arguments**
No arguments

**Example**

```plaintext
validate_component
```

**Related Information**
- `validate_component_interface` on page 545
- `load_component` on page 510
6.12.9.4. validate_component_interface

Description
Validates an interface of the loaded component.

Usage
validate_component_interface <interface>

Returns
String[] List of validation messages

Arguments

instance Specifies the name of the instance for the loaded component.

Example

validate_instance_interface data_master

Related Information

• load_component on page 510
• validate_component on page 544
6.12.9.5. validate_connection

**Description**
Validates the specified connection and returns validation messages.

**Usage**
validate_connection `<connection>`

**Returns**
A list of validation messages.

**Arguments**

*connection* The connection name to validate.

**Example**

```
validate_connection cpu.data_master/sdram.s1
```

**Related Information**
- [validate_instance](#) on page 547
- [validate_instance_interface](#) on page 548
- [validate_system](#) on page 549
6.12.9.6. validate_instance

**Description**
Validates the specified child instance and returns validation messages.

**Usage**
validate_instance `<instance>`

**Returns**
A list of validation messages.

**Arguments**

`instance` The child instance name to validate.

**Example**

validate_instance cpu

**Related Information**
- *validate_connection* on page 546
- *validate_instance_interface* on page 548
- *validate_system* on page 549
6.12.9.7. validate_instance_interface

**Description**
Validates an interface of an instance and returns validation messages.

**Usage**
validate_instance_interface `<instance>` `<interface>`

**Returns**
A list of validation messages.

**Arguments**

`instance`  The child instance name.

`interface`  The interface to validate.

**Example**

validate_instance_interface cpu data_master

**Related Information**
- validate_connection on page 546
- validate_instance on page 547
- validate_system on page 549
6.12.9.8. validate_system

**Description**
Validates the system and returns validation messages.

**Usage**
validate_system

**Returns**
A list of validation messages.

**Arguments**
No arguments.

**Example**
validate_system

**Related Information**
- validate_connection on page 546
- validate_instance on page 547
- validate_instance_interface on page 548
### 6.12.9.9. validate_component_footprint

**Description**
Validates the footprint of the specified child instance.

**Usage**
validate_component_footprint <instance>

**Returns**
String[] List of validation messages.

**Arguments**

*instance (optional)* Specifies the child instance name. If you omit this option, the command validates all generic components in the system.

**Example**

validate_component_footprint cpu_0

**Related Information**
- load_instantiation on page 477
- save_instantiation on page 481
6.12.9.10. reload_component_footprint

Description
Validates the footprint of a specified child instance, and updates the footprint of the instance in case of issues.

Usage
reload_component_footprint [<instance>]

Returns
String[] A list of validation messages.

Arguments

instance (optional) Specifies the child instance name to validate. If you do not specify this option, the command validates all the generic components in the system.

Example
reload_component_footprint cpu_0

Related Information
• load_instantiation on page 477
• save_instantiation on page 481
• validate_component_footprint on page 550
6.12.10. Miscellaneous

This section lists the miscellaneous commands that you can use for your Platform Designer systems.

- auto_assign_base_addresses on page 553
- auto_assign_irqs on page 554
- auto_assign_system_base_addresses on page 555
- get_parameter_properties on page 556
- lock_avalon_base_address on page 557
- send_message on page 558
- set_use_testbench_naming_pattern on page 559
- unlock_avalon_base_address on page 560
- get_testbench_dutname on page 561
- get_use_testbench_naming_pattern on page 562
6.12.10.1. auto_assign_base_addresses

Description
Assigns base addresses to all memory-mapped interfaces of an instance in the system. Instance interfaces that are locked with lock_avalon_base_address keep their addresses during address auto-assignment.

Usage
auto_assign_base_addresses <instance>

Returns
No return value.

Arguments

instance The name of the instance with memory-mapped interfaces.

Example
auto_assign_base_addresses sdram

Related Information
- auto_assign_system_base_addresses on page 555
- lock_avalon_base_address on page 557
- unlock_avalon_base_address on page 560
### 6.12.10.2. auto_assign_irqs

**Description**
Assigns interrupt numbers to all connected interrupt senders of an instance in the system.

**Usage**
`auto_assign_irqs <instance>`

**Returns**
No return value.

**Arguments**

*instance*  The name of the instance with an interrupt sender.

**Example**

```
auto_assign_irqs uart_0
```
6.12.10.3. auto_assign_system_base_addresses

**Description**
Assigns legal base addresses to all memory-mapped interfaces of all instances in the system. Instance interfaces that are locked with `lock_avalon_base_address` keep their addresses during address auto-assignment.

**Usage**
amuto_assign_system_base_addresses

**Returns**
No return value.

**Arguments**
No arguments.

**Example**
amuto_assign_system_base_addresses

**Related Information**
- auto_assign_base_addresses on page 553
- lock_avalon_base_address on page 557
- unlock_avalon_base_address on page 560
6.12.10.4. get_parameter_properties

**Description**
Returns the list of properties that you can query for any parameters, for example parameters of instances, interfaces, instance interfaces, and connections.

**Usage**
get_parameter_properties

**Returns**

*String[]* The list of parameter properties.

**Arguments**
No arguments.

**Example**
```
get_parameter_properties
```

**Related Information**
- get_connection_parameter_property on page 518
- get_instance_interface_parameter_property on page 429
- get_instance_parameter_property on page 437
6.12.10.5. lock_avalon_base_address

Description
Prevents the memory-mapped base address from being changed for connections to
the specified interface of an instance when Platform Designer runs the
auto_assign_base_addresses or auto_assign_system_base_addresses
commands.

Usage
lock_avalon_base_address <instance.interface>

Returns
No return value.

Arguments

instance.interface   The qualified name of the interface of an instance, in
                  <instance>.<interface> format.

Example
lock_avalon_base_address sdram.s1

Related Information
• auto_assign_base_addresses on page 553
• auto_assign_system_base_addresses on page 555
• unlock_avalon_base_address on page 560
### 6.12.10.6. send_message

**Description**
Sends a message to the user of the component. The message text is normally HTML. You can use the `<b>` element to provide emphasis. If you do not want the message text to be HTML, then pass a list like `{ Info Text }` as the message level.

**Usage**

```
send_message <level> <message>
```

**Returns**
No return value.

**Arguments**

- **level** Intel Quartus Prime supports the following message levels:
  - `ERROR`—provides an error message.
  - `WARNING`—provides a warning message.
  - `INFO`—provides an informational message.
  - `PROGRESS`—provides a progress message.
  - `DEBUG`—provides a debug message when debug mode is enabled.

- **message** The text of the message.

**Example**

```
send_message ERROR "The system is down!"
send_message { Info Text } "The system is up!"
```
6.12.10.7. set_use_testbench_naming_pattern

**Description**
Use this command to create testbench systems so that the generated file names for the test system match the system’s original generated file names. Without setting this command, the generated file names for the test system receive the top-level testbench system name.

**Usage**
set_use_testbench_naming_pattern <value>

**Returns**
No return value.

**Arguments**
value  True or false.

**Example**
set_use_testbench_naming_pattern true

**Notes**
Use this command only to create testbench systems.
6.12.10.8. unlock_avalon_base_address

**Description**
Allows the memory-mapped base address to change for connections to the specified interface of an instance when Platform Designer runs the auto_assign_base_addresses or auto_assign_system_base_addresses commands.

**Usage**
unlock_avalon_base_address <instance.interface>

**Returns**
No return value.

**Arguments**

*instance.interface* The qualified name of the interface of an instance, in `<instance>.<interface>` format.

**Example**
unlock_avalon_base_address sdram.s1

**Related Information**
- auto_assign_base_addresses on page 553
- auto_assign_system_base_addresses on page 555
- lock_avalon_base_address on page 557
6.12.10.9. get_testbench_dutname

Description
Returns the currently set dutname for the test-bench systems. Use this command only when creating test-bench systems.

Usage
get_testbench_dutname

Returns

String The currently set dutname. Returns NULL if empty.

Arguments
No arguments.

Example
get_testbench_dutname

Related Information
- get_use_testbench_naming_pattern on page 562
- set_use_testbench_naming_pattern on page 559
6.12.10.10. get_use_testbench_naming_pattern

Description
Verifies if the test-bench naming pattern is set to be used. Use this command only when creating test-bench systems.

Usage
get_use_testbench_naming_pattern

Returns

boolean True, if the test-bench naming pattern is set to be used.

Arguments
No arguments.

Example
get_use_testbench_naming_pattern

Related Information
• get_testbench_dutname on page 561
• set_use_testbench_naming_pattern on page 559

6.12.11. Wire-Level Connection Commands

Wire-level commands accept optional input ports and wire-level expressions as arguments for the qsys-script utility and in _hw.tcl files.

You can use wire-level commands to:
• Apply a wire-level expression to a port with set_wirelevel_expression.
• Retrieve a list of expressions from a port, instance, or all expressions in the current level of system hierarchy with get_wirelevel_expression.
• Remove a list of expressions from a port, instance, or all expressions in the current level of system hierarchy with remove_wirelevel_expression.

Note: The following restrictions apply when using wire-level commands _hw.tcl files:
• Wire-level commands are only valid in a composition callback.
• Wire-level expressions can only be applied to instances created by add_instance.

Related Information
• Scripting Wire-Level Expressions on page 48
• Wire-Level Connectivity on page 43
• Create a Composed Component or Subsystem on page 135
6.12.11.1. set_wirelevel_expression

Description
Applies a wire-level expression to an optional input port or instance in the system.

Usage
set_wirelevel_expression <instance_or_port_bitselection> <expression>

Returns
No return value.

Arguments
instance_or_port_bitselection Specify the instance or port to which the wire-level expression using the <instance_name>.<port_name>[<bit_selection>] format. The bit selection can be a bit-select, for example [0], or a partial range defined in descending order, for example [7:0]. If no bit selection is specified, the full range of the port is selected.

expression The expression to be applied to an optional input port.

Examples
set_wirelevel_expression {module0.portA[7:0]} "8'b0"
set_wirelevel_expression module0.portA "8'b0"
set_wirelevel_expression {module0.portA[0]} "1'b0"

Related Information
• Scripting Wire-Level Expressions on page 48
• Wire-Level Connectivity on page 43

6.12.11.2. get_wirelevel_expressions

Description
Retrieve a list of wire-level expressions from an optional input port, instance, or all expressions in the current level of system hierarchy. If the port bit selection is specified as an argument, the range must be identical to what was used in the set_wirelevel_expression statement.

Usage
get_wirelevel_expressions <instance_or_port_bitselection>

Returns
String[] A flattened list of wire-level expressions. Every item in the list consists of right- and left-hand clauses of a wire-level expression. You can loop over the returned list using foreach{port expr} $return_list{}. 
Arguments

instance_or_port_bitselection Specifies which instance or port from which a list of wire-level expressions are retrieved using the <instance_name>.<port_name>[<bit_selection>] format.
  - If no <port_name>[<bit_selection>] is specified, the command causes the return of all expressions from the specified instance.
  - If no argument is present, the command causes the return of all expressions from the current level of system hierarchy.

The bit selection can be a bit-select, for example [0], or a partial range defined in descending order, for example [7:0]. If no bit selection is specified, the full range of the port is selected.

Example

get_wirelevel_expressions
get_wirelevel_expressions module0
get_wirelevel_expressions {module0.portA[7:0]}

Related Information
- Scripting Wire-Level Expressions on page 48
- Wire-Level Connectivity on page 43

6.12.11.3. remove_wirelevel_expressions

Description
Remove a list of wire-level expressions from an optional input port, instance, or all expressions in the current level of system hierarchy. If the port bit selection is specified as an argument, the range must be identical to what was used in the set_wirelevel_expressions statement.

Usage

remove_wirelevel_expressions <instance_or_port_bitselection>

Returns
No return value.

Arguments

instance_or_port_bitselection Specifies which instance or port from which a list of wire-level expressions are removed using the <instance_name>.<port_name>[<bit_selection>] format.
• If no `<port_name><bit_selection>` is specified, the command causes the removal of all expressions from the specified instance.

• If no argument is present, the command causes the return of all expressions from the current level of system hierarchy.

The *bit selection* can be a bit-select, for example `[0]`, or a partial range defined in descending order, for example `[7:0]`. If no *bit selection* is specified, the full range of the port is selected.

**Examples**

```
remove_wirelevel_expressions
remove_wirelevel_expressions module0
remove_wirelevel_expressions {module0.portA[7:0]}
```

**Related Information**

• [Scripting Wire-Level Expressions](#) on page 48

• [Wire-Level Connectivity](#) on page 43
6.13. Platform Designer Scripting Property Reference

Interface properties work differently for _hw.tcl scripting than with Platform Designer scripting. In _hw.tcl, interfaces do not distinguish between properties and parameters. In Platform Designer scripting, the properties and parameters are unique.

The following are the Platform Designer scripting properties:

- Connection Properties on page 567
- Design Environment Type Properties on page 568
- Direction Properties on page 569
- Element Properties on page 570
- Instance Properties on page 571
- Interface Properties on page 572
- Message Levels Properties on page 573
- Module Properties on page 574
- Parameter Properties on page 575
- Parameter Status Properties on page 577
- Parameter Type Properties on page 578
- Port Properties on page 579
- Project Properties on page 580
- System Info Type Properties on page 581
- Units Properties on page 583
- Validation Properties on page 584
- Interface Direction on page 585
- File Set Kind on page 586
- Access Type on page 587
- Instantiation HDL File Properties on page 588
- Instantiation Interface Duplicate Type on page 589
- Instantiation Interface Properties on page 590
- Instantiation Properties on page 591
- Port Properties on page 592
- VHDL Type on page 593
### 6.13.1. Connection Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>string</td>
<td>END</td>
<td>Indicates the end interface of the connection.</td>
</tr>
<tr>
<td>string</td>
<td>NAME</td>
<td>Indicates the name of the connection.</td>
</tr>
<tr>
<td>string</td>
<td>START</td>
<td>Indicates the start interface of the connection.</td>
</tr>
<tr>
<td>String</td>
<td>TYPE</td>
<td>The type of the connection.</td>
</tr>
</tbody>
</table>
6.13.2. Design Environment Type Properties

**Description**

IP cores use the design environment to identify the most appropriate interfaces to connect to the parent system.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NATIVE</td>
<td>Supports native IP interfaces.</td>
</tr>
<tr>
<td>QSYS</td>
<td>Supports standard Platform Designer interfaces.</td>
</tr>
</tbody>
</table>
## 6.13.3. Direction Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIDIR</td>
<td>Indicates the direction for a bidirectional signal.</td>
</tr>
<tr>
<td>INOUT</td>
<td>Indicates the direction for an input signal.</td>
</tr>
<tr>
<td>OUTPUT</td>
<td>Indicates the direction for an output signal.</td>
</tr>
</tbody>
</table>
6.13.4. Element Properties

Description
Element properties are, with the exception of ENABLED and NAME, read-only properties of the types of instances, interfaces, and connections. These read-only properties represent metadata that does not vary between copies of the same type. ENABLED and NAME properties are specific to particular instances, interfaces, or connections.

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>AUTHOR</td>
<td>The author of the component or interface.</td>
</tr>
<tr>
<td>Boolean</td>
<td>AUTO_EXPORT</td>
<td>Indicates whether unconnected interfaces on the instance are automatically exported.</td>
</tr>
<tr>
<td>String</td>
<td>CLASS_NAME</td>
<td>The type of the instance, interface or connection, for example, altera_nios2 or avalon_slave.</td>
</tr>
<tr>
<td>String</td>
<td>DESCRIPTION</td>
<td>The description of the instance, interface or connection type.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_NAME</td>
<td>The display name for referencing the type of instance, interface or connection.</td>
</tr>
<tr>
<td>Boolean</td>
<td>EDITABLE</td>
<td>Indicates whether you can edit the component in the Platform Designer Component Editor.</td>
</tr>
<tr>
<td>Boolean</td>
<td>ENABLED</td>
<td>Indicates whether the instance is enabled.</td>
</tr>
<tr>
<td>String</td>
<td>GROUP</td>
<td>The IP Catalog category.</td>
</tr>
<tr>
<td>Boolean</td>
<td>INTERNAL</td>
<td>Hides internal IP components or sub-components from the IP Catalog.</td>
</tr>
<tr>
<td>String</td>
<td>NAME</td>
<td>The name of the instance, interface or connection.</td>
</tr>
<tr>
<td>String</td>
<td>VERSION</td>
<td>The version number of the instance, interface or connection, for example, 16.1.</td>
</tr>
</tbody>
</table>
### 6.13.5. Instance Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>AUTO_EXPORT</td>
<td>Indicates whether Platform Designer automatically exports the unconnected interfaces on the instance.</td>
</tr>
<tr>
<td>Boolean</td>
<td>ENABLED</td>
<td>If true, Platform Designer includes this instance in the generated system.</td>
</tr>
<tr>
<td>String</td>
<td>NAME</td>
<td>The name of the system, which Platform Designer uses as the name of the top-level module in the generated HDL.</td>
</tr>
</tbody>
</table>
### 6.13.6. Interface Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>EXPORT_OF</td>
<td>Indicates which interface of a child instance to export through the top-level interface. Before using this command, you must create the top-level interface using the <code>add_interface</code> command. You must use the format: <code>&lt;instanceName.interfaceName&gt;</code>. For example: <code>set_interface_property CSC_input EXPORT_OF my_colorSpaceConverter.input_port</code></td>
</tr>
</tbody>
</table>
### 6.13.7. Message Levels Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMPONENT_INFO</td>
<td>Reports an informational message only during component editing.</td>
</tr>
<tr>
<td>DEBUG</td>
<td>Provides messages when debug mode is enabled.</td>
</tr>
<tr>
<td>ERROR</td>
<td>Provides an error message.</td>
</tr>
<tr>
<td>INFO</td>
<td>Provides an informational message.</td>
</tr>
<tr>
<td>PROGRESS</td>
<td>Reports progress during generation.</td>
</tr>
<tr>
<td>TODOERROR</td>
<td>Provides an error message that indicates the system is incomplete.</td>
</tr>
<tr>
<td>WARNING</td>
<td>Provides a warning message.</td>
</tr>
</tbody>
</table>
### 6.13.8. Module Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>GENERATION_ID</td>
<td>The generation ID for the system.</td>
</tr>
<tr>
<td>String</td>
<td>NAME</td>
<td>The name of the instance.</td>
</tr>
</tbody>
</table>
### 6.13.9. Parameter Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>AFFECTS_ELABORATION</td>
<td>Set AFFECTS_ELABORATION to false for parameters that do not affect the external interface of the module. An example of a parameter that does not affect the external interface is isNonVolatileStorage. An example of a parameter that does affect the external interface is width. When the value of a parameter changes and AFFECTS_ELABORATION is false, the elaboration phase does not repeat and improves performance. When AFFECTS_ELABORATION is set to true, the default value, Platform Designer reanalyzes the HDL file to determine the port widths and configuration each time a parameter changes.</td>
</tr>
<tr>
<td>Boolean</td>
<td>AFFECTS_GENERATION</td>
<td>The default value of AFFECTS_GENERATION is false if you provide a top-level HDL module. The default value is true if you provide a filesel callback. Set AFFECTS_GENERATION to false if the value of a parameter does not change the results of filesel generation.</td>
</tr>
<tr>
<td>Boolean</td>
<td>AFFECTS_VALIDATION</td>
<td>The AFFECTS_VALIDATION property determines whether a parameter's value sets derived parameters, and whether the value affects validation messages. Setting this property to false may improve response time in the parameter editor when the value changes.</td>
</tr>
<tr>
<td>String[]</td>
<td>ALLOWED_RANGES</td>
<td>Indicates the range or ranges of the parameter. For integers, each range is a single value, or a range of values defined by a start and end value, and delimited by a colon, for example, 11:15. This property also specifies the legal values and description strings for integers, for example, {0:None 1:Monophonic 2:Stereo 4:Quadrophonic}, where 0, 1, 2, and 4 are the legal values. You can assign description strings in the parameter editor for string variables. For example, ALLOWED_RANGES = {&quot;dev1:Cyclone IV GX&quot;**dev2:Stratix V GT&quot;}</td>
</tr>
<tr>
<td>String</td>
<td>DEFAULT_VALUE</td>
<td>The default value.</td>
</tr>
<tr>
<td>Boolean</td>
<td>DERIVED</td>
<td>When True, indicates that the parameter value is set by the component and cannot be set by the user. Derived parameters are not saved as part of an instance's parameter values. The default value is False.</td>
</tr>
<tr>
<td>String</td>
<td>DESCRIPTION</td>
<td>A short user-visible description of the parameter, suitable for a tooltip description in the parameter editor.</td>
</tr>
<tr>
<td>String[]</td>
<td>DISPLAY_HINT</td>
<td>Provides a hint about how to display a property.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• boolean—for integer parameters whose value are 0 or 1. The parameter displays as an option that you can turn on or off.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• radio—displays a parameter with a list of values as radio buttons.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• hexadecimal—for integer parameters, displays and interprets the value as a hexadecimal number, for example: 0x00000010 instead of 16.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• fixed_size—for string_list and integer_list parameters, the fixed_size DISPLAY_HINT eliminates the Add and Remove buttons from tables.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_NAME</td>
<td>The GUI label that appears to the left of this parameter.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_UNITS</td>
<td>The GUI label that appears to the right of the parameter.</td>
</tr>
<tr>
<td>Boolean</td>
<td>ENABLED</td>
<td>When False, the parameter is disabled. The parameter displays in the parameter editor but is grayed out, indicating that you cannot edit this parameter.</td>
</tr>
<tr>
<td>String</td>
<td>GROUP</td>
<td>Controls the layout of parameters in the GUI.</td>
</tr>
<tr>
<td>Type</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>--------------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Boolean</td>
<td>HDL_PARAMETER</td>
<td>When True, Platform Designer passes the parameter to the HDL component description. The default value is False.</td>
</tr>
<tr>
<td>String</td>
<td>LONG_DESCRIPTION</td>
<td>A user-visible description of the parameter. Similar to DESCRIPTION, but allows a more detailed explanation.</td>
</tr>
<tr>
<td>String</td>
<td>NEW_INSTANCE_VALUE</td>
<td>Changes the default value of a parameter without affecting older components that do not explicitly set a parameter value, and use the DEFAULT_VALUE property. Oder instances continue to use DEFAULT_VALUE for the parameter and new instances use the value assigned by NEW_INSTANCE_VALUE.</td>
</tr>
<tr>
<td>String[]</td>
<td>SYSTEM_INFO</td>
<td>Allows you to assign information about the instantiating system to a parameter that you define. SYSTEM_INFO requires an argument specifying the type of information. For example: <code>SYSTEM_INFO &lt;info-type&gt;</code></td>
</tr>
<tr>
<td>String</td>
<td>SYSTEM_INFO_ARG</td>
<td>Defines an argument to pass to SYSTEM_INFO. For example, the name of a reset interface.</td>
</tr>
<tr>
<td>(various)</td>
<td>SYSTEM_INFO_TYPE</td>
<td>Specifies the types of system information that you can query. Refer to System Info Type Properties.</td>
</tr>
<tr>
<td>(various)</td>
<td>TYPE</td>
<td>Specifies the type of the parameter. Refer to Parameter Type Properties.</td>
</tr>
<tr>
<td>(various)</td>
<td>UNITS</td>
<td>Sets the units of the parameter. Refer to Units Properties.</td>
</tr>
<tr>
<td>Boolean</td>
<td>VISIBLE</td>
<td>Indicates whether or not to display the parameter in the parameter editor.</td>
</tr>
<tr>
<td>String</td>
<td>WIDTH</td>
<td>Indicates the width of the logic vector for the STD_LOGIC_VECTOR parameter.</td>
</tr>
</tbody>
</table>

**Related Information**

- System Info Type Properties on page 581
- Parameter Type Properties on page 578
- Units Properties on page 583
### 6.13.10. Parameter Status Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>ACTIVE</td>
<td>Indicates that this parameter is an active parameter.</td>
</tr>
<tr>
<td>Boolean</td>
<td>DEPRECATED</td>
<td>Indicates that this parameter exists only for backwards compatibility, and may not have any effect.</td>
</tr>
<tr>
<td>Boolean</td>
<td>EXPERIMENTAL</td>
<td>Indicates that this parameter is experimental and not exposed in the design flow.</td>
</tr>
</tbody>
</table>
### 6.13.11. Parameter Type Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOLEAN</td>
<td>A boolean parameter set to true or false.</td>
</tr>
<tr>
<td>FLOAT</td>
<td>A signed 32-bit floating point parameter. (Not supported for HDL parameters.)</td>
</tr>
<tr>
<td>INTEGER</td>
<td>A signed 32-bit integer parameter.</td>
</tr>
<tr>
<td>INTEGER_LIST</td>
<td>A parameter that contains a list of 32-bit integers. (Not supported for HDL parameters.)</td>
</tr>
<tr>
<td>LONG</td>
<td>A signed 64-bit integer parameter. (Not supported for HDL parameters.)</td>
</tr>
<tr>
<td>NATURAL</td>
<td>A 32-bit number that contains values 0 to 2147483647 (0x7fffffff).</td>
</tr>
<tr>
<td>POSITIVE</td>
<td>A 32-bit number that contains values 1 to 2147483647 (0x7fffffff).</td>
</tr>
<tr>
<td>STD_LOGIC</td>
<td>A single bit parameter set to 0 or 1.</td>
</tr>
<tr>
<td>STD_LOGIC_VECTOR</td>
<td>An arbitrary-width number. The parameter property WIDTH determines the size of the logic vector.</td>
</tr>
<tr>
<td>STRING</td>
<td>A string parameter.</td>
</tr>
<tr>
<td>STRING_LIST</td>
<td>A parameter that contains a list of strings. (Not supported for HDL parameters.)</td>
</tr>
</tbody>
</table>
### 6.13.12. Port Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(various)</td>
<td>DIRECTION</td>
<td>The direction of the signal. Refer to Direction Properties.</td>
</tr>
<tr>
<td>String</td>
<td>ROLE</td>
<td>The type of the signal. Each interface type defines a set of interface types for its ports.</td>
</tr>
<tr>
<td>Integer</td>
<td>WIDTH</td>
<td>The width of the signal in bits.</td>
</tr>
</tbody>
</table>

**Related Information**

Direction Properties on page 569
### 6.13.13. Project Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>DEVICE</td>
<td>The device part number in the Intel Quartus Prime project that contains the Platform Designer system.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_FAMILY</td>
<td>The device family name in the Intel Quartus Prime project that contains the Platform Designer system.</td>
</tr>
</tbody>
</table>
### 6.13.14. System Info Type Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>ADDRESS_MAP</td>
<td>An XML-formatted string that describes the address map for the interface specified in the SYSTEM_INFO parameter property.</td>
</tr>
<tr>
<td>Integer</td>
<td>ADDRESS_WIDTH</td>
<td>The number of address bits that Platform Designer requires to address memory-mapped slaves connected to the specified memory-mapped master in this instance.</td>
</tr>
<tr>
<td>String</td>
<td>AVALON_SPEC</td>
<td>The version of the Platform Designer interconnect. Refer to Avalon Interface Specifications.</td>
</tr>
<tr>
<td>Integer</td>
<td>CLOCK_DOMAIN</td>
<td>An integer that represents the clock domain for the interface specified in the SYSTEM_INFO parameter property. If this instance has interfaces on multiple clock domains, you can use this property to determine which interfaces are on each clock domain. The absolute value of the integer is arbitrary.</td>
</tr>
<tr>
<td>Long, Integer</td>
<td>CLOCK_RATE</td>
<td>The rate of the clock connected to the clock input specified in the SYSTEM_INFO parameter property. If zero, the clock rate is currently unknown.</td>
</tr>
<tr>
<td>String</td>
<td>CLOCK_RESET_INFO</td>
<td>The name of this instance’s primary clock or reset sink interface. You use this property to determine the reset sink for global reset when you use Platform Designer interconnect that conforms to Avalon Interface Specifications.</td>
</tr>
<tr>
<td>String</td>
<td>CUSTOM_INSTRUCTION_SLAVES</td>
<td>Provides slave information, including the name, base address, address span, and clock cycle type.</td>
</tr>
<tr>
<td>String</td>
<td>DESIGN_ENVIRONMENT</td>
<td>A string that identifies the current design environment. Refer to Design Environment Type Properties.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE</td>
<td>The device part number of the selected device.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_FAMILY</td>
<td>The family name of the selected device.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_FEATURES</td>
<td>A list of key/value pairs delimited by spaces that indicate whether a device feature is available in the selected device family. The format of the list is suitable for passing to the array command. The keys are device features. The values are 1 if the feature is present, and 0 if the feature is absent.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_SPEEDGRADE</td>
<td>The speed grade of the selected device.</td>
</tr>
<tr>
<td>Integer</td>
<td>GENERATION_ID</td>
<td>An integer that stores a hash of the generation time that Platform Designer uses as a unique ID for a generation run.</td>
</tr>
<tr>
<td>BigInteger, Long</td>
<td>INTERRUPTS_USED</td>
<td>A mask indicating which bits of an interrupt receiver are connected to interrupt senders. The interrupt receiver is specified in the system info argument.</td>
</tr>
<tr>
<td>Integer</td>
<td>MAX_SLAVE_DATA_WIDTH</td>
<td>The data width of the widest slave connected to the specified memory-mapped master.</td>
</tr>
<tr>
<td>String, Boolean, Integer</td>
<td>QUARTUS_INI</td>
<td>The value of the quartus.ini setting specified in the system info argument.</td>
</tr>
<tr>
<td>Integer</td>
<td>RESET_DOMAIN</td>
<td>An integer representing the reset domain for the interface specified in the SYSTEM_INFO parameter property. If this instance has interfaces on multiple reset domains.</td>
</tr>
<tr>
<td>Type</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>domains, you can use this property to determine which interfaces are on each reset domain. The absolute value of the integer is arbitrary.</td>
</tr>
<tr>
<td>String</td>
<td>TRISTATECONDUIT_INFO</td>
<td>An XML description of the tri-state conduit masters connected to a tri-state conduit slave. The slave is specified as the SYSTEM_INFO parameter property. The value contains information about the slave, connected master instance and interface names, and signal names, directions, and widths.</td>
</tr>
<tr>
<td>String</td>
<td>TRISTATECONDUIT_MASTERS</td>
<td>The names of the instance's interfaces that are tri-state conduit slaves.</td>
</tr>
<tr>
<td>String</td>
<td>UNIQUE_ID</td>
<td>A string guaranteed to be unique to this instance.</td>
</tr>
</tbody>
</table>

**Related Information**

- [Design Environment Type Properties](#) on page 568
- [Avalon Interface Specifications](#)
- [Platform Designer Interconnect](#) on page 143
### 6.13.15. Units Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS</td>
<td>A memory-mapped address.</td>
</tr>
<tr>
<td>BITS</td>
<td>Memory size in bits.</td>
</tr>
<tr>
<td>BITSPERSECOND</td>
<td>Rate in bits per second.</td>
</tr>
<tr>
<td>BYTES</td>
<td>Memory size in bytes.</td>
</tr>
<tr>
<td>CYCLES</td>
<td>A latency or count in clock cycles.</td>
</tr>
<tr>
<td>GIGABITSPERSECOND</td>
<td>Rate in gigabits per second.</td>
</tr>
<tr>
<td>GIGABYTES</td>
<td>Memory size in gigabytes.</td>
</tr>
<tr>
<td>GIGAHertz</td>
<td>Frequency in GHz.</td>
</tr>
<tr>
<td>Hertz</td>
<td>Frequency in Hz.</td>
</tr>
<tr>
<td>KILOBITSPERSECOND</td>
<td>Rate in kilobits per second.</td>
</tr>
<tr>
<td>KILOBYTES</td>
<td>Memory size in kilobytes.</td>
</tr>
<tr>
<td>KILOHERTZ</td>
<td>Frequency in kHz.</td>
</tr>
<tr>
<td>MEGABITSPERSECOND</td>
<td>Rate, in megabits per second.</td>
</tr>
<tr>
<td>MEGABYTES</td>
<td>Memory size in megabytes.</td>
</tr>
<tr>
<td>MEGAHERTZ</td>
<td>Frequency in MHz.</td>
</tr>
<tr>
<td>MICROSECONDS</td>
<td>Time in microseconds.</td>
</tr>
<tr>
<td>MILLISECONDS</td>
<td>Time in milliseconds.</td>
</tr>
<tr>
<td>NANOSECONDS</td>
<td>Time in nanoseconds.</td>
</tr>
<tr>
<td>NONE</td>
<td>Unspecified units.</td>
</tr>
<tr>
<td>PERCENT</td>
<td>A percentage.</td>
</tr>
<tr>
<td>PICOSECONDS</td>
<td>Time in picoseconds.</td>
</tr>
<tr>
<td>SECONDS</td>
<td>Time in seconds.</td>
</tr>
</tbody>
</table>
6.13.16. Validation Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>AUTOMATIC_VALIDATION</td>
<td>When true, Platform Designer runs system validation and elaboration after each scripting command. When false, Platform Designer runs system validation with validation scripting commands. Some queries affected by system elaboration may be incorrect if automatic validation is disabled. You can disable validation to make a system script run faster.</td>
</tr>
</tbody>
</table>
6.13.17. Interface Direction

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>INPUT</td>
<td>Indicates that the interface is a slave (input, transmitter, sink, or end).</td>
</tr>
<tr>
<td>String</td>
<td>OUTPUT</td>
<td>Indicates that the interface is a master (output, receiver, source, or start).</td>
</tr>
</tbody>
</table>
### 6.13.18. File Set Kind

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXAMPLE_DESIGN</td>
<td>This file-set contains example design files.</td>
</tr>
<tr>
<td>QUARTUS_SYNTH</td>
<td>This file-set contains files that Platform Designer uses for Intel Quartus Prime Synthesis</td>
</tr>
<tr>
<td>SIM_VERILOG</td>
<td>This file-set contains files that Platform Designer uses for Verilog HDL Simulation.</td>
</tr>
<tr>
<td>SIM_VHDL</td>
<td>This file-set contains files that Platform Designer uses for VHDL Simulation.</td>
</tr>
</tbody>
</table>
### 6.13.19. Access Type

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>READ_ONLY</td>
<td>Indicates that the parameter can be only read-only.</td>
</tr>
<tr>
<td>String</td>
<td>WRITABLE</td>
<td>Indicates that the parameter has read/write properties.</td>
</tr>
</tbody>
</table>
### 6.13.20. Instantiation HDL File Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean CONTAINS_INLINE_CONFIG</td>
<td>Returns True if the HDL file contains inline configuration.</td>
<td></td>
</tr>
<tr>
<td>Boolean IS_CONFIGURATION_PACKAGE</td>
<td>Returns True if the HDL file is a configuration package.</td>
<td></td>
</tr>
<tr>
<td>Boolean IS_TOP_LEVEL</td>
<td>Returns True if the HDL file is the top-level HDL file.</td>
<td></td>
</tr>
<tr>
<td>String OUTPUT_PATH</td>
<td>Specifies the output path of the HDL file.</td>
<td></td>
</tr>
<tr>
<td>String TYPE</td>
<td>Specifies the HDL file type of the HDL file.</td>
<td></td>
</tr>
</tbody>
</table>
6.13.21. Instantiation Interface Duplicate Type

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>CLONE</td>
<td>Creates a copy of an interface and all the interface ports.</td>
</tr>
<tr>
<td>String</td>
<td>MIRROR</td>
<td>Creates a copy of an interface with all the port roles and directions reversed.</td>
</tr>
</tbody>
</table>
### 6.13.22. Instantiation Interface Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>DIRECTION</td>
<td>The direction of the interface.</td>
</tr>
<tr>
<td>String</td>
<td>TYPE</td>
<td>The type of the interface.</td>
</tr>
</tbody>
</table>
### 6.13.23. Instantiation Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>HDL_COMPILATION_LIBRARY</td>
<td>Indicates the HDL compilation library name of the generic component.</td>
</tr>
<tr>
<td>String</td>
<td>HDL_ENTITY_NAME</td>
<td>Indicates the HDL entity name of the Generic Component.</td>
</tr>
<tr>
<td>String</td>
<td>IP_FILE</td>
<td>Indicates the .ip file path that implements the generic component.</td>
</tr>
</tbody>
</table>
### 6.13.24. Port Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>DIRECTION</td>
<td>Specifies the direction of the signal</td>
</tr>
<tr>
<td>String</td>
<td>NAME</td>
<td>Renames a top-level port. Only use with <code>set_interface_port_property</code></td>
</tr>
<tr>
<td>String</td>
<td>ROLE</td>
<td>Specifies the type of the signal. Each interface type defines a set of interface types for its ports.</td>
</tr>
<tr>
<td>String</td>
<td>VHDL_TYPE</td>
<td>Specifies the VHDL type of the signal. Can be either <code>STANDARD_LOGIC</code>, or <code>STANDARD_LOGIC_VECTOR</code>.</td>
</tr>
<tr>
<td>Integer</td>
<td>WIDTH</td>
<td>Specifies the width of the signal in bits.</td>
</tr>
</tbody>
</table>

**Related Information**

- Direction Properties on page 569
6.13.25. VHDL Type

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>STD_LOGIC</td>
<td>Represents the value of a digital signal in a wire.</td>
</tr>
<tr>
<td>STD_LOGIC_VECTOR</td>
<td>Represents an array of digital signals and variables.</td>
</tr>
</tbody>
</table>


The following revision history applies to this chapter:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020.06.22</td>
<td>20.2.0</td>
<td>• Added set_design_id command.</td>
</tr>
<tr>
<td>2019.11.11</td>
<td>19.1.0</td>
<td>• Added statement to <code>qsys-generate</code> topic indicating that <code>graybox</code> option is only for individual Intel FPGA IP cores, and not for complete Platform Designer systems.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added statement to <code>qsys-generate</code> topic indicating that <code>upgrade-ip-cores</code> has no impact on subsystems.</td>
</tr>
<tr>
<td>2019.04.01</td>
<td>19.1.0</td>
<td>• Added new Domains command-line reference and deprecated <code>get_interconnect_requirement</code>, <code>get_interconnect_requirements</code>, and <code>set_interconnect_requirement</code> assignments.</td>
</tr>
<tr>
<td>2018.12.15</td>
<td>18.1.0</td>
<td>First release as separate chapter.</td>
</tr>
<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Added command-line options for <code>qsys-archive</code>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added command-line options for <code>quartus_ipgenerate</code>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated the Qsys Pro scripting commands.</td>
</tr>
<tr>
<td>2016.05.03</td>
<td>16.0.0</td>
<td>• Qsys Command-Line Utilities updated with latest supported command-line options.</td>
</tr>
<tr>
<td>June 2012</td>
<td>12.0.0</td>
<td>• Added command-line utilities, and scripts.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.1.0</td>
<td>Initial release of content.</td>
</tr>
</tbody>
</table>
7. Component Interface Tcl Reference

Tcl commands allow you to perform a wide range of functions in Platform Designer. Command descriptions contain the Platform Designer phases where you can use the command, for example, main program, elaboration, composition, or fileset callback. This reference denotes optional command arguments in brackets [ ].

Note: Intel now refers to Qsys Pro as Platform Designer.

Platform Designer supports Avalon, AMBA 3 AXI (version 1.0), AMBA 4 AXI (version 2.0), AMBA 4 AXI-Lite (version 2.0), AMBA 4 AXI-Stream (version 1.0), and AMBA 3 APB (version 1.0) interface specifications.

For more information about procedures for creating IP component _hw.tcl files in the Platform Designer Component Editor, and supported interface standards, refer to Creating Platform Designer Components and Platform Designer Interconnect.

If you are developing an IP component to work with the Nios II processor, refer to Publishing Component Information to Embedded Software in section 3 of the Nios II Software Developer's Handbook, which describes how to publish hardware IP component information for embedded software tools, such as a C compiler and a Board Support Package (BSP) generator.

Related Information
- Avalon Interface Specifications
- AMBA Protocol Specifications
- Creating Platform Designer Components on page 90
- Platform Designer Interconnect on page 143
- Publishing Component Information to Embedded Software in Nios II Gen2 Software Developer's Handbook

7.1. Platform Designer _hw.tcl Command Reference
7. Component Interface Tcl Reference

7.1.1. Interfaces and Ports

add_interface on page 596
add_interface_port on page 598
get_interfaces on page 600
get_interface_assignment on page 601
get_interface_assignments on page 602
get_interface_ports on page 603
get_interface_properties on page 604
get_interface_property on page 605
get_port_properties on page 606
get_port_property on page 607
set_interface_assignment on page 608
set_interface_property on page 610
set_port_property on page 611
set_interface_upgrade_map on page 612

Related Information
Interface Properties on page 693
7.1.1.1. add_interface

Description
Adds an interface to your module. An interface represents a collection of related signals that are managed together in the parent system. These signals are implemented in the IP component's HDL, or exported from an interface from a child instance. As the IP component author, you choose the name of the interface.

Availability
Discovery, Main Program, Elaboration, Composition

Usage
add_interface <name> <type> <direction> [<associated_clock>]

Returns
No returns value.

Arguments

name  A name you choose to identify an interface.

type  The type of interface.

direction  The interface direction.

associated_clock (optional)  (deprecated) For interfaces requiring associated clocks, use:
set_interface_property <interface> associatedClock <clockInterface> For interfaces requiring associated resets, use: set_interface_property <interface> associatedReset <resetInterface>

Example
add_interface mm_slave avalon slave
add_interface my_export conduit end
set_interface_property my_export EXPORT_OF uart_0.external_connection

Notes
By default, interfaces are enabled. You can set the interface property ENABLED to false to disable an interface. If an interface is disabled, it is hidden and its ports are automatically terminated to their default values. Active high signals are terminated to 0. Active low signals are terminated to 1.

If the IP component is composed of child instances, the top-level interface is associated with a child instance's interface with set_interface_property interface EXPORT_OF child_instance.interface.

The following direction rules apply to Platform Designer-supported interfaces.
### Related Information

- [add_interface_port](#) on page 598
- [get_interface_assignments](#) on page 602
- [get_interface_properties](#) on page 604
- [get_interfaces](#) on page 600
7.1.1.2. add_interface_port

**Description**
Adds a port to an interface on your module. The name must match the name of a signal on the top-level module in the HDL of your IP component. The port width and direction must be set before the end of the elaboration phase. You can set the port width as follows:

- In the Main program, you can set the port width to a fixed value or a width expression.
- If the port width is set to a fixed value in the Main program, you can update the width in the elaboration callback.

**Availability**
Main Program, Elaboration

**Usage**

```
add_interface_port <interface> <port> [signal_type] <direction> [width_expression]
```

**Returns**

**Arguments**

- `interface`  The name of the interface to which this port belongs.
- `port`  The name of the port. This name must match a signal in your top-level HDL for this IP component.
- `signal_type`  The type of signal for this port, which must be unique. Refer to the Avalon Interface Specifications for the signal types available for each interface type.
- `direction`  The direction of the signal. Refer to Direction Properties.
- `width_expression`  The width of the port, in bits. The width may be a fixed value, or a simple arithmetic expression of parameter values.

**Example**

**fixed width:**
```
add_interface_port mm_slave s0_rdata readdata output 32
```

**width expression:**
```
add_parameter DATA_WIDTH INTEGER 32
add_interface_port s0 rdata readdata output "DATA_WIDTH/2"
```

**Related Information**
- `add_interface` on page 596
- `get_port_properties` on page 606
7. Component Interface Tcl Reference

- `get_port_property` on page 607
- `get_port_property` on page 607
- `Direction Properties` on page 702
- `Avalon Interface Specifications`
7.1.1.3. get_interfaces

**Description**
Returns a list of top-level interfaces.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_interfaces

**Returns**
A list of the top-level interfaces exported from the system.

**Arguments**
No arguments.

**Example**

```
get_interfaces
```

**Related Information**
add_interface on page 596
### 7.1.1.4. `get_interface_assignment`

**Description**
Returns the value of the specified assignment for the specified interface

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**

```
get_interface_assignment <interface> <assignment>
```

**Returns**
The value of the assignment.

**Arguments**

- `interface`  The name of a top-level interface.
- `assignment`  The name of an assignment.

**Example**

```
get_interface_assignment s1 embeddedsw.configuration.isFlash
```

**Related Information**
- `add_interface` on page 596
- `get_interface_assignments` on page 602
- `get_interfaces` on page 600
7.1.1.5. get_interface_assignments

Description
Returns the value of all interface assignments for the specified interface.

Availability
Main Program, Elaboration, Validation, Composition

Usage
get_interface_assignments <interface>

Returns
A list of assignment keys.

Arguments

interface The name of the top-level interface whose assignment is being retrieved.

Example
get_interface_assignments s1

Related Information
- add_interface on page 596
- get_interface_assignment on page 601
- get_interfaces on page 600
7.1.1.6. get_interface_ports

Description
Returns the names of all of the ports that have been added to a given interface. If the interface name is omitted, all ports for all interfaces are returned.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

Usage
get_interface_ports [<interface>]

Returns
A list of port names.

Arguments

interface (optional) The name of a top-level interface.

Example
get_interface_ports mm_slave

Related Information
- add_interface_port on page 598
- get_port_property on page 607
- set_port_property on page 611
7.1.1.7. get_interface_properties

**Description**
Returns the names of all the interface properties for the specified interface as a space separated list.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_interface_properties <interface>

**Returns**
A list of properties for the interface.

**Arguments**

*interface*  The name of an interface.

**Example**

get_interface_properties interface

**Notes**
The properties for each interface type are different. Refer to the *Avalon Interface Specifications* for more information about interface properties.

**Related Information**
- get_interface_property on page 605
- set_interface_property on page 610
- Avalon Interface Specifications
7.1.1.8. get_interface_property

**Description**
Returns the value of a single interface property from the specified interface.

**Availability**
Discovery, Main Program, Elaboration, Composition, Fileset Generation

**Usage**
get_interface_property <interface> <property>

**Returns**

**Arguments**

*interface*  The name of an interface.

*property*  The name of the property whose value you want to retrieve. Refer to Interface Properties.

**Example**

get_interface_property mm_slave linewrapBursts

**Notes**
The properties for each interface type are different. Refer to the *Avalon Interface Specifications* for more information about interface properties.

**Related Information**
- get_interface_properties on page 604
- set_interface_property on page 610
- *Avalon Interface Specifications*
7.1.1.9. get_port_properties

Description
Returns a list of port properties.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

Usage
get_port_properties

Returns
A list of port properties. Refer to Port Properties.

Arguments
No arguments.

Example
get_port_properties

Related Information
• add_interface_port on page 598
• get_port_property on page 607
• set_port_property on page 611
• Port Properties on page 700
7.1.1.10. get_port_property

**Description**
Returns the value of a property for the specified port.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_port_property <port> <property>

**Returns**
The value of the property.

**Arguments**

port The name of the port.

property The name of a port property. Refer to Port Properties.

**Example**
get_port_property rdata WIDTH_VALUE

**Related Information**
- add_interface_port on page 598
- get_port_properties on page 606
- set_port_property on page 611
- Port Properties on page 700
### 7.1.1.11. set_interface_assignment

**Description**
Sets the value of the specified assignment for the specified interface.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
```
set_interface_assignment <interface> <assignment> [::<value>]
```

**Returns**
No return value.

**Arguments**

*interface*  The name of the top-level interface whose assignment is being set.

*assignment*  The assignment whose value is being set.

*value (optional)*  The new assignment value.

**Example**
```
set_interface_assignment s1 embeddedsw.configuration.isFlash 1
```

**Notes**

**Assignments for Nios II Software Build Tools**

Interface assignments provide extra data for the Nios II Software Build Tools working with the generated system.

**Assignments for Platform Designer Tools**

There are several assignments that guide behavior in the Platform Designer tools.

*qsx.ui.export_name:*  If present, this interface should always be exported when an instance is added to a Platform Designer system. The value is the requested name of the exported interface in the parent system.

*qsx.ui.connect:*  If present, this interface should be auto-connected when an instance is added to a Platform Designer system. The value is a comma-separated list of other interfaces on the same instance that should be connected with this interface.
ui.blockdiagram.direction: If present, the direction of this interface in the block diagram is set by the user. The value is either "output" or "input".

Related Information
- add_interface on page 596
- get_interface_assignment on page 601
- get_interface_assignments on page 602
7.1.1.12. set_interface_property

**Description**
Sets the value of a property on an exported top-level interface. You can use this command to set the `EXPORT_OF` property to specify which interface of a child instance is exported via this top-level interface.

**Availability**
Main Program, Elaboration, Composition

**Usage**
```
set_interface_property <interface> <property> <value>
```

**Returns**
No return value.

**Arguments**
- `interface`  The name of an exported top-level interface.
- `property`   The name of the property Refer to [Interface Properties](#).
- `value`      The new property value.

**Example**
```
set_interface_property clk_out EXPORT_OF clk.clk_out
set_interface_property mm_slave linewrapBursts false
```

**Notes**
The properties for each interface type are different. Refer to the Avalon Interface Specifications for more information about interface properties.

**Related Information**
- [get_interface_properties](#) on page 604
- [get_interface_property](#) on page 605
- Avalon Interface Specifications
7.1.1.13. set_port_property

Description
Sets a port property.

Availability
Elaboration

Usage
set_port_property <port> <property> [<value>]

Returns
The new value.

Arguments

port  The name of the port.

property  One of the supported properties. Refer to Port Properties.

value (optional)  The value to set.

Example

set_port_property rdata WIDTH 32

Related Information

• add_interface_port on page 598
• get_port_properties on page 606
• set_port_property on page 611
7.1.1.14. set_interface_upgrade_map

Description
Maps the interface name of an older version of an IP core to the interface name of the current IP core. The interface type must be the same between the older and newer versions of the IP cores. This allows system connections and properties to maintain proper functionality. By default, if the older and newer versions of IP core have the same name and type, then Platform Designer maintains all properties and connections automatically.

Availability
Parameter Upgrade

Usage
set_interface_upgrade_map { <old_interface_name> <new_interface_name> <old_interface_name_2> <new_interface_name_2> ... }

Returns
No return value.

Arguments
{ <old_interface_name> <new_interface_name> } List of mappings between names of older and newer interfaces.

Example
set_interface_upgrade_map { avalon_master_interface new_avalon_master_interface }
7.1.2. Parameters

- add_parameter on page 614
- get_parameters on page 615
- get_parameter_properties on page 616
- get_parameter_property on page 617
- get_parameter_value on page 618
- get_string on page 619
- load_strings on page 620
- set_parameter_property on page 621
- set_parameter_value on page 622
7.1.2.1. add_parameter

Description
Adds a parameter to your IP component.

Availability
Main Program

Usage
add_parameter <name> <type> [<default_value> <description>]

Returns

Arguments

name  The name of the parameter.

type  The data type of the parameter Refer to Parameter Type Properties.

default_value (optional)  The initial value of the parameter in a new instance of the IP component.

description (optional)  Explains the use of the parameter.

Example

add_parameter seed INTEGER 17 "The seed to use for data generation."

Notes
Most parameter types have a single GUI element for editing the parameter value. string_list and integer_list parameters are different, because they are edited as tables. A multi-column table can be created by grouping multiple into a single table. To edit multiple list parameters in a single table, the display items for the parameters must be added to a group with a TABLE hint:

add_parameter coefficients INTEGER_LIST add_parameter positions INTEGER_LIST add_display_item "" "Table Group" GROUP TABLE
add_display_item "Table Group" coefficients PARAMETER
add_display_item "Table Group" positions PARAMETER

Related Information

• get_parameter_properties on page 616
• get_parameter_property on page 617
• get_parameter_value on page 618
• set_parameter_property on page 621
• set_parameter_value on page 622
• Parameter Type Properties on page 698
7.1.2.2. get_parameters

**Description**
Returns the names of all the parameters in the IP component.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_parameters

**Returns**
A list of parameter names

**Arguments**
No arguments.

**Example**
get_parameters

**Related Information**
- add_parameter on page 614
- get_parameter_property on page 617
- get_parameter_value on page 618
- get_parameters on page 615
- set_parameter_property on page 621
7.1.2.3. get_parameter_properties

**Description**
Returns a list of all the parameter properties as a list of strings. The `get_parameter_property` and `set_parameter_property` commands are used to get and set the values of these properties, respectively.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_parameter_properties

**Returns**
A list of parameter property names. Refer to *Parameter Properties*.

**Arguments**
No arguments.

**Example**
```
set property_summary [ get_parameter_properties ]
```

**Related Information**
- `add_parameter` on page 614
- `get_parameter_property` on page 617
- `get_parameter_value` on page 618
- `get_parameters` on page 615
- `set_parameter_property` on page 621
- *Parameter Properties* on page 696
### 7.1.2.4. `get_parameter_property`

**Description**
Returns the value of a property of a parameter.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
```tcl
get_parameter_property <parameter> <property>
```

**Returns**
The value of the property.

**Arguments**

- `parameter`  The name of the parameter whose property value is being retrieved.
- `property`  The name of the property. Refer to [Parameter Properties](#).

**Example**
```tcl
set enabled [ get_parameter_property parameter1 ENABLED ]
```

**Related Information**
- `add_parameter` on page 614
- `get_parameter_properties` on page 616
- `get_parameter_value` on page 618
- `get_parameters` on page 615
- `set_parameter_property` on page 621
- `set_parameter_value` on page 622
- Parameter Properties on page 696
7.1.2.5. get_parameter_value

**Description**
Returns the current value of a parameter defined previously with the `add_parameter` command.

**Availability**
Discovery, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
`get_parameter_value <parameter>`

**Returns**
The value of the parameter.

**Arguments**

*parameter*  The name of the parameter whose value is being retrieved.

**Example**
```
set width [ get_parameter_value fifo_width ]
```

**Notes**
If `AFFECTS_ELABORATION` is false for a given parameter, `get_parameter_value` is not available for that parameter from the elaboration callback. If `AFFECTS_GENERATION` is false then it is not available from the generation callback.

**Related Information**
- `add_parameter` on page 614
- `get_parameter_property` on page 617
- `get_parameters` on page 615
- `set_parameter_property` on page 621
- `set_parameter_value` on page 622
7.1.2.6. get_string

**Description**

Returns the value of an externalized string previously loaded by the `load_strings` command.

**Availability**

Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**

get_string `<identifier>`

**Returns**

The externalized string.

**Arguments**

`identifier` The string identifier.

**Example**

hw.tcl:

```tcl
load_strings test.properties
set_module_property NAME test
set_module_property VERSION [get_string VERSION]
set_module_property DISPLAY_NAME [get_string DISPLAY_NAME]
add_parameter firepower INTEGER 0 ""
set_parameter_property firepower DISPLAY_NAME [get_string PARAM_DISPLAY_NAME]
set_parameter_property firepower TYPE INTEGER
set_parameter_property firepower DESCRIPTION [get_string PARAM_DESCRIPTION]
```

test.properties:

```properties
DISPLAY_NAME = Trogdor!
VERSION = 1.0
PARAM_DISPLAY_NAME = Firepower
PARAM_DESCRIPTION = The amount of force to use when breathing fire.
```

**Notes**

Use uppercase words separated with underscores to name string identifiers. If you are externalizing module properties, use the module property name for the string identifier:

```tcl
set_module_property DISPLAY_NAME [get_string DISPLAY_NAME]
```

If you are externalizing a parameter property, qualify the parameter property with the parameter name, with uppercase format, if needed:

```tcl
set_parameter_property my_param DISPLAY_NAME [get_string MY_PARAM_DISPLAY_NAME]
```

If you use a string to describe a string format, end the identifier with `_FORMAT`.

```tcl
set formatted_string [ format [ get_string TWO_ARGUMENT_MESSAGE_FORMAT ] "arg1" "arg2" ]
```

**Related Information**

load_strings on page 620
7.1.2.7. load_strings

**Description**
Loads strings from an external .properties file.

**Availability**
Discovery, Main Program

**Usage**
load_strings <path>

**Returns**
No return value.

**Arguments**

*path*  The path to the properties file.

**Example**

```tcl
hw.tcl:
load_strings test.properties
set_module_property NAME test
set_module_property VERSION [get_string VERSION]
set_module_property DISPLAY_NAME [get_string DISPLAY_NAME]
add_parameter firepower INTEGER 0 ""
set_parameter_property firepower DISPLAY_NAME [get_string PARAM_DISPLAY_NAME]
set_parameter_property firepower TYPE INTEGER
set_parameter_property firepower DESCRIPTION [get_string PARAM_DESCRIPTION]
```

```properties
<test.properties>
DISPLAY_NAME = Trogdor!
VERSION = 1.0
PARAM_DISPLAY_NAME = Firepower
PARAM_DESCRIPTION = The amount of force to use when breathing fire.
```

**Notes**

Refer to the Java Properties File for properties file format. A .properties file is a text file with `KEY=value` pairs. For externalized strings, the `KEY` is a string identifier and the `value` is the externalized string.

For example:

```
TROGDOR = A dragon with a big beefy arm
```

**Related Information**

- *get_string* on page 619
- *Java Properties File*
7.1.2.8. set_parameter_property

Description
Sets a single parameter property.

Availability
Main Program, Edit, Elaboration, Validation, Composition

Usage
set_parameter_property <parameter> <property> <value>

Returns

Arguments

parameter The name of the parameter that is being set.

property The name of the property. Refer to Parameter Properties.

value The new value for the property.

Example

set_parameter_property BAUD_RATE ALLOWED_RANGES {9600 19200 38400}

Related Information

- add_parameter on page 614
- get_parameter_properties on page 616
- set_parameter_property on page 621
- Parameter Properties on page 696
7.1.2.9. set_parameter_value

**Description**
Sets a parameter value. The value of a derived parameter can be updated by the IP component in the elaboration callback or the edit callback. Any changes to the value of a derived parameter in the edit callback is not preserved.

**Availability**
Edit, Elaboration, Validation, Composition, Parameter Upgrade

**Usage**

```
set_parameter_value <parameter> <value>
```

**Returns**
No return value.

**Arguments**

- `parameter`  The name of the parameter that is being set.
- `value`  Specifies the new parameter value.

**Example**

```
set_parameter_value half_clock_rate [ expr { [ get_parameter_value clock_rate ] / 2 } ]
```

7.1.3. Interconnect Parameters

- `set_domain_assignment` on page 622
- `get_domain_assignment` on page 623
- `get_domain_assignments` on page 623
- `set_postadaptation_assignment` on page 624
- `get_postadaptation_assignment` on page 624
- `get_postadaptation_assignments` on page 625

7.1.3.1. set_domain_assignment

**Description**
Sets the assignment value to all connections on the given domain.

**Availability**
Composition

**Usage**

```
set_domain_assignment <element> <assignment> <value>
```
Arguments

*element* Connection or interface in the domain to which you want to set the assignment. If the element name is `$system`, the assignment applies to all the domains in the system.

*assignment* The name of the assignment.

*value* The value of the assignment.

### 7.1.3.2. get_domain_assignment

**Description**
Returns the value for the specified assignment in the given domain.

**Availability**
Composition

**Usage**

```
get_domain_assignment <element> <assignment>
```

Arguments

*element* Connection or interface in the domain for which you want to get the assignment value.

*assignment* The name of the assignment.

### 7.1.3.3. get_domain_assignments

**Description**
Returns all domain assignments for the given domain as a list of strings. Each "group" of three elements in the list contains the element name, assignment name, and value, in that order. Element name in the output is the input element name. If the input element is `$system`, then the output element name is the connection point in the domain. The Returns section shows a typical list.

**Returns**

```
[element0 name0 value0 element1 name1 value1 ... ]
```

In TCL, you'd loop over the list by writing a `foreach` loop:

```
foreach {element name value} $requirement_list { puts "$element $name $value" }
```

**Availability**

Composition
Usage

get_domain_assignments <element>

Arguments

element  Connection or interface in the domains for which you want to get the assignments value. If you specify $system as the element, the command returns values of all the domains in the system.

7.1.3.4. set_postadaptation_assignment

Description
Adds an post adaptation interconnect assignment.

Availability
Composition

Usage

set_postadaptation_assignment <element> <assignment> <value>

Arguments

element  Connection or interface in the domain to which you want to set the assignment.

assignment  The name of the assignment.

value  The value of the assignment.

7.1.3.5. get_postadaptation_assignment

Description
Returns the value of the named post adaptation interconnect assignment on the specified element.

Availability
Composition

Usage

get_postadaptation_assignment <element> <assignment>

Arguments

element  Connection or interface in the domain for which you want to get the assignment value.

assignment  The name of the assignment.
7.1.3.6. get_postadaptation_assignments

**Description**
Returns all post adaptation interconnect assignments for the given domain as a list of strings. Each "group" of three elements in the list contains the element name, assignment name and value in that order. The \text{Returns} section shows a typical list.

**Returns**

```
[element0 name0 value0 element1 name1 value1 ... ]
```

In Tcl, you loop over the list by writing a foreach loop:

```
foreach {element name value} $requirement_list \
    { puts " $element $name $value" }
```

**Availability**
Composition

**Usage**

```
get_postadaptation_assignments <element>
```

**Arguments**

- `element` Connection or interface in the domain to which you want to set the assignment.
7.1.4. Display Items

add_display_item on page 627
get_display_items on page 629
get_display_item_properties on page 630
get_display_item_property on page 631
set_display_item_property on page 632
### 7.1.4.1. add_display_item

**Description**
Specifies the following aspects of the IP component display:

- Creates logical groups for an IP component's parameters. For example, to create separate groups for the IP component's timing, size, and simulation parameters. An IP component displays the groups and parameters in the order that you specify the display items in the _hw.tcl file.
- Groups a list of parameters to create multi-column tables.
- Specifies an image to provide representation of a parameter or parameter group.
- Creates a button by adding a display item of type action. The display item includes the name of the callback to run.

**Availability**
Main Program

**Usage**

```tcl
add_display_item <parent_group> <id> <type> [<args>]
```

**Returns**

**Arguments**

- `parent_group` Specifies the group to which a display item belongs
- `id` The identifier for the display item. If the item being added is a parameter, this is the parameter name. If the item is a group, this is the group name.
- `type` The type of the display item. Refer to Display Item Kind Properties.
- `args (optional)` Provides extra information required for display items.

**Example**

```tcl
add_display_item "Timing" read_latency PARAMETER
add_display_item "Sounds" speaker_image_id ICON speaker.jpg
```
Notes

The following examples illustrate further illustrate the use of arguments:

• `add_display_item groupName id icon path-to-image-file`
• `add_display_item groupName parameterName parameter`
• `add_display_item groupName id text "your-text"`
  The your-text argument is a block of text that is displayed in the GUI. Some simple HTML formatting is allowed, such as `<b>` and `<i>`, if the text starts with `<html>`.
• `add_display_item parentGroupName childGroupName group [tab]`
  The tab is an optional parameter. If present, the group appears in separate tab in the GUI for the instance.
• `add_display_item parentGroupName actionName action buttonClickCallbackProc`

Related Information

• `get_display_item_properties` on page 630
• `get_display_item_property` on page 631
• `get_display_items` on page 629
• `set_display_item_property` on page 632
• `Display Item Kind Properties` on page 704
7.1.4.2. get_display_items

Description
Returns a list of all items to be displayed as part of the parameterization GUI.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

Usage
get_display_items

Returns
List of display item IDs.

Arguments
No arguments.

Example
get_display_items

Related Information
- add_display_item on page 627
- get_display_item_properties on page 630
- get_display_item_property on page 631
- set_display_item_property on page 632
### 7.1.4.3. get_display_item_properties

**Description**
Returns a list of names of the properties of display items that are part of the parameterization GUI.

**Availability**
Main Program

**Usage**
get_display_item_properties

**Returns**
A list of display item property names. Refer to *Display Item Properties*.

**Arguments**
No arguments.

**Example**

```
get_display_item_properties
```

**Related Information**
- `add_display_item` on page 627
- `get_display_item_property` on page 631
- `set_display_item_property` on page 632
- *Display Item Properties* on page 703
7.1.4.4. get_display_item_property

**Description**
Returns the value of a specific property of a display item that is part of the parameterization GUI.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
get_display_item_property <display_item> <property>

**Returns**
The value of a display item property.

**Arguments**

*display_item*  The id of the display item.

*property*  The name of the property. Refer to Display Item Properties.

**Example**
set my_label [get_display_item_property my_action DISPLAY_NAME]

**Related Information**
- add_display_item on page 627
- get_display_item_properties on page 630
- get_display_items on page 629
- set_display_item_property on page 632
- Display Item Properties on page 703
7.1.4.5. set_display_item_property

**Description**
Sets the value of specific property of a display item that is part of the parameterization GUI.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Composition

**Usage**
set_display_item_property <display_item> <property> <value>

**Returns**
No return value.

**Arguments**

*display_item*  The name of the display item whose property value is being set.

*property*    The property that is being set. Refer to *Display Item Properties*.

*value*    The value to set.

**Example**

```
set_display_item_property my_action DISPLAY_NAME "Click Me"
set_display_item_property my_action DESCRIPTION "clicking this button runs the click_me_callback proc in the hw.tcl file"
```

**Related Information**

- [add_display_item](#) on page 627
- [get_display_item_properties](#) on page 630
- [get_display_item_property](#) on page 631
- Display Item Properties on page 703
7. Component Interface Tcl Reference

7.1.5. Module Definition

add_documentation_link on page 634
get_module_assignment on page 635
get_module_assignments on page 636
get_module_ports on page 637
get_module_properties on page 638
get_module_property on page 639
send_message on page 640
set_module_assignment on page 641
set_module_property on page 642
add_hdl_instance on page 643
package on page 644
7.1.5.1. add_documentation_link

**Description**
Allows you to link to documentation for your IP component.

**Availability**
Discovery, Main Program

**Usage**

```
add_documentation_link <title> <path>
```

**Returns**
No return value.

**Arguments**

*title* The title of the document for use on menus and buttons.

*path* A path to the IP component documentation, using a syntax that provides the entire URL, not a relative path. For example: `http://www.mydomain.com/my_memory_controller.html` or `file:///datasheet.txt`

**Example**

```
```
7.1.5.2. get_module_assignment

**Description**
This command returns the value of an assignment. You can use the get_module_assignment and set_module_assignment and the get_interface_assignment and set_interface_assignment commands to provide information about the IP component to embedded software tools and applications.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
get_module_assignment <assignment>

**Returns**
The value of the assignment

**Arguments**

assignment  The name of the assignment whose value is being retrieved

**Example**

get_module_assignment embeddedsw.CMacro.colorSpace

**Related Information**
- get_module_assignments on page 636
- set_module_assignment on page 641
7.1.5.3. get_module_assignments

**Description**
Returns the names of the module assignments.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
get_module_assignments

**Returns**
A list of assignment names.

**Arguments**
No arguments.

**Example**
get_module_assignments

**Related Information**
- get_module_assignment on page 635
- set_module_assignment on page 641
7.1.5.4. get_module_ports

**Description**
Returns a list of the names of all the ports which are currently defined.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_module_ports

**Returns**
A list of port names.

**Arguments**
No arguments.

**Example**

get_module_ports

**Related Information**
- add_interface on page 596
- add_interface_port on page 598
7.1.5.5. get_module_properties

**Description**
Returns the names of all the module properties as a list of strings. You can use the `get_module_property` and `set_module_property` commands to get and set values of individual properties. The value returned by this command is always the same for a particular version of Platform Designer.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_module_properties

**Returns**
List of strings. Refer to *Module Properties*.

**Arguments**
No arguments.

**Example**
```
get_module_properties
```

**Related Information**
- `get_module_property` on page 639
- `set_module_property` on page 642
- *Module Properties* on page 706
7.1.5.6. get_module_property

**Description**
Returns the value of a single module property.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_module_property <property>

**Returns**
Various.

**Arguments**

*property*  The name of the property, Refer to *Module Properties*.

**Example**

```
set my_name [ get_module_property NAME ]
```

**Related Information**
- get_module_properties on page 638
- set_module_property on page 642
- Module Properties on page 706
7.1.5.7. send_message

**Description**
Sends a message to the user of the IP component. The message text is normally interpreted as HTML. You can use the `<b>` element to provide emphasis. If you do not want the message text to be interpreted as HTML, then pass a list as the message level, for example, `{ Info Text }`.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
```
send_message <level> <message>
```

**Returns**
No return value.

**Arguments**

*level*  The following message levels are supported:

- **ERROR**--Provides an error message. The Platform Designer system cannot be generated with existing error messages.
- **WARNING**--Provides a warning message.
- **INFO**--Provides an informational message. The **INFO** level is not available in the Main Program.
- **PROGRESS**--Reports progress during generation.
- **DEBUG**--Provides a debug message when debug mode is enabled.

*message*  The text of the message.

**Example**
```
send_message ERROR "The system is down!"
send_message { Info Text } "The system is up!"
```
7.1.5.8. set_module_assignment

Description
Sets the value of the specified assignment.

Availability
Main Program, Elaboration, Validation, Composition

Usage
set_module_assignment <assignment> [ <value> ]

Returns
No return value.

Arguments

assignment The assignment whose value is being set

value (optional) The value of the assignment

Example
set_module_assignment embeddedsw.CMacro.colorSpace CMYK

Related Information
- get_module_assignment on page 635
- get_module_assignments on page 636
7.1.5.9. set_module_property

**Description**
Allows you to set the values for module properties.

**Availability**
Discovery, Main Program

**Usage**
set_module_property <property> <value>

**Returns**
No return value.

**Arguments**

property The name of the property. Refer to Module Properties.

value The new value of the property.

**Example**

```
set_module_property VERSION 10.0
```

**Related Information**
- get_module_properties on page 638
- get_module_property on page 639
- Module Properties on page 706
7.1.5.10. add_hdl_instance

**Description**

Adds an instance of a predefined module, referred to as a *child or child instance*. The HDL entity generated from this instance can be instantiated and connected within this IP component’s HDL.

**Availability**

Main Program, Elaboration, Composition

**Usage**

```
add_hdl_instance <entity_name> <ip_type> [<version>]
```

**Returns**

The entity name of the added instance.

**Arguments**

- `entity_name`  
  Specifies a unique local name that you can use to manipulate the instance. This name is used in the generated HDL to identify the instance.

- `ip_type`  
  The type refers to a kind of instance available in the IP Catalog, for example `altera_avalon_uart`.

- `version (optional)`  
  The required version of the specified instance type. If no version is specified, the latest version is used.

**Example**

```
add_hdl_instance my_uart altera_avalon_uart
```

**Related Information**

- `get_instance_parameter_value` on page 661
- `get_instance_parameters` on page 659
- `get_instances` on page 651
- `set_instance_parameter_value` on page 664
7.1.5.11. package

**Description**

Allows you to specify a particular version of the Platform Designer software to avoid software compatibility issues, and to determine which version of the `_hw.tcl` API to use for the IP component. You must use the package command at the beginning of your `_hw.tcl` file.

**Availability**

Main Program

**Usage**

```
package require -exact qsys <version>
```

**Returns**

No return value

**Arguments**

*version*  The version of Platform Designer that you require, such as 14.1.

**Example**

```
package require -exact qsys 14.1
```
7.1.6. Composition

add_instance on page 646
add_connection on page 647
get_connections on page 648
get_connection_parameters on page 649
get_connection_parameter_value on page 650
get_instances on page 651
get_instance_interfaces on page 652
get_instance_interface_ports on page 653
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set_instance_property on page 656
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get_instance_interface_property on page 658
get_instance_parameters on page 659
get_instance_parameter_property on page 660
get_instance_parameter_value on page 661
get_instance_port_property on page 662
set_connection_parameter_value on page 663
set_instance_parameter_value on page 664
7.1.6.1. add_instance

**Description**
Adds an instance of an IP component, referred to as a child or child instance to the subsystem. You can use this command to create IP components that are composed of other IP component instances. The HDL for this subsystem generates; There is no need to write custom HDL for the IP component.

**Availability**
Main Program, Composition

**Usage**
```
add_instance <name> <type> [<<version>>]
```

**Returns**
No return value.

**Arguments**
- **name** Specifies a unique local name that you can use to manipulate the instance. This name is used in the generated HDL to identify the instance.

- **type** The type refers to a type available in the IP Catalog, for example `altera_avalon_uart`.

- **version (optional)** The required version of the specified type. If no version is specified, the highest available version is used.

**Example**
```
add_instance my_uart altera_avalon_uart
add_instance my_uart altera_avalon_uart 14.1
```

**Related Information**
- [add_connection](#) on page 647
- [get_instance_interface_property](#) on page 658
- [get_instance_parameter_value](#) on page 661
- [get_instance_parameters](#) on page 659
- [get_instance_property](#) on page 655
- [get_instances](#) on page 651
- [set_instance_parameter_value](#) on page 664
7.1.6.2. add_connection

**Description**
Connects the named interfaces on child instances together using an appropriate connection type. Both interface names consist of a child instance name, followed by the name of an interface provided by that module. For example, `mux0.out` is the interface named `out` on the instance named `mux0`. Be careful to connect the start to the end, and not the other way around.

**Availability**
Main Program, Composition

**Usage**
```
add_connection <start> [<end> <kind> <name>]
```

**Returns**
The name of the newly added connection in `start.point/end.point` format.

**Arguments**

- **start**  The start interface to be connected, in `<instance_name>.<interface_name>` format.

- **end (optional)**  The end interface to be connected, `<instance_name>.<interface_name>`.

- **kind (optional)**  The type of connection, such as `avalon` or `clock`.

- **name (optional)**  A custom name for the connection. If unspecified, the name will be `<start_instance>.<interface>.<end_instance><interface>.

**Example**
```
add_connection dma.read_master sdram.s1 avalon
```

**Related Information**
- [add_instance](#) on page 646
- [get_instance_interfaces](#) on page 652
7.1.6.3. get_connections

**Description**
Returns a list of all connections in the composed subsystem.

**Availability**
Main Program, Composition

**Usage**
get_connections

**Returns**
A list of connections.

**Arguments**
No arguments.

**Example**
```
set all_connections [ get_connections ]
```

**Related Information**
add_connection on page 647
7.1.6.4. get_connection_parameters

**Description**
Returns a list of parameters found on a connection.

**Availability**
Main Program, Composition

**Usage**
get_connection_parameters <connection>

**Returns**
A list of parameter names

**Arguments**

connection The connection to query.

**Example**

```
get_connection_parameters cpu.data_master/dma0.csr
```

**Related Information**
- add_connection on page 647
- get_connection_parameter_value on page 650
7.1.6.5. get_connection_parameter_value

Description
Returns the value of a parameter on the connection. Parameters represent aspects of the connection that can be modified once the connection is created, such as the base address for an Avalon Memory Mapped connection.

Availability
Composition

Usage
get_connection_parameter_value <connection> <parameter>

Returns
The value of the parameter.

Arguments

connection  The connection to query.

parameter  The name of the parameter.

Example

get_connection_parameter_value cpu.data_master/dma0.csr baseAddress

Related Information
• add_connection on page 647
• get_connection_parameters on page 649
7. Component Interface Tcl Reference

7.1.6.6. get_instances

Description
Returns a list of the instance names for all child instances in the system.

Availability
Main Program, Elaboration, Validation, Composition

Usage
get_instances

Returns
A list of child instance names.

Arguments
No arguments.

Example
get_instances

Notes
This command can be used with instances created by either add_instance or add_hdl_instance.

Related Information
- add_hdl_instance on page 643
- add_instance on page 646
- get_instance_parameter_value on page 661
- get_instance_parameters on page 659
- set_instance_parameter_value on page 664
7.1.6.7. get_instance_interfaces

Description
Returns a list of interfaces found in a child instance. The list of interfaces can change if the parameterization of the instance changes.

Availability
Validation, Composition

Usage
get_instance_interfaces \textless instance \textgreater

Returns
A list of interface names.

Arguments
\textit{instance} The name of the child instance.

Example
\begin{verbatim}
get_instance_interfaces pixel_converter
\end{verbatim}

Related Information
- \texttt{add_instance} on page 646
- \texttt{get_instance_interface_ports} on page 653
- \texttt{get_instance_interfaces} on page 652
### 7. Component Interface Tcl Reference

#### 7.1.6.8. get_instance_interface_ports

**Description**
Returns a list of ports found in an interface of a child instance.

**Availability**
Validation, Composition, Fileset Generation

**Usage**
get_instance_interface_ports <instance> <interface>

**Returns**
A list of port names found in the interface.

**Arguments**

*instance*   The name of the child instance.

*interface*  The name of an interface on the child instance.

**Example**

```tcl
set port_names [ get_instance_interface_ports cpu data_master ]
```

**Related Information**

- [add_instance](#) on page 646
- [get_instance_interfaces](#) on page 652
- [get_instance_port_property](#) on page 662
7.1.6.9. get_instance_interface_properties

**Description**

Returns the names of all of the properties of the specified interface.

**Availability**

Validation, Composition

**Usage**

get_instance_interface_properties <instance> <interface>

**Returns**

List of property names.

**Arguments**

*instance*  The name of the child instance.

*interface*  The name of an interface on the instance.

**Example**

```
set properties [ get_instance_interface_properties cpu data_master ]
```

**Related Information**

- add_instance on page 646
- get_instance_interface_property on page 658
- get_instance_interfaces on page 652
7.1.6.10. get_instance_property

**Description**
Returns the value of a single instance property.

**Availability**
Main Program, Elaboration, Validation, Composition, Fileset Generation

**Usage**
get_instance_property <instance> <property>

**Returns**
Various.

**Arguments**

*instance*  The name of the instance.

*property*  The name of the property. Refer to *Instance Properties*.

**Example**

```tcl
set my_name [ get_instance_property myinstance NAME ]
```

**Related Information**
- add_instance on page 646
- get_instance_properties on page 657
- set_instance_property on page 656
- Instance Properties on page 695
7.1.6.11. set_instance_property

**Description**
Allows a user to set the properties of a child instance.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
set_instance_property <instance> <property> <value>

**Returns**

**Arguments**

*instance*   The name of the instance.

*property*   The name of the property to set. Refer to Instance Properties.

*value*   The new property value.

**Example**

```
set_instance_property myinstance SUPRESS_ALL_WARNINGS true
```

**Related Information**

- add_instance on page 646
- get_instance_properties on page 657
- get_instance_property on page 655
- Instance Properties on page 695
7.1.6.12. get_instance_properties

**Description**

Returns the names of all the instance properties as a list of strings. You can use the get_instance_property and set_instance_property commands to get and set values of individual properties. The value returned by this command is always the same for a particular version of Platform Designer

**Availability**

Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**

get_instance_properties

**Returns**

List of strings. Refer to *Instance Properties*.

**Arguments**

No arguments.

**Example**

get_instance_properties

**Related Information**

- add_instance on page 646
- get_instance_property on page 655
- set_instance_property on page 656
- Instance Properties on page 695
7.1.6.13. get_instance_interface_property

Description
Returns the value of a property for an interface in a child instance.

Availability
Validation, Composition

Usage
get_instance_interface_property <instance> <interface> <property>

Returns
The value of the property.

Arguments

instance The name of the child instance.

interface The name of an interface on the child instance.

property The name of the property of the interface.

Example

set value [ get_instance_interface_property cpu data_master setupTime ]

Related Information
- add_instance on page 646
- get_instance_interfaces on page 652
7.1.6.14. get_instance_parameters

**Description**
Returns a list of names of the parameters on a child instance that can be set using `set_instance_parameter_value`. It omits parameters that are derived and those that have the `SYSTEM_INFO` parameter property set.

**Availability**
Main Program, Elaboration, Validation, Composition

**Usage**
get_instance_parameters `<instance>`

**Returns**
A list of parameters in the instance.

**Arguments**

`instance` The name of the child instance.

**Example**
```
set parameters [ get_instance_parameters instance ]
```

**Notes**
You can use this command with instances created by either `add_instance` or `add_hdl_instance`.

**Related Information**
- `add_hdl_instance` on page 643
- `add_instance` on page 646
- `get_instance_parameter_value` on page 661
- `get_instances` on page 651
- `set_instance_parameter_value` on page 664
7.1.6.15. get_instance_parameter_property

**Description**
Returns the value of a property on a parameter in a child instance. Parameter properties are metadata that describe how the Platform Designer tools use the parameter.

**Availability**
Validation, Composition

**Usage**
get_instance_parameter_property <instance> <parameter> <property>

**Returns**
The value of the parameter property.

**Arguments**

*instance*   The name of the child instance.

*parameter*  The name of the parameter in the instance.

*property*   The name of the property of the parameter. Refer to Parameter Properties.

**Example**
get_instance_parameter_property instance parameter property

**Related Information**
- add_instance on page 646
- Parameter Properties on page 696
7.1.6.16. get_instance_parameter_value

Description
Returns the value of a parameter in a child instance. You cannot use this command to get the value of parameters whose values are derived or those that are defined using the SYSTEM_INFO parameter property.

Availability
Elaboration, Validation, Composition

Usage
get_instance_parameter_value <instance> <parameter>

Returns
The value of the parameter.

Arguments

instance  The name of the child instance.

parameter  Specifies the parameter whose value is being retrieved.

Example

set dpi [ get_instance_parameter_value pixel_converter input_DPI ]

Notes
You can use this command with instances created by either add_instance or add_hdl_instance.

Related Information
• add_hdl_instance on page 643
• add_instance on page 646
• get_instance_parameters on page 659
• get_instances on page 651
• set_instance_parameter_value on page 664
7.1.6.17. `get_instance_port_property`

**Description**
Returns the value of a property of a port contained by an interface in a child instance.

**Availability**
Validation, Composition, Fileset Generation

**Usage**

```
get_instance_port_property <instance> <port> <property>
```

**Returns**
The value of the property for the port.

**Arguments**

- `instance` The name of the child instance.
- `port` The name of a port in one of the interfaces on the child instance.
- `property` The property whose value is being retrieved. Only the following port properties can be queried on ports of child instances: ROLE, DIRECTION, WIDTH, WIDTH_EXPR and VHDL_TYPE. Refer to Port Properties.

**Example**
```
get_instance_port_property instance port property
```

**Related Information**
- `add_instance` on page 646
- `get_instance_interface_ports` on page 653
- Port Properties on page 700
7.1.6.18. set_connection_parameter_value

Description
Sets the value of a parameter of the connection. The start and end are each interface names of the format `<instance>.<interface>`. Connection parameters depend on the type of connection, for Avalon memory mapped they include base addresses and arbitration priorities.

Availability
Main Program, Composition

Usage
set_connection_parameter_value <connection> <parameter> <value>

Returns
No return value.

Arguments

connection  Specifies the name of the connection as returned by the add_connection command. It is of the form start.point/end.point.

parameter  The name of the parameter.

value  The new parameter value.

Example

set_connection_parameter_value cpu.data_master/dma0.csr baseAddress "0x000a0000"

Related Information

- add_connection on page 647
- get_connection_parameter_value on page 650
7.1.6.19. set_instance_parameter_value

**Description**
Sets the value of a parameter for a child instance. Derived parameters and SYSTEM_INFO parameters for the child instance cannot be set with this command.

**Availability**
Main Program, Elaboration, Composition

**Usage**
```
set_instance_parameter_value <instance> <parameter> <value>
```

**Returns**
Vo return value.

**Arguments**

*instance*  Specifies the name of the child instance.

*parameter*  Specifies the parameter that is being set.

*value*  Specifies the new parameter value.

**Example**
```
set_instance_parameter_value uart_0 baudRate 9600
```

**Notes**
You can use this command with instances created by either `add_instance` or `add_hdl_instance`.

**Related Information**
- `add_hdl_instance` on page 643
- `add_instance` on page 646
- `get_instance_parameter_value` on page 661
- `get_instances` on page 651
7.1.7. Fileset Generation

- `add_fileset` on page 666
- `add_fileset_file` on page 667
- `set_fileset_property` on page 668
- `get_fileset_file_attribute` on page 669
- `set_fileset_file_attribute` on page 670
- `get_fileset_properties` on page 671
- `get_fileset_property` on page 672
- `get_fileset_sim_properties` on page 673
- `set_fileset_sim_properties` on page 674
- `create_temp_file` on page 675
7.1.7.1. add_fileset

**Description**

Adds a generation fileset for a particular target as specified by the `kind`. Platform Designer calls the target (SIM_VHDL, SIM_VERILOG, QUARTUS_SYNTH, or EXAMPLE_DESIGN) when the specified generation target is requested. You can define multiple filesets for each kind of fileset. Platform Designer passes a single argument to the specified callback procedure. The value of the argument is a generated name, which you must use in the top-level module or entity declaration of your IP component. To override this generated name, you can set the fileset property `TOP_LEVEL`.

**Availability**

Main Program

**Usage**

```
add_fileset <name> <kind> [<callback_proc> <display_name>]
```

**Returns**

No return value.

**Arguments**

- **name**  The name of the fileset.
- **kind**  The kind of fileset. Refer to Fileset Properties.
- **callback_proc** (optional)  A string identifying the name of the callback procedure. If you add files in the global section, you can then specify a blank callback procedure.
- **display_name (optional)**  A display string to identify the fileset.

**Example**

```
add_fileset my_synthesis_fileset QUARTUS_SYNTH mySynthCallbackProc "My Synthesis"
proc mySynthCallbackProc { topLevelName } { ... }
```

**Notes**

If using the `TOP_LEVEL` fileset property, all parameterizations of the component must use identical HDL.

**Related Information**

- `add_fileset_file` on page 667
- `get_fileset_property` on page 672
- Fileset Properties on page 708
7.1.7.2. add_fileset_file

Description
Adds a file to the generation directory. You can specify source file locations with either an absolute path, or a path relative to the IP component's _hw.tcl file. When you use the add_fileset_file command in a fileset callback, the Intel Quartus Prime software compiles the files in the order that they are added.

Availability
Main Program, Fileset Generation

Usage
add_fileset_file <output_file> <file_type> <file_source> <path_or_contents> [<attributes>]

Returns
No return value.

Arguments

output_file  Specifies the location to store the file after Platform Designer generation

file_type  The kind of file. Refer to File Kind Properties.

file_source  Specifies whether the file is being added by path, or by file contents. Refer to File Source Properties.

path_or_contents  When the file_source is PATH, specifies the file to be copied to output_file. When the file_source is TEXT, specifies the text contents to be stored in the file.

attributes (optional)  An optional list of file attributes. Typically used to specify that a file is intended for use only in a particular simulator. Refer to File Attribute Properties.

Example

add_fileset_file "./implementation/rx_pma.sv" SYSTEM_VERILOG PATH
synth_rx_pma.sv
add_fileset_file gui.sv SYSTEM_VERILOG TEXT "Customize your IP core"

Related Information
- add_fileset on page 666
- get_fileset_file_attribute on page 669
- File Kind Properties on page 712
- File Source Properties on page 713
- File Attribute Properties on page 711
7.1.7.3. set_fileset_property

Description
Allows you to set the properties of a fileset.

Availability
Main Program, Elaboration, Fileset Generation

Usage
set_fileset_property <fileset> <property> <value>

Returns
No return value.

Arguments

fileset  The name of the fileset.

property  The name of the property to set. Refer to Fileset Properties.

value  The new property value.

Example
set_fileset_property mySynthFileset TOP_LEVEL simple_uart

Notes
When a fileset callback is called, the callback procedure is passed a single argument. The value of this argument is a generated name which must be used in the top-level module or entity declaration of your IP component. If set, the TOP_LEVEL specifies a fixed name for the top-level name of your IP component.

The TOP_LEVEL property must be set in the global section. It cannot be set in a fileset callback.

If using the TOP_LEVEL fileset property, all parameterizations of the IP component must use identical HDL.

Related Information
•  add_fileset on page 666
•  Fileset Properties on page 708
7.1.7.4. get_fileset_file_attribute

**Description**
Returns the attribute of a fileset file.

**Availability**
Main Program, Fileset Generation

**Usage**
get_fileset_file_attribute <output_file> <attribute>

**Returns**
Value of the fileset File attribute.

**Arguments**

*output_file*  Location of the output file.

*attribute*  Specifies the name of the attribute Refer to *File Attribute Properties*.

**Example**

get_fileset_file_attribute my_file.sv ALDEC_SPECIFIC

**Related Information**
- add_fileset on page 666
- add_fileset_file on page 667
- get_fileset_file_attribute on page 669
- File Attribute Properties on page 711
- add_fileset on page 666
- add_fileset_file on page 667
- get_fileset_file_attribute on page 669
- File Attribute Properties on page 711
7.1.7.5. set_fileset_file_attribute

**Description**
Sets the attribute of a fileset file.

**Availability**
Main Program, Fileset Generation

**Usage**
set_fileset_file_attribute <output_file> <attribute> <value>

**Returns**
The attribute value if it was set.

**Arguments**

- **output_file**  Location of the output file.

- **attribute**  Specifies the name of the attribute Refer to File Attribute Properties.

- **value**  Value to set the attribute to.

**Example**

```
set_fileset_file_attribute my_file_pkg.sv COMMON_SYSTEMVERILOG_PACKAGE my_file_package
```
7.1.7.6. get_fileset_properties

**Description**
Returns a list of properties that can be set on a fileset.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Generation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
get_fileset_properties

**Returns**
A list of property names. Refer to *Fileset Properties*.

**Arguments**
No arguments.

**Example**

get_fileset_properties

**Related Information**
- add_fileset on page 666
- get_fileset_properties on page 671
- set_fileset_property on page 668
- Fileset Properties on page 708
7.1.7.7. get_fileset_property

Description
Returns the value of a fileset property for a fileset.

Availability
Main Program, Elaboration, Fileset Generation

Usage
get_fileset_property <fileset> <property>

Returns
The value of the property.

Arguments

fileset  The name of the fileset.

property  The name of the property to query. Refer to Fileset Properties.

Example
get_fileset_property fileset property

Related Information
Fileset Properties on page 708
7.1.7.8. get_fileset_sim_properties

**Description**
Returns simulator properties for a fileset.

**Availability**
Main Program, Fileset Generation

**Usage**
get_fileset_sim_properties `<fileset>` `<platform>` `<property>`

**Returns**
The fileset simulator properties.

**Arguments**

`fileset` The name of the fileset.

`platform` The operating system that applies to the property. Refer to *Operating System Properties*.

`property` Specifies the name of the property to set. Refer to *Simulator Properties*.

**Example**
get_fileset_sim_properties my_fileset LINUX64 OPT_CADENCE_64BIT

**Related Information**
- [add_fileset](#) on page 666
- [set_fileset_sim_properties](#) on page 674
- [Operating System Properties](#) on page 720
- [Simulator Properties](#) on page 714
7.1.7.9. set_fileset_sim_properties

**Description**
Sets simulator properties for a given fileset

**Availability**
Main Program, Fileset Generation

**Usage**
set_fileset_sim_properties <fileset> <platform> <property> <value>

**Returns**
The fileset simulator properties if they were set.

**Arguments**

=fileset The name of the fileset.

=platform The operating system that applies to the property. Refer to Operating System Properties.

=property Specifies the name of the property to set. Refer to Simulator Properties.

=value Specifies the value of the property.

**Example**

set_fileset_sim_properties my_fileset LINUX64 OPT_MENTOR_PLI "\{libA\} \{libB\}"

**Related Information**

- get_fileset_sim_properties on page 673
- Operating System Properties on page 720
- Simulator Properties on page 714
7.1.7.10. create_temp_file

Description
Creates a temporary file, which you can use inside the fileset callbacks of a _hw.tcl file. This temporary file is included in the generation output if it is added using the add_fileset_file command.

Availability
Fileset Generation

Usage
create_temp_file <path>

Returns
The path to the temporary file.

Arguments

path  The name of the temporary file.

Example

set filelocation [create_temp_file "/hdl/compute_frequency.v"
add_fileset_file compute_frequency.v VERILOG PATH ${filelocation}

Related Information
•  add_fileset on page 666
•  add_fileset_file on page 667
7.1.8. Miscellaneous

check_device_family_equivalence on page 677
get_device_family_displayname on page 678
get_qip_strings on page 679
set_qip_strings on page 680
7.1.8.1. check_device_family_equivalence

**Description**
Returns 1 if the device family is equivalent to one of the families in the device families list. Returns 0 if the device family is not equivalent to any families. This command ignores differences in capitalization and spaces.

**Availability**
Discovery, Main Program, Edit, Elaboration, Validation, Composition, Fileset Generation, Parameter Upgrade

**Usage**
check_device_family_equivalence <device_family> <device_family_list>

**Returns**
1 if equivalent, 0 if not equivalent.

**Arguments**

*device_family*  The device family name that is being checked.

*device_family_list*  The list of device family names to check against.

**Example**
check_device_family_equivalence "CYLCONE III LS" { "stratixv" "Cyclone IV" "cycloneiiIs" }

**Related Information**
get_device_family_displayname on page 678
7.1.8.2. get_device_family_displayname

Description
Returns the display name of a given device family.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Composition, Fileset Generation, Parameter Upgrade

Usage
get_device_family_displayname <device_family>

Returns
The preferred display name for the device family.

Arguments

device_family  A device family name.

Example

get_device_family_displayname cycloneiiils ( returns: "Cyclone IV LS" )

Related Information
check_device_family_equivalence on page 677
7. Component Interface Tcl Reference

7.1.8.3. get_qip_strings

Description
Returns a Tcl list of QIP strings for the IP component.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Composition, Parameter Upgrade

Usage
get_qip_strings

Returns
A Tcl list of qip strings set by this IP component.

Arguments
No arguments.

Example
set strings [ get_qip_strings ]

Related Information
set_qip_strings on page 680
7.1.8.4. set_qip_strings

Description
Places strings in the Intel Quartus Prime IP File (.qip) file, which Platform Designer passes to the command as a Tcl list. You add the .qip file to your Intel Quartus Prime project on the Files page, in the Settings dialog box. Successive calls to set_qip_strings are not additive and replace the previously declared value.

Availability
Discovery, Main Program, Edit, Elaboration, Validation, Composition, Parameter Upgrade

Usage
set_qip_strings <qip_strings>

Returns
The Tcl list which was set.

Arguments
qip_strings A space-delimited Tcl list.

Example
```
set_qip_strings {"QIP Entry 1" "QIP Entry 2"}
```

Notes
You can use the following macros in your QIP strings entry:

- `%entityName%` The generated name of the entity replaces this macro when the string is written to the .qip file.
- `%libraryName%` The compilation library this IP component was compiled into is inserted in place of this macro inside the .qip file.
- `%instanceName%` The name of the instance is inserted in place of this macro inside the .qip file.

Related Information
get_qip_strings on page 679
7.1.9. SystemVerilog Interface Commands

- `add_sv_interface` on page 682
- `get_sv_interfaces` on page 683
- `get_sv_interface_property` on page 684
- `get_sv_interface_properties` on page 685
- `set_sv_interface_property` on page 686
7.1.9.1. add_sv_interface

Description
Adds a SystemVerilog interface to the IP component.

Availability
Elaboration, Global

Usage
add_sv_interface <sv_interface_name> <sv_interface_type>

Returns
No return value.

Arguments

sv_interface_name  The name of the SystemVerilog interface in the IP component.

sv_interface_type  The type of the SystemVerilog interface used by the IP component.

Example

add_sv_interface my_sv_interface my_sv_interface_type
7.1.9.2. get sv interfaces

**Description**
Returns the list of SystemVerilog interfaces in the IP component.

**Availability**
Elaboration, Global

**Usage**
get sv interfaces

**Returns**
String[] Returns the list of SystemVerilog interfaces defined in the IP component.

**Arguments**
No arguments.

**Example**
get sv interfaces
7.1.9.3. get_sv_interface_property

**Description**
Returns the value of a single SystemVerilog interface property from the specified interface.

**Availability**
Elaboration, Global

**Usage**
get_sv_interface_property <sv_interface_name> <sv_interface_property>

**Returns**

*various*  The property value.

**Arguments**

*sv_interface_name*  The name of a SystemVerilog interface of the system.

*sv_interface_property*  The name of the property. Refer to *System Verilog Interface Properties*.

**Example**

```
get_sv_interface_property my_sv_interface USE_ALL_PORTS
```
7.1.9.4. get_sv_interface_properties

**Description**
Returns the names of all the available SystemVerilog interface properties common to all interface types.

**Availability**
Elaboration, Global

**Usage**
get_sv_interface_properties

**Returns**

*String[]* The list of SystemVerilog interface properties.

**Arguments**
No arguments.

**Example**

get_sv_interface_properties
7.1.9.5. set_sv_interface_property

**Description**
Sets the value of a property on a SystemVerilog interface.

**Availability**
Elaboration, Global

**Usage**
```
set_sv_interface_property <sv_interface_name> <sv_interface_property> <value>
```

**Returns**
No return value.

**Arguments**

*interface*  The name of a SystemVerilog interface.

*sv_interface_property*  The name of the property. Refer to SystemVerilog Interface Properties.

*value*  The property value.

**Example**
```
set_sv_interface_property my_sv_interface USE_ALL_PORTS True
```
7.1.10. Wire-Level Expression Commands

set_wirelevel_expression on page 563
get_wirelevel_expressions on page 563
remove_wirelevel_expressions on page 564
7.1.10.1. set_wirelevel_expression

Description
Applies a wire-level expression to an optional input port or instance in the system.

Usage
set_wirelevel_expression <instance_or_port_bitselection> <expression>

Returns
No return value.

Arguments

instance_or_port_bitselection Specify the instance or port to which the wire-level expression using the 
<instance_name>..<port_name>[<bit_selection>] format. The bit selection can be a bit-select, for example [0], or a partial range defined in descending order, for example [7:0]. If no bit selection is specified, the full range of the port is selected.

expression The expression to be applied to an optional input port.

Examples

set_wirelevel_expression {module0.portA[7:0]} "8'b0"
set_wirelevel_expression module0.portA "8'b0"
set_wirelevel_expression {module0.portA[0]} "1'b0"

Related Information
- Scripting Wire-Level Expressions on page 48
- Wire-Level Connectivity on page 43
7.1.10.2. get_wirelevel_expressions

**Description**
Retrieve a list of wire-level expressions from an optional input port, instance, or all expressions in the current level of system hierarchy. If the port *bit selection* is specified as an argument, the range must be identical to what was used in the *set_wirelevel_expression* statement.

**Usage**

get_wirelevel_expressions <instance_or_port_bitselection>

**Returns**

`String[]` A flattened list of wire-level expressions. Every item in the list consists of right- and left-hand clauses of a wire-level expression. You can loop over the returned list using `foreach(port expr) $return_list{}`.

**Arguments**

`instance_or_port_bitselection` Specifies which instance or port from which a list of wire-level expressions are retrieved using the `<instance_name>..<port_name>[<bit_selection>]` format.

- If no `<port_name>[<bit_selection>]` is specified, the command causes the return of all expressions from the specified instance.
- If no argument is present, the command causes the return of all expressions from the current level of system hierarchy.

The *bit selection* can be a bit-select, for example `[0]`, or a partial range defined in descending order, for example `[7:0]`. If no *bit selection* is specified, the full range of the port is selected.

**Example**

get_wirelevel_expressions
get_wirelevel_expressions module0
get_wirelevel_expressions {module0.portA[7:0]}

**Related Information**
- [Scripting Wire-Level Expressions](#) on page 48
- [Wire-Level Connectivity](#) on page 43
7.1.10.3. remove_wirelevel_expressions

**Description**
Remove a list of wire-level expressions from an optional input port, instance, or all expressions in the current level of system hierarchy. If the port *bit selection* is specified as an argument, the range must be identical to what was used in the *set_wirelevel_expressions* statement.

**Usage**
remove_wirelevel_expressions <instance_or_port_bitselection>

**Returns**
No return value.

**Arguments**

*instance_or_port_bitselection*  
Specifies which instance or port from which a list of wire-level expressions are removed using the *
<instance_name>.<port_name>[<bit_selection>]*
format.

- If no *
<port_name>[<bit_selection>]*
is specified, the command causes the removal of all expressions from the specified instance.
- If no argument is present, the command causes the return of all expressions from the current level of system hierarchy.

The *bit selection* can be a bit-select, for example [0], or a partial range defined in descending order, for example [7:0]. If no *bit selection* is specified, the full range of the port is selected.

**Examples**
remove_wirelevel_expressions  
remove_wirelevel_expressions module0  
remove_wirelevel_expressions {module0.portA[7:0]}

**Related Information**
- *Scripting Wire-Level Expressions* on page 48  
- *Wire-Level Connectivity* on page 43
7.2. Platform Designer _hw.tcl Property Reference

- **Script Language Properties** on page 692
- **Interface Properties** on page 693
- **SystemVerilog Interface Properties** on page 693
- **Instance Properties** on page 695
- **Parameter Properties** on page 696
- **Parameter Type Properties** on page 698
- **Parameter Status Properties** on page 699
- **Port Properties** on page 700
- **Direction Properties** on page 702
- **Display Item Properties** on page 703
- **Display Item Kind Properties** on page 704
- **Display Hint Properties** on page 705
- **Module Properties** on page 706
- **Fileset Properties** on page 708
- **Fileset Kind Properties** on page 709
- **Callback Properties** on page 710
- **File Attribute Properties** on page 711
- **File Kind Properties** on page 712
- **File Source Properties** on page 713
- **Simulator Properties** on page 714
- **Port VHDL Type Properties** on page 715
- **System Info Type Properties** on page 716
- **Design Environment Type Properties** on page 718
- **Units Properties** on page 719
- **Operating System Properties** on page 720
- **Quartus.ini Type Properties** on page 721
### 7.2.1. Script Language Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCL</td>
<td>Implements the script in Tcl.</td>
</tr>
</tbody>
</table>
### 7.2.2. Interface Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMSIS_SVD_FILE</td>
<td>Specifies the connection point’s associated CMSIS file.</td>
</tr>
<tr>
<td>CMSIS_SVD_VARIABLES</td>
<td>Defines the variables inside a .svd file.</td>
</tr>
<tr>
<td>ENABLED</td>
<td>Specifies whether or not interface is enabled.</td>
</tr>
<tr>
<td>EXPORT_OF</td>
<td>For composed _hw1.tcl files, the EXPORT_OF property indicates which interface of a child instance is to be exported through this interface. Before using this command, you must have created the border interface using add_interface. The interface to be exported is of the form &lt;instanceName.interfaceName&gt;. Example: set_interface_property CSC_input EXPORT_OF my_colorSpaceConverter.input_port</td>
</tr>
<tr>
<td>PORT_NAME_MAP</td>
<td>A map of external port names to internal port names, formatted as a Tcl list. Example: set_interface_property &lt;interface name&gt; PORT_NAME_MAP &quot;&lt;new port name&gt; &lt;old port name&gt; &lt;new port name 2&gt; &lt;old port name 2&gt;&quot;</td>
</tr>
<tr>
<td>SVD_ADDRESS_GROUP</td>
<td>Generates a CMSIS SVD file. Masters in the same SVD address group write register data of their connected slaves into the same SVD file.</td>
</tr>
<tr>
<td>SVD_ADDRESS_OFFSET</td>
<td>Generates a CMSIS SVD file. Slaves connected to this master have their base address offset by this amount in the SVD file.</td>
</tr>
<tr>
<td>SV_INTERFACE</td>
<td>When SV_INTERFACE is set, all the ports in the given interface are part of the SystemVerilog interface. Example: set_interface_property my_qsys_interface SV_INTERFACE my_sv_interface</td>
</tr>
<tr>
<td>IPXACT_REGISTER_MAP</td>
<td>Specifies the connection point’s associated IP-XACT register map file. Platform Designer supports register map files in IP-XACT 2009 or 2014 format. Example: set_interface_property my_qsys_interface IPXACT_REGISTER_MAP &lt;path_to_ipxact_reg_file&gt;</td>
</tr>
<tr>
<td>IPXACT_REGISTER_MAP_VARIABLES</td>
<td>For macro substitution inside the IP-XACT register map file. Specifies a list of key value pairs, where key is the macro name and value is the replacement text that substitutes the macros in the IP-XACT register map.</td>
</tr>
</tbody>
</table>

**Related Information**

Interfaces and Ports on page 595

### 7.2.3. SystemVerilog Interface Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SV_INTERFACE_TYPE</td>
<td>Set the interface type of the SystemVerilog interface.</td>
</tr>
<tr>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>---------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>USE_ALL_PORTS</td>
<td>When USE_ALL_PORTS is set to true, all the ports defined in the Module, are declared in this SystemVerilog interface. USE_ALL_PORTS must be set to true only if the module has one SystemVerilog interface and the SystemVerilog interface signal names match with the port names declared for Platform Designer interface. When USE_ALL_PORTS is true, SV_INTERFACE_PORT or SV_INTERFACE_SIGNAL port properties should not be set.</td>
</tr>
</tbody>
</table>
### 7.2.4. Instance Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDLINSTANCE_GET_GENERATED_NAME</td>
<td>Platform Designer uses this property to get the auto-generated fixed name when the instance property HDLINSTANCE_USE_GENERATED_NAME is set to true, and only applies to fileSet callbacks.</td>
</tr>
</tbody>
</table>
### 7.2.5. Parameter Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>AFFECTS_ELABORATION</td>
<td>Set AFFECTS_ELABORATION to false for parameters that do not affect the external interface of the module. An example of a parameter that does not affect the external interface is isNonVolatileStorage. An example of a parameter that does affect the external interface is width. When the value of a parameter changes, if that parameter has set AFFECTS_ELABORATION=false, the elaboration phase (calling the callback or hardware analysis) is not repeated, improving performance. Because the default value of AFFECTS_ELABORATION is true, the provided HDL file is normally re-analyzed to determine the new port widths and configuration every time a parameter changes.</td>
</tr>
<tr>
<td>Boolean</td>
<td>AFFECTS_GENERATION</td>
<td>The default value of AFFECTS_GENERATION is false if you provide a top-level HDL module; it is true if you provide a fileset callback. Set AFFECTS_GENERATION to false if the value of a parameter does not change the results of fileset generation.</td>
</tr>
<tr>
<td>Boolean</td>
<td>AFFECTS_VALIDATION</td>
<td>The AFFECTS_VALIDATION property marks whether a parameter's value is used to set derived parameters, and whether the value affects validation messages. When set to false, this may improve response time in the parameter editor UI when the value is changed.</td>
</tr>
<tr>
<td>String[]</td>
<td>ALLOWED_RANGES</td>
<td>Indicates the range or ranges that the parameter value can have. For integers, The ALLOWED_RANGES property is a list of ranges that the parameter can take on, where each range is a single value, or a range of values defined by a start and end value separated by a colon, such as 11:15. This property can also specify legal values and display strings for integers, such as {0:None 1:Monophonic 2:Stereo 4:Quadrophonic} meaning 0, 1, 2, and 4 are the legal values. You can also assign display strings to be displayed in the parameter editor for string variables. For example, ALLOWED_RANGES = {&quot;dev1:Cyclone IV GX&quot;&quot;dev2:Stratix V GT&quot;}.</td>
</tr>
<tr>
<td>String</td>
<td>DEFAULT_VALUE</td>
<td>The default value.</td>
</tr>
<tr>
<td>Boolean</td>
<td>DERIVED</td>
<td>When true, indicates that the parameter value can only be set by the IP component, and cannot be set by the user. Derived parameters are not saved as part of an instance's parameter values. The default value is false.</td>
</tr>
<tr>
<td>String</td>
<td>DESCRIPTION</td>
<td>A short user-visible description of the parameter, suitable for a tooltip description in the parameter editor.</td>
</tr>
<tr>
<td>String[]</td>
<td>DISPLAY_HINT</td>
<td>Provides a hint about how to display a property. The following values are possible:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- boolean--for integer parameters whose value can be 0 or 1. The parameter displays as an option that you can turn on or off.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- radio--displays a parameter with a list of values as radio buttons instead of a drop-down list.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- hexadecimal--for integer parameters, display and interpret the value as a hexadecimal number, for example: 0x000000010 instead of 16.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- fixed_size--for string_list and integer_list parameters, the fixed_size DISPLAY_HINT eliminates the add and remove buttons from tables.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_NAME</td>
<td>This is the GUI label that appears to the left of this parameter.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_UNITS</td>
<td>This is the GUI label that appears to the right of the parameter.</td>
</tr>
<tr>
<td>Type</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>-----------------------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Boolean</td>
<td>ENABLED</td>
<td>When false, the parameter is disabled, meaning that it is displayed, but greyed out, indicating that it is not editable on the parameter editor.</td>
</tr>
<tr>
<td>String</td>
<td>GROUP</td>
<td>Controls the layout of parameters in GUI.</td>
</tr>
<tr>
<td>Boolean</td>
<td>HDL_PARAMETER</td>
<td>When true, the parameter must be passed to the HDL IP component description. The default value is false.</td>
</tr>
<tr>
<td>String</td>
<td>LONG_DESCRIPTION</td>
<td>A user-visible description of the parameter. Similar to DESCRIPTION, but allows for a more detailed explanation.</td>
</tr>
<tr>
<td>String</td>
<td>NEW_INSTANCE_VALUE</td>
<td>This property allows you to change the default value of a parameter without affecting older IP components that have not explicitly set a parameter value, and use the DEFAULT_VALUE property. The practical result is that older instances continue to use DEFAULT_VALUE for the parameter and new instances use the value that NEW_INSTANCE_VALUE assigns.</td>
</tr>
<tr>
<td>String</td>
<td>SV_INTERFACE_PARAMETER</td>
<td>This parameter is used in the SystemVerilog interface instantiation. Example: set_parameter_property my_parameter SV_INTERFACE_PARAMETER my_sv_interface</td>
</tr>
<tr>
<td>String[]</td>
<td>SYSTEM_INFO</td>
<td>Allows you to assign information about the instantiating system to a parameter that you define. SYSTEM_INFO requires an argument specifying the type of information requested, &lt;info-type&gt;.</td>
</tr>
<tr>
<td>String</td>
<td>SYSTEM_INFO_ARG</td>
<td>Defines an argument to be passed to a particular SYSTEM_INFO function, such as the name of a reset interface.</td>
</tr>
<tr>
<td>(various)</td>
<td>SYSTEM_INFO_TYPE</td>
<td>Specifies one of the types of system information that can be queried. Refer to System Info Type Properties.</td>
</tr>
<tr>
<td>(various)</td>
<td>TYPE</td>
<td>Specifies the type of the parameter. Refer to Parameter Type Properties.</td>
</tr>
<tr>
<td>(various)</td>
<td>UNITS</td>
<td>Sets the units of the parameter. Refer to Units Properties.</td>
</tr>
<tr>
<td>Boolean</td>
<td>VISIBLE</td>
<td>Indicates whether or not to display the parameter in the parameterization GUI.</td>
</tr>
<tr>
<td>String</td>
<td>WIDTH</td>
<td>For a STD_LOGIC_VECTOR parameter, this indicates the width of the logic vector.</td>
</tr>
</tbody>
</table>

**Related Information**
- System Info Type Properties on page 716
- Parameter Type Properties on page 698
- Units Properties on page 719
### 7.2.6. Parameter Type Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOLEAN</td>
<td>A boolean parameter whose value is true or false.</td>
</tr>
<tr>
<td>FLOAT</td>
<td>A signed 32-bit floating point parameter. Not supported for HDL parameters.</td>
</tr>
<tr>
<td>INTEGER</td>
<td>A signed 32-bit integer parameter.</td>
</tr>
<tr>
<td>INTEGER_LIST</td>
<td>A parameter that contains a list of 32-bit integers. Not supported for HDL parameters.</td>
</tr>
<tr>
<td>LONG</td>
<td>A signed 64-bit integer parameter. Not supported for HDL parameters.</td>
</tr>
<tr>
<td>NATURAL</td>
<td>A 32-bit number that contain values 0 to (2^{32}-1) (0x7fffffff).</td>
</tr>
<tr>
<td>POSITIVE</td>
<td>A 32-bit number that contains values 1 to (2^{32}-1) (0x7fffffff).</td>
</tr>
<tr>
<td>STD_LOGIC</td>
<td>A single bit parameter whose value can be 1 or 0;</td>
</tr>
<tr>
<td>STD_LOGIC_VECTOR</td>
<td>An arbitrary-width number. The parameter property WIDTH determines the size of the logic vector.</td>
</tr>
<tr>
<td>STRING</td>
<td>A string parameter.</td>
</tr>
<tr>
<td>STRING_LIST</td>
<td>A parameter that contains a list of strings. Not supported for HDL parameters.</td>
</tr>
</tbody>
</table>
### 7.2.7. Parameter Status Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Boolean</td>
<td>ACTIVE</td>
<td>Indicates the parameter is a regular parameter.</td>
</tr>
<tr>
<td>Boolean</td>
<td>DEPRECATED</td>
<td>Indicates the parameter exists only for backwards compatibility, and may not have any effect.</td>
</tr>
<tr>
<td>Boolean</td>
<td>EXPERIMENTAL</td>
<td>Indicates the parameter is experimental, and not exposed in the design flow.</td>
</tr>
</tbody>
</table>
### 7.2.8. Port Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(various)</td>
<td>DIRECTION</td>
<td>The direction of the port from the IP component's perspective. Refer to Direction Properties.</td>
</tr>
<tr>
<td>String</td>
<td>DRIVEN_BY</td>
<td>Indicates that this output port is always driven to a constant value or by an input port. If all outputs on an IP component specify a driven_by property, the HDL for the IP component is generated automatically.</td>
</tr>
<tr>
<td>String[]</td>
<td>FRAGMENT_LIST</td>
<td>This property can be used in 2 ways: First you can take a single RTL signal and split it into multiple Platform Designer signals: add_interface_port &lt;interface&gt; alpha &lt;role&gt; &lt;direction&gt; &lt;width&gt; add_interface_port &lt;interface&gt; bar &lt;role&gt; &lt;direction&gt; &lt;width&gt; set_port_property alpha fragment_list &quot;my_rtl_signal(3:0)&quot; set_port_property bar fragment_list &quot;my_rtl_signal(6:4)&quot;. Second you can take multiple RTL signals and combine them into a single Platform Designer signal: add_interface_port &lt;interface&gt; baz &lt;role&gt; &lt;direction&gt; &lt;width&gt; set_port_property baz fragment_list &quot;rtl_signal_1(3:0) rtl_signal_2(3:0)&quot;. Note: The listed bits in a port fragment must match the declared width of the Platform Designer signal.</td>
</tr>
<tr>
<td>String</td>
<td>ROLE</td>
<td>Specifies an Avalon signal type such as waitrequest, readdata, or read. For a complete list of signal types, refer to the Avalon Interface Specifications.</td>
</tr>
<tr>
<td>String</td>
<td>SV_INTERFACE_PORT</td>
<td>This port from the module is used as I/O in the SystemVerilog interface instantiation. The top-level wrapper of the module which contains this port is from the SystemVerilog interface. Example: set_port_property port_x SV_INTERFACE_PORT my_sv_interface</td>
</tr>
<tr>
<td>String</td>
<td>SV_INTERFACE_PORT_NAME</td>
<td>This property is used only when the Platform Designer port name defined for the module is different from the port name in the SystemVerilog interface. Example: set_port_property port_x SV_INTERFACE_PORT_NAME port_a When writing the RTL, the Platform Designer port name port_x is mapped to RTL name port_a in the SystemVerilog interface</td>
</tr>
<tr>
<td>String</td>
<td>SV_INTERFACE_SIGNAL</td>
<td>This port from the module is assumed to be inside the SystemVerilog interface or the modport used by the module. The top-level wrapper of the module containing this port is unwrapped from SystemVerilog interface. Example: set_port_property port_y SV_INTERFACE_SIGNAL my_sv_interface</td>
</tr>
<tr>
<td>String</td>
<td>SV_INTERFACE_SIGNAL_NAME</td>
<td>This property is only used when the Platform Designer port name defined for the module is different from the port name in the SystemVerilog interface. Example: set_port_property port_y SV_INTERFACE_SIGNAL_NAME port_b</td>
</tr>
<tr>
<td>Type</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Boolean</td>
<td>TERMINATION</td>
<td>When true, instead of connecting the port to the Platform Designer system, it is left unconnected for output and bidir or set to a fixed value for input. Has no effect for IP components that implement a generation callback instead of using the default wrapper generation.</td>
</tr>
<tr>
<td>BigInteger</td>
<td>TERMINATION_VALUE</td>
<td>The constant value to drive an input port.</td>
</tr>
<tr>
<td>(various)</td>
<td>VHDL_TYPE</td>
<td>Indicates the type of a VHDL port. The default value, auto, selects std_logic if the width is fixed at 1, and std_logic_vector otherwise. Refer to Port VHDL Type Properties.</td>
</tr>
<tr>
<td>String</td>
<td>WIDTH</td>
<td>The width of the port in bits. Cannot be set directly. Any changes must be set through the WIDTH_EXPR property.</td>
</tr>
<tr>
<td>String</td>
<td>WIDTH_EXPR</td>
<td>The width expression of a port. The width_value_expr property can be set directly to a numeric value if desired. When get_port_property is used width always returns the current integer width of the port while width_expr always returns the unevaluated width expression.</td>
</tr>
<tr>
<td>Integer</td>
<td>WIDTH_VALUE</td>
<td>The width of the port in bits. Cannot be set directly. Any changes must be set through the WIDTH_EXPR property.</td>
</tr>
</tbody>
</table>

**Related Information**

- [Direction Properties](#) on page 702
- [Port VHDL Type Properties](#) on page 715
- [Avalon Interface Specifications](#)
### 7.2.9. Direction Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bidir</td>
<td>Direction for a bidirectional signal.</td>
</tr>
<tr>
<td>Input</td>
<td>Direction for an input signal.</td>
</tr>
<tr>
<td>Output</td>
<td>Direction for an output signal.</td>
</tr>
</tbody>
</table>
# 7.2.10. Display Item Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>DESCRIPTION</td>
<td>A description of the display item, which you can use as a tooltip.</td>
</tr>
<tr>
<td>String[]</td>
<td>DISPLAY_HINT</td>
<td>A hint that affects how the display item displays in the parameter editor.</td>
</tr>
<tr>
<td>String</td>
<td>DISPLAY_NAME</td>
<td>The label for the display item in a the parameter editor.</td>
</tr>
<tr>
<td>Boolean</td>
<td>ENABLED</td>
<td>Indicates whether the display item is enabled or disabled.</td>
</tr>
<tr>
<td>String</td>
<td>PATH</td>
<td>The path to a file. Only applies to display items of type ICON.</td>
</tr>
<tr>
<td>String</td>
<td>TEXT</td>
<td>Text associated with a display item. Only applies to display items of type TEXT.</td>
</tr>
<tr>
<td>Boolean</td>
<td>VISIBLE</td>
<td>Indicates whether this display item is visible or not.</td>
</tr>
</tbody>
</table>
# 7.2.11. Display Item Kind Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACTION</td>
<td>An action displays as a button in the GUI. When the button is clicked, it calls the callback procedure. The button label is the display item id.</td>
</tr>
<tr>
<td>GROUP</td>
<td>A group that is a child of the parent_group group. If the parent_group is an empty string, this is a top-level group.</td>
</tr>
<tr>
<td>ICON</td>
<td>A .gif, .jpg, or .png file.</td>
</tr>
<tr>
<td>PARAMETER</td>
<td>A parameter in the instance.</td>
</tr>
<tr>
<td>TEXT</td>
<td>A block of text.</td>
</tr>
</tbody>
</table>
### 7.2.12. Display Hint Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIT_WIDTH</td>
<td>Bit width of a number</td>
</tr>
<tr>
<td>BOOLEAN</td>
<td>Integer value either 0 or 1.</td>
</tr>
<tr>
<td>COLLAPSED</td>
<td>Indicates whether a group is collapsed when initially displayed.</td>
</tr>
<tr>
<td>COLUMNS</td>
<td>Number of columns in text field, for example, &quot;columns:N&quot;.</td>
</tr>
<tr>
<td>EDITABLE</td>
<td>Indicates whether a list of strings allows free-form text entry (editable combo box).</td>
</tr>
<tr>
<td>FILE</td>
<td>Indicates that the string is an optional file path, for example, &quot;file:jpg,png,gif&quot;.</td>
</tr>
<tr>
<td>FIXED_SIZE</td>
<td>Indicates a fixed size for a table or list.</td>
</tr>
<tr>
<td>GROW</td>
<td>If set, the widget can grow when the IP component is resized.</td>
</tr>
<tr>
<td>HEXADECIMAL</td>
<td>Indicates that the long integer is hexadecimal.</td>
</tr>
<tr>
<td>RADIO</td>
<td>Indicates that the range displays as radio buttons.</td>
</tr>
<tr>
<td>ROWS</td>
<td>Number of rows in text field, or visible rows in a table, for example, &quot;rows:N&quot;.</td>
</tr>
<tr>
<td>SLIDER</td>
<td>Range displays as slider.</td>
</tr>
<tr>
<td>TAB</td>
<td>If present for a group, the group displays in a tab</td>
</tr>
<tr>
<td>TABLE</td>
<td>If present for a group, the group must contain all list-type parameters, which display collectively in a single table.</td>
</tr>
<tr>
<td>TEXT</td>
<td>String is a text field with a limited character set, for example, &quot;text:A-Za-z0-9_&quot;.</td>
</tr>
<tr>
<td>WIDTH</td>
<td>Width of a table column</td>
</tr>
</tbody>
</table>
## 7.2.13. Module Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALYZE_HDL</td>
<td>When set to false, prevents a call to the Intel Quartus Prime mapper to verify port widths and directions, speeding up generation time at the expense of fewer validation checks. If this property is set to false, invalid port widths and directions are discovered during the Intel Quartus Prime software compilation. This does not affect IP components using filesets to manage synthesis files.</td>
</tr>
<tr>
<td>AUTHOR</td>
<td>The IP component author.</td>
</tr>
<tr>
<td>COMPOSITION_CALLBACK</td>
<td>The name of the composition callback. If you define a composition callback, you cannot not define the generation or elaboration callbacks.</td>
</tr>
<tr>
<td>DATASHEET_URL</td>
<td>Deprecated. Use add_documentation_link to provide documentation links.</td>
</tr>
<tr>
<td>DESCRIPTION</td>
<td>The description of the IP component, such as &quot;This IP component implements a half-rate bridge.&quot;</td>
</tr>
<tr>
<td>DISPLAY_NAME</td>
<td>The name to display when referencing the IP component, such as &quot;My Platform Designer IP Component&quot;.</td>
</tr>
<tr>
<td>EDITABLE</td>
<td>Indicates whether you can edit the IP component in the Component Editor.</td>
</tr>
<tr>
<td>ELABORATION_CALLBACK</td>
<td>The name of the elaboration callback. When set, the IP component's elaboration callback is called to validate and elaborate interfaces for instances of the IP component.</td>
</tr>
<tr>
<td>GENERATION_CALLBACK</td>
<td>The name for a custom generation callback.</td>
</tr>
<tr>
<td>GROUP</td>
<td>The group in the IP Catalog that includes this IP component.</td>
</tr>
<tr>
<td>ICON_PATH</td>
<td>A path to an icon to display in the IP component's parameter editor.</td>
</tr>
<tr>
<td>INSTANTIATE_IN_SYSTEM_MODULE</td>
<td>If true, this IP component is implemented by HDL provided by the IP component. If false, the IP component creates exported interfaces allowing the implementation to be connected in the parent.</td>
</tr>
<tr>
<td>INTERNAL</td>
<td>An IP component which is marked as internal does not appear in the IP Catalog. This feature allows you to hide the sub-IP-components of a larger composed IP component.</td>
</tr>
<tr>
<td>MODULE_DIRECTORY</td>
<td>The directory in which the hw.tcl file exists.</td>
</tr>
<tr>
<td>MODULE_TCL_FILE</td>
<td>The path to the hw.tcl file.</td>
</tr>
<tr>
<td>NAME</td>
<td>The name of the IP component, such as my_qsys_component.</td>
</tr>
<tr>
<td>OPAQUE_ADDRESS_MAP</td>
<td>For composed IP components created using a _hw.tcl file that include children that are memory-mapped slaves, specifies whether the children's addresses are visible to downstream software tools. When true, the children's address are not visible. When false, the children's addresses are visible.</td>
</tr>
<tr>
<td>PREFERRED_SIMULATION_LANGUAGE</td>
<td>The preferred language to use for selecting the fileset for simulation model generation.</td>
</tr>
<tr>
<td>REPORT_HIERARCHY</td>
<td>null</td>
</tr>
<tr>
<td>STATIC_TOP_LEVEL_MODULE_NAME</td>
<td>Deprecated.</td>
</tr>
<tr>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------------------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>STRUCTURAL_COMPOSITION_CALLBACK</td>
<td>The name of the structural composition callback. This callback is used to represent the structural hierarchical model of the IP component and the RTL can be generated either with module property COMPOSITION_CALLBACK or by ADD_FILESET with target QUARTUS_SYNTH</td>
</tr>
<tr>
<td>SUPPORTED_DEVICE_FAMILIES</td>
<td>A list of device family supported by this IP component.</td>
</tr>
<tr>
<td>TOP_LEVEL_HDL_FILE</td>
<td>Deprecated.</td>
</tr>
<tr>
<td>TOP_LEVEL_HDL_MODULE</td>
<td>Deprecated.</td>
</tr>
<tr>
<td>UPGRADEABLE_FROM</td>
<td>null</td>
</tr>
<tr>
<td>VALIDATION_CALLBACK</td>
<td>The name of the validation callback procedure.</td>
</tr>
<tr>
<td>VERSION</td>
<td>The IP component’s version, such as 10.0.</td>
</tr>
</tbody>
</table>
## 7.2.14. Fileset Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENABLE_FILE_OVERWRITE_MODE</td>
<td>null</td>
</tr>
<tr>
<td>ENABLE_RELATIVE_INCLUDE_PATHS</td>
<td>If true, HDL files can include other files using relative paths in the fileset.</td>
</tr>
<tr>
<td>TOP_LEVEL</td>
<td>The name of the top-level HDL module that the fileset generates. If set, the HDL top level must match the TOP_LEVEL name, and the HDL must not be parameterized. Platform Designer runs the generate callback one time, regardless of the number of instances in the system.</td>
</tr>
</tbody>
</table>
### 7.2.15. Fileset Kind Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXAMPLE_DESIGN</td>
<td>Contains example design files.</td>
</tr>
<tr>
<td>QUARTUS_SYNTH</td>
<td>Contains files that Platform Designer uses for the Intel Quartus Prime software synthesis.</td>
</tr>
<tr>
<td>SIM_VERILOG</td>
<td>Contains files that Platform Designer uses for Verilog HDL simulation.</td>
</tr>
<tr>
<td>SIM_VHDL</td>
<td>Contains files that Platform Designer uses for VHDL simulation.</td>
</tr>
<tr>
<td>SYSTEMVERILOG_INTERFACE</td>
<td>This file is treated as SystemVerilog interface file by the Platform Designer.</td>
</tr>
</tbody>
</table>

Example:
```
add_fileset_file mem_ifc.sv SYSTEM_VERILOG PATH ".ifc/mem_ifc.sv"
```

```bash
SYSTEMVERILOG_INTERFACE
```
### 7.2.16. Callback Properties

**Description**

This list describes each type of callback. Each command may only be available in some callback contexts.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACTION</td>
<td>Called when an ACTION display item's action is performed.</td>
</tr>
<tr>
<td>COMPOSITION</td>
<td>Called during instance elaboration when the IP component contains a subsystem.</td>
</tr>
<tr>
<td>EDITOR</td>
<td>Called when the IP component is controlling the parameterization editor.</td>
</tr>
<tr>
<td>ELABORATION</td>
<td>Called to elaborate interfaces and signals after a parameter change. In API 9.1 and later, validation is called before elaboration. In API 9.0 and earlier, elaboration is called before validation.</td>
</tr>
<tr>
<td>GENERATE_VERILOG_SIMULATION</td>
<td>Called when the IP component uses a custom generator to generates the Verilog simulation model for an instance.</td>
</tr>
<tr>
<td>GENERATE_VHDL_SIMULATION</td>
<td>Called when the IP component uses a custom generator to generates the VHDL simulation model for an instance.</td>
</tr>
<tr>
<td>GENERATION</td>
<td>Called when the IP component uses a custom generator to generates the synthesis HDL for an instance.</td>
</tr>
<tr>
<td>PARAMETER_UPGRADE</td>
<td>Called when attempting to instantiate an IP component with a newer version than the saved version. This allows the IP component to upgrade parameters between released versions of the component.</td>
</tr>
<tr>
<td>STRUCTURAL_COMPOSITION</td>
<td>Called during instance elaboration when an IP component is represented by a structural hierarchical model which may be different from the generated RTL.</td>
</tr>
<tr>
<td>VALIDATION</td>
<td>Called to validate parameter ranges and report problems with the parameter values. In API 9.1 and later, validation is called before elaboration. In API 9.0 and earlier, elaboration is called before validation.</td>
</tr>
</tbody>
</table>
### 7.2.17. File Attribute Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALDEC_SPECIFIC</td>
<td>Applies to Aldec simulation tools and for simulation filesets only.</td>
</tr>
<tr>
<td>CADENCE_SPECIFIC</td>
<td>Applies to Cadence simulation tools and for simulation filesets only.</td>
</tr>
<tr>
<td>COMMON_SYSTEMVERILOG_PACKAGE</td>
<td>The name of the common SystemVerilog package. Applies to simulation filesets only.</td>
</tr>
<tr>
<td>MENTOR_SPECIFIC</td>
<td>Applies to Mentor simulation tools and for simulation filesets only.</td>
</tr>
<tr>
<td>SYNOPSYS_SPECIFIC</td>
<td>Applies to Synopsys simulation tools and for simulation filesets only.</td>
</tr>
<tr>
<td>TOP_LEVEL_FILE</td>
<td>Contains the top-level module for the fileset and applies to synthesis filesets only.</td>
</tr>
</tbody>
</table>
### 7.2.18. File Kind Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DAT</td>
<td>DAT Data</td>
</tr>
<tr>
<td>FLI_LIBRARY</td>
<td>FLI Library</td>
</tr>
<tr>
<td>HEX</td>
<td>HEX Data</td>
</tr>
<tr>
<td>MIF</td>
<td>MIF Data</td>
</tr>
<tr>
<td>OTHER</td>
<td>Other</td>
</tr>
<tr>
<td>PLI_LIBRARY</td>
<td>PLI Library</td>
</tr>
<tr>
<td>SDC</td>
<td>Timing Constraints</td>
</tr>
<tr>
<td>SYSTEM_VERILOG</td>
<td>SystemVerilog HDL</td>
</tr>
<tr>
<td>SYSTEM_VERILOG_ENCRYPT</td>
<td>Encrypted SystemVerilog HDL</td>
</tr>
<tr>
<td>SYSTEM_VERILOG_INCLUDE</td>
<td>SystemVerilog Include</td>
</tr>
<tr>
<td>VERILOG</td>
<td>Verilog HDL</td>
</tr>
<tr>
<td>VERILOG_ENCRYPT</td>
<td>Encrypted Verilog HDL</td>
</tr>
<tr>
<td>VERILOG_INCLUDE</td>
<td>Verilog Include</td>
</tr>
<tr>
<td>VHDL</td>
<td>VHDL</td>
</tr>
<tr>
<td>VHDL_ENCRYPT</td>
<td>Encrypted VHDL</td>
</tr>
<tr>
<td>VPI_LIBRARY</td>
<td>VPI Library</td>
</tr>
</tbody>
</table>
## 7.2.19. File Source Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PATH</td>
<td>Specifies the original source file and copies to <code>output_file</code>.</td>
</tr>
</tbody>
</table>
| TEXT | Specifies an arbitrary text string for the contents of `output_file`.

### 7.2.20. Simulator Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENV_ALDEC_LD_LIBRARY_PATH</td>
<td>LD_LIBRARY_PATH when running riviera-pro</td>
</tr>
<tr>
<td>ENV_CADENCE_LD_LIBRARY_PATH</td>
<td>LD_LIBRARY_PATH when running ncsim</td>
</tr>
<tr>
<td>ENV_MENTOR_LD_LIBRARY_PATH</td>
<td>LD_LIBRARY_PATH when running modelsim</td>
</tr>
<tr>
<td>ENV_SYNOPSYS_LD_LIBRARY_PATH</td>
<td>LD_LIBRARY_PATH when running vcs</td>
</tr>
<tr>
<td>OPT_ALDEC_PLI</td>
<td>-pli option for riviera-pro</td>
</tr>
<tr>
<td>OPT_CADENCE_64BIT</td>
<td>-64bit option for ncsim</td>
</tr>
<tr>
<td>OPT_CADENCE_PLI</td>
<td>-loadpli1 option for ncsim</td>
</tr>
<tr>
<td>OPT_CADENCE_SVLIB</td>
<td>-sv_lib option for ncsim</td>
</tr>
<tr>
<td>OPT_CADENCE_SVROOT</td>
<td>-sv_root option for ncsim</td>
</tr>
<tr>
<td>OPT_MENTOR_64</td>
<td>-64 option for modelsim</td>
</tr>
<tr>
<td>OPT_MENTOR_CPPPATH</td>
<td>-cpppath option for modelsim</td>
</tr>
<tr>
<td>OPT_MENTOR_LDFLAGS</td>
<td>-ldflags option for modelsim</td>
</tr>
<tr>
<td>OPT_MENTOR_PLI</td>
<td>-pli option for modelsim</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_ACC</td>
<td>+acc option for vcs</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_CPP</td>
<td>-cpp option for vcs</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_FULL64</td>
<td>-full64 option for vcs</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_LDFLAGS</td>
<td>-LDFLAGS option for vcs</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_LLIB</td>
<td>-l option for vcs</td>
</tr>
<tr>
<td>OPT_SYNOPSYS_VPI</td>
<td>+vpi option for vcs</td>
</tr>
</tbody>
</table>
### 7.2.21. Port VHDL Type Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUTO</td>
<td>The VHDL type of this signal is automatically determined. Single-bit signals are STD_LOGIC; signals wider than one bit are STD_LOGIC_VECTOR.</td>
</tr>
<tr>
<td>STD_LOGIC</td>
<td>Indicates that the signal is not rendered in VHDL as a STD_LOGIC signal.</td>
</tr>
<tr>
<td>STD_LOGIC_VECTOR</td>
<td>Indicates that the signal is rendered in VHDL as a STD_LOGIC_VECTOR signal.</td>
</tr>
</tbody>
</table>
### 7.2.22. System Info Type Properties

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>String</td>
<td>ADDRESS_MAP</td>
<td>An XML-formatted string describing the address map for the interface specified in the system info argument.</td>
</tr>
<tr>
<td>Integer</td>
<td>ADDRESS_WIDTH</td>
<td>The number of address bits required to address all memory-mapped slaves connected to the specified memory-mapped master in this instance, using byte addresses.</td>
</tr>
<tr>
<td>String</td>
<td>AVALON_SPEC</td>
<td>The version of the interconnect. SOPC Builder interconnect uses Avalon Specification 1.0. Platform Designer interconnect uses Avalon Specification 2.0.</td>
</tr>
<tr>
<td>Integer</td>
<td>CLOCK_DOMAIN</td>
<td>An integer that represents the clock domain for the interface specified in the system info argument. If this instance has interfaces on multiple clock domains, this can be used to determine which interfaces are on each clock domain. The absolute value of the integer is arbitrary.</td>
</tr>
<tr>
<td>Long, Integer</td>
<td>CLOCK_RATE</td>
<td>The rate of the clock connected to the clock input specified in the system info argument. If 0, the clock rate is currently unknown.</td>
</tr>
<tr>
<td>String</td>
<td>CLOCK_RESET_INFO</td>
<td>The name of this instance’s primary clock or reset sink interface. This is used to determine the reset sink to use for global reset when using SOPC interconnect.</td>
</tr>
<tr>
<td>String</td>
<td>CUSTOM_INSTRUCTION_SLAVES</td>
<td>Provides custom instruction slave information, including the name, base address, address span, and clock cycle type.</td>
</tr>
<tr>
<td>(various)</td>
<td>DESIGN_ENVIRONMENT</td>
<td>A string that identifies the current design environment. Refer to Design Environment Type Properties.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE</td>
<td>The device part number of the currently selected device.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_FAMILY</td>
<td>The family name of the currently selected device.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_FEATURES</td>
<td>A list of key/value pairs delineated by spaces indicating whether a particular device feature is available in the currently selected device family. The format of the list is suitable for passing to the Tcl array set command. The keys are device features; the values are 1 if the feature is present, and 0 if the feature is absent.</td>
</tr>
<tr>
<td>String</td>
<td>DEVICE_SPEEDGRADE</td>
<td>The speed grade of the currently selected device.</td>
</tr>
<tr>
<td>Integer</td>
<td>GENERATION_ID</td>
<td>A integer that stores a hash of the generation time to be used as a unique ID for a generation run.</td>
</tr>
<tr>
<td>BigInteger, Long</td>
<td>INTERRUPTS_USED</td>
<td>A mask indicating which bits of an interrupt receiver are connected to interrupt senders. The interrupt receiver is specified in the system info argument.</td>
</tr>
<tr>
<td>Integer</td>
<td>MAX_SLAVE_DATA_WIDTH</td>
<td>The data width of the widest slave connected to the specified memory-mapped master.</td>
</tr>
<tr>
<td>String, Boolean, Integer</td>
<td>QUARTUS_INI</td>
<td>The value of the quartus.ini setting specified in the system info argument.</td>
</tr>
<tr>
<td>Integer</td>
<td>RESET_DOMAIN</td>
<td>An integer that represents the reset domain for the interface specified in the system info argument. If this instance has interfaces on multiple reset domains, this can be used to determine which interfaces are on each reset domain. The absolute value of the integer is arbitrary.</td>
</tr>
<tr>
<td>Type</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>String</td>
<td>TRISTATECONDUIT_INFO</td>
<td>An XML description of the Avalon Tri-state Conduit masters connected to an Avalon Tri-state Conduit slave. The slave is specified as the system info argument. The value contains information about the slave, the connected master instance and interface names, and signal names, directions and widths.</td>
</tr>
<tr>
<td>String</td>
<td>TRISTATECONDUIT_MASTERS</td>
<td>The names of the instance's interfaces that are tri-state conduit slaves.</td>
</tr>
<tr>
<td>String</td>
<td>UNIQUE_ID</td>
<td>A string guaranteed to be unique to this instance.</td>
</tr>
</tbody>
</table>

**Related Information**

Design Environment Type Properties on page 718
7.2.23. Design Environment Type Properties

Description
A design environment is used by IP to tell what sort of interfaces are most appropriate to connect in the parent system.

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NATIVE</td>
<td>Design environment prefers native IP interfaces.</td>
</tr>
<tr>
<td>QSYS</td>
<td>Design environment prefers standard Platform Designer interfaces.</td>
</tr>
</tbody>
</table>
### 7.2.24. Units Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address</td>
<td>A memory-mapped address.</td>
</tr>
<tr>
<td>Bits</td>
<td>Memory size, in bits.</td>
</tr>
<tr>
<td>BitsPerSecond</td>
<td>Rate, in bits per second.</td>
</tr>
<tr>
<td>Bytes</td>
<td>Memory size, in bytes.</td>
</tr>
<tr>
<td>Cycles</td>
<td>A latency or count, in clock cycles.</td>
</tr>
<tr>
<td>GigabitsPerSecond</td>
<td>Rate, in gigabits per second.</td>
</tr>
<tr>
<td>Gigabytes</td>
<td>Memory size, in gigabytes.</td>
</tr>
<tr>
<td>Gigahertz</td>
<td>Frequency, in GHz.</td>
</tr>
<tr>
<td>Hertz</td>
<td>Frequency, in Hz.</td>
</tr>
<tr>
<td>KilobitsPerSecond</td>
<td>Rate, in kilobits per second.</td>
</tr>
<tr>
<td>Kilobytes</td>
<td>Memory size, in kilobytes.</td>
</tr>
<tr>
<td>Kilohertz</td>
<td>Frequency, in kHz.</td>
</tr>
<tr>
<td>MegabitsPerSecond</td>
<td>Rate, in megabits per second.</td>
</tr>
<tr>
<td>Megabytes</td>
<td>Memory size, in megabytes.</td>
</tr>
<tr>
<td>Megahertz</td>
<td>Frequency, in MHz.</td>
</tr>
<tr>
<td>Microseconds</td>
<td>Time, in micros.</td>
</tr>
<tr>
<td>Milliseconds</td>
<td>Time, in ms.</td>
</tr>
<tr>
<td>Nanoseconds</td>
<td>Time, in ns.</td>
</tr>
<tr>
<td>None</td>
<td>Unspecified units.</td>
</tr>
<tr>
<td>Percent</td>
<td>A percentage.</td>
</tr>
<tr>
<td>Picoseconds</td>
<td>Time, in ps.</td>
</tr>
<tr>
<td>Seconds</td>
<td>Time, in s.</td>
</tr>
</tbody>
</table>
### 7.2.25. Operating System Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALL</td>
<td>All operating systems</td>
</tr>
<tr>
<td>LINUX32</td>
<td>Linux 32-bit</td>
</tr>
<tr>
<td>LINUX64</td>
<td>Linux 64-bit</td>
</tr>
<tr>
<td>WINDOWS32</td>
<td>Windows 32-bit</td>
</tr>
<tr>
<td>WINDOWS64</td>
<td>Windows 64-bit</td>
</tr>
</tbody>
</table>
## 7.2.26. Quartus.ini Type Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENABLED</td>
<td>Returns 1 if the setting is turned on, otherwise returns 0.</td>
</tr>
<tr>
<td>STRING</td>
<td>Returns the string value of the .ini setting.</td>
</tr>
</tbody>
</table>
7.3. Component Interface Tcl Reference Revision History

The table below indicates edits made to the Component Interface Tcl Reference content since its creation:

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2019.04.01</td>
<td>19.1.0</td>
<td>• Described new domain and post adaptation assignments in &quot;Interconnect Parameters&quot; topic.</td>
</tr>
<tr>
<td>2018.09.24</td>
<td>18.1.0</td>
<td>• Added new _hw.tcl interface properties that allow importing and exporting register maps in IP-XACT format.</td>
</tr>
<tr>
<td>2018.05.07</td>
<td>18.0.0</td>
<td>• Added wire-level expression commands to support wire-level interfaces.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated send_message level availability for INFO messages.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated $set_port_property availability.</td>
</tr>
<tr>
<td>2017.11.06</td>
<td>17.1.0</td>
<td>• Changed instances of Qsys Pro to Platform Designer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added statement clarifying use of brackets.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added properties and interface commands to support SystemVerilog.</td>
</tr>
<tr>
<td>2016.10.31</td>
<td>16.1.0</td>
<td>• Implemented Intel rebranding.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Implemented Qsys rebranding.</td>
</tr>
<tr>
<td>2015.11.02</td>
<td>15.1.0</td>
<td>• Changed instances of Quartus II to Quartus Prime.</td>
</tr>
<tr>
<td>2015.05.04</td>
<td>15.0.0</td>
<td>• Edit to add_filesset_file command.</td>
</tr>
<tr>
<td>December 2014</td>
<td>14.1.0</td>
<td>• $set_interface_upgrade_map</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Moved Port Roles (Interface Signal Types) section to Qsys Interconnect.</td>
</tr>
<tr>
<td>November 2013</td>
<td>13.1.0</td>
<td>• add_hdl_instance</td>
</tr>
<tr>
<td>May 2013</td>
<td>13.0.0</td>
<td>• Consolidated content from other Qsys chapters.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added AMBA APB support.</td>
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<tr>
<td>November 2012</td>
<td>12.1.0</td>
<td>• Added the demo_axis_memory example with screen shots and example_hw.tcl code.</td>
</tr>
<tr>
<td>June 2012</td>
<td>12.0.0</td>
<td>• Added AXI 3 support.</td>
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<tr>
<td></td>
<td></td>
<td>• Added: $set_display_item_property, $set_parameter_property,LONG_DESCRIPTION, and static filesets.</td>
</tr>
<tr>
<td>November 2011</td>
<td>11.1.0</td>
<td>• Template update.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added: $set_qip_strings, get_qip_strings, get_device_family_displayname, check_device_family_equivalence.</td>
</tr>
<tr>
<td>May 2011</td>
<td>11.0.0</td>
<td>• Revised section describing HDL and composed component implementations.</td>
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<tr>
<td></td>
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<td>• Separated reset and clock interfaces in example.</td>
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<td></td>
<td></td>
<td>• Added: TRISTATECONDUIT_INFO, GENERATION_ID, UNIQUE_ID SYSTEM_INFO.</td>
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<td></td>
<td>• Added: WIDTH and SYSTEM_INFO_ARG parameter properties.</td>
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<td>• Removed the doc_type argument from the add_documentation_link command.</td>
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<td></td>
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<td>• Removed: get_instance_parameter_properties</td>
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<tr>
<td></td>
<td></td>
<td>• Added: add_filesset, add_filesset_file, create_temp_file.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated Tcl examples to show separate clock and reset interfaces.</td>
</tr>
<tr>
<td>December 2010</td>
<td>10.1.0</td>
<td>• Initial release.</td>
</tr>
</tbody>
</table>

If a software version is not listed, the user guide for the previous IP core version applies.

<table>
<thead>
<tr>
<th>Intel Quartus Prime Version</th>
<th>User Guide</th>
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</table>
A. Intel Quartus Prime Pro Edition User Guides

Refer to the following user guides for comprehensive information on all phases of the Intel Quartus Prime Pro Edition FPGA design flow.

Related Information

  Introduces the basic features, files, and design flow of the Intel Quartus Prime Pro Edition software, including managing Intel Quartus Prime Pro Edition projects and IP, initial design planning considerations, and project migration from previous software versions.

  Describes creating and optimizing systems using Platform Designer, a system integration tool that simplifies integrating customized IP cores in your project. Platform Designer automatically generates interconnect logic to connect intellectual property (IP) functions and subsystems.

  Describes best design practices for designing FPGAs with the Intel Quartus Prime Pro Edition software. HDL coding styles and synchronous design practices can significantly impact design performance. Following recommended HDL coding styles ensures that Intel Quartus Prime Pro Edition synthesis optimally implements your design in hardware.

  Describes set up, running, and optimization for all stages of the Intel Quartus Prime Pro Edition Compiler. The Compiler synthesizes, places, and routes your design before generating a device programming file.

  Describes Intel Quartus Prime Pro Edition settings, tools, and techniques that you can use to achieve the highest design performance in Intel FPGAs. Techniques include optimizing the design netlist, addressing critical chains that limit retiming and timing closure, optimizing device resource usage, device floorplanning, and implementing engineering change orders (ECOs).

  Describes operation of the Intel Quartus Prime Pro Edition Programmer, which allows you to configure Intel FPGA devices, and program CPLD and configuration devices, via connection with an Intel FPGA download cable.

- Intel Quartus Prime Pro Edition User Guide: Block-Based Design
  Describes block-based design flows, also known as modular or hierarchical design flows. These advanced flows enable preservation of design blocks (or logic that comprises a hierarchical design instance) within a project, and reuse of design blocks in other projects.
Describes Partial Reconfiguration, an advanced design flow that allows you to reconfigure a portion of the FPGA dynamically, while the remaining FPGA design continues to function. Define multiple personas for a particular design region, without impacting operation in other areas.

Describes RTL- and gate-level design simulation support for third-party simulation tools by Aldec*, Cadence*, Mentor Graphics*, and Synopsys that allow you to verify design behavior before device programming. Includes simulator support, simulation flows, and simulating Intel FPGA IP.

Describes support for optional synthesis of your design in third-party synthesis tools by Mentor Graphics*, and Synopsys. Includes design flow steps, generated file descriptions, and synthesis guidelines.

Describes support for optional logic equivalence checking (LEC) of your design in third-party LEC tools by OneSpin*.

Describes a portfolio of Intel Quartus Prime Pro Edition in-system design debugging tools for real-time verification of your design. These tools provide visibility by routing (or “tapping”) signals in your design to debugging logic. These tools include System Console, Signal Tap logic analyzer, system debugging toolkits, In-System Memory Content Editor, and In-System Sources and Probes Editor.

Explains basic static timing analysis principals and use of the Intel Quartus Prime Pro Edition Timing Analyzer, a powerful ASIC-style timing analysis tool that validates the timing performance of all logic in your design using an industry-standard constraint, analysis, and reporting methodology.

Describes the Intel Quartus Prime Pro Edition Power Analysis tools that allow accurate estimation of device power consumption. Estimate the power consumption of a device to develop power budgets and design power supplies, voltage regulators, heat sink, and cooling systems.

Describes timing and logic constraints that influence how the Compiler implements your design, such as pin assignments, device options, logic options, and timing constraints. Use the Interface Planner to prototype interface implementations, plan clocks, and quickly define a legal device floorplan. Use the Pin Planner to visualize, modify, and validate all I/O assignments in a graphical representation of the target device.

Describes support for optional third-party PCB design tools by Mentor Graphics* and Cadence*. Also includes information about signal integrity analysis and simulations with HSPICE and IBIS Models.

Describes use of Tcl and command line scripts to control the Intel Quartus Prime Pro Edition software and to perform a wide range of functions, such as managing projects, specifying constraints, running compilation or timing analysis, or generating reports.